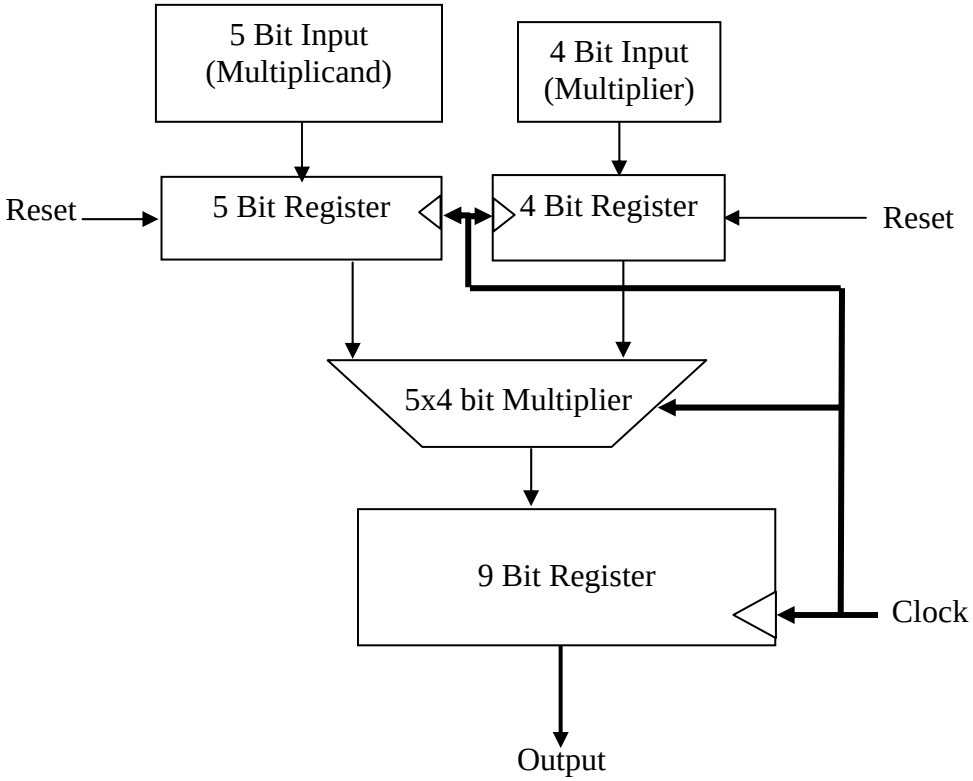
EEC 118 Spring 2010 Design Project Part 1:
Logic Design of a Pipelined Unsigned 5x4 Bit Multiplier

Design a 5x4 bit Multiplier: Since the multiplier is part of an integer execution pipeline, it should have registers at all its inputs and should have a 9 bit output register. It should also have at least one stage of pipelining within the multiplier itself. It is required to perform simple unsigned multiplication of two positive numbers, one 5 bits and the second 4 bits (no two's complement and no signed bits). It should have a reset input so that the registers may be reset.

High level organization should be as follows:



Control Signals (Reset, Clock): You do not need to design a circuit to create those. Just have SPICE provide the signals for you. Reset is an active High signal.

Multiplier: Multipliers can be implemented in a number of ways. However, an **array multiplier** is a good choice for this assignment. If you choose a different topology, please run by myself or one of the TAs.

Create the schematic. You should simulate for functional verification of the design. You must use the Altera Quartus software currently used in EEC 180A as your logic design tool. Please keep in mind that this design will be used in the final project. Design parameters for the upcoming project are that the clock frequency must be greater than 1.0 GHz with each output bit driving a 50fF load. Hence, make sure that your design does not have too many logic levels between pipeline stages.

Specs for the project are below (although all you have to do for Part 1 is design and verify functionality of design):

Area	Frequency	Cload	Output Tr/Tf
Miminize	1.0 GHz	50fF	400 ps