For all transistors: $L_{\text{min}} = 1 \mu m$, $W_{\text{min}} = 1 \mu m$, $V_{T,p} = -1 \text{V}$, $\mu_{p}C_{ox} = (1/6) \times 10^{-3} \text{A/V}^2$, $\lambda_{p} = 0.0\text{V}^{-1}$, $V_{T,n} = 1 \text{V}$, $\mu_{n}C_{ox} = (1/2) \times 10^{-3} \text{A/V}^2$, $\lambda_{n} = 0.0\text{V}^{-1}$.

**Problem 1 (5 points)** Design a four-input static CMOS logic gate which implements the Boolean expression $F = A \cdot B \cdot C + D$. Clearly label all inputs, outputs, and power supply connections. Pick sizes for the transistors such that the worst case rise and fall times of the output are equal to a minimum-sized inverter.

**Problem 2 (5 points)** A step input is applied at time $t=0$ to the loaded inverter with dimensions and initial conditions as shown below. What is the current $I_L$ immediately after the step is applied?

$$
I_L = \left( \frac{1}{2} \times 10^{-3} \text{A/V}^2 \right) \left( 3.0 \text{V} - (-1 \text{V}) \right)^2 \approx 1.67 \text{mA} \quad (0.5 \text{pt.})
$$