EEC 116 Lecture #4: CMOS Inverter AC Characteristics

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Acknowledgments

- Slides due to Rajit Manohar from ECE 547 Advanced VLSI Design at Cornell University

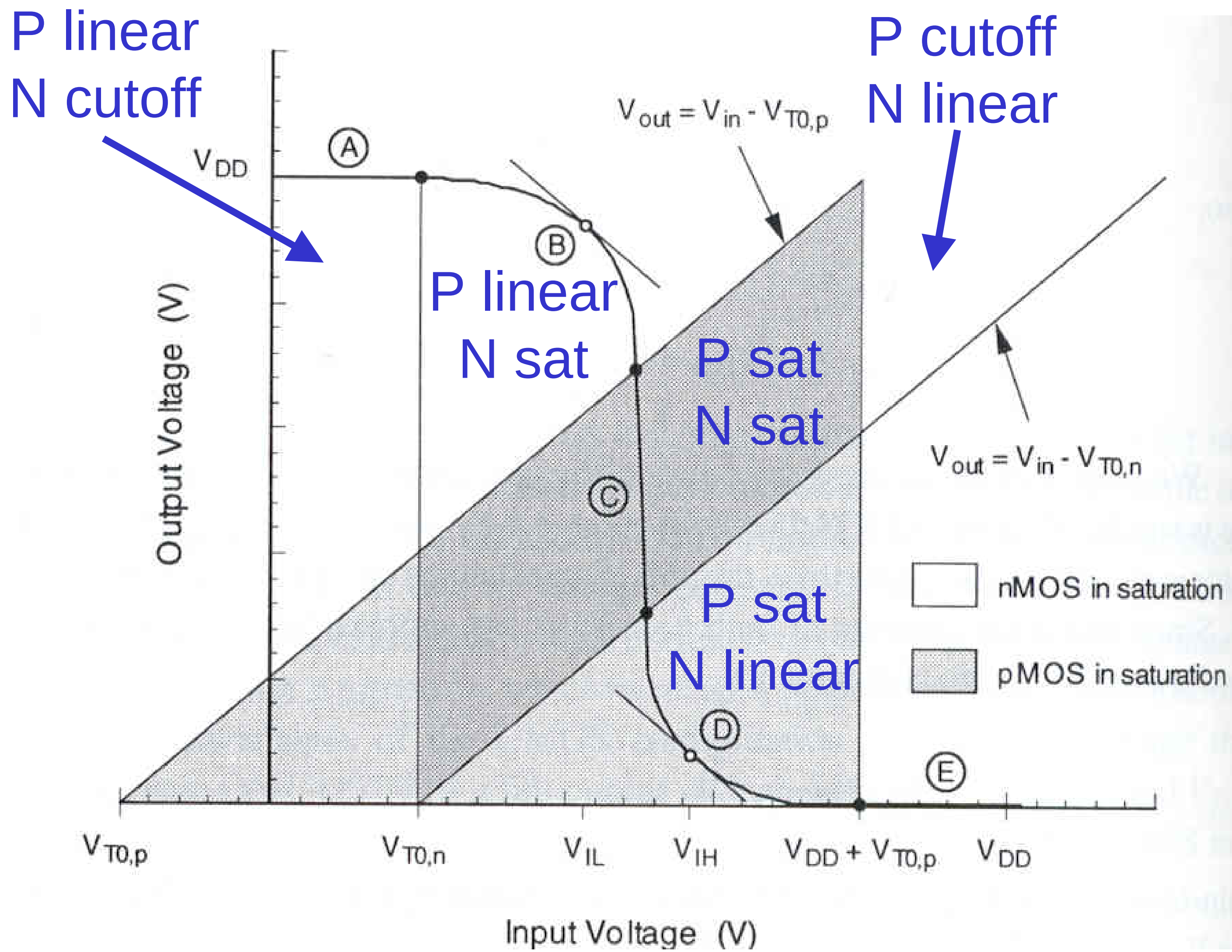
Announcements

- **Lab 2 this week, report due next week**
- **Quiz 1 on Monday!**

Outline

- **Review: CMOS Inverter Transfer Characteristics**
- **Finish Lecture 3 slides**
- **CMOS Inverters: Rabaey 5.4-5.5 (Kang & Leblebici, 6.1-6.4, 6.7)**

CMOS Inverter VTC: Device Operation



Logic Circuit Delay

- **For CMOS (or almost all logic circuit families), only one fundamental equation necessary to determine delay:**

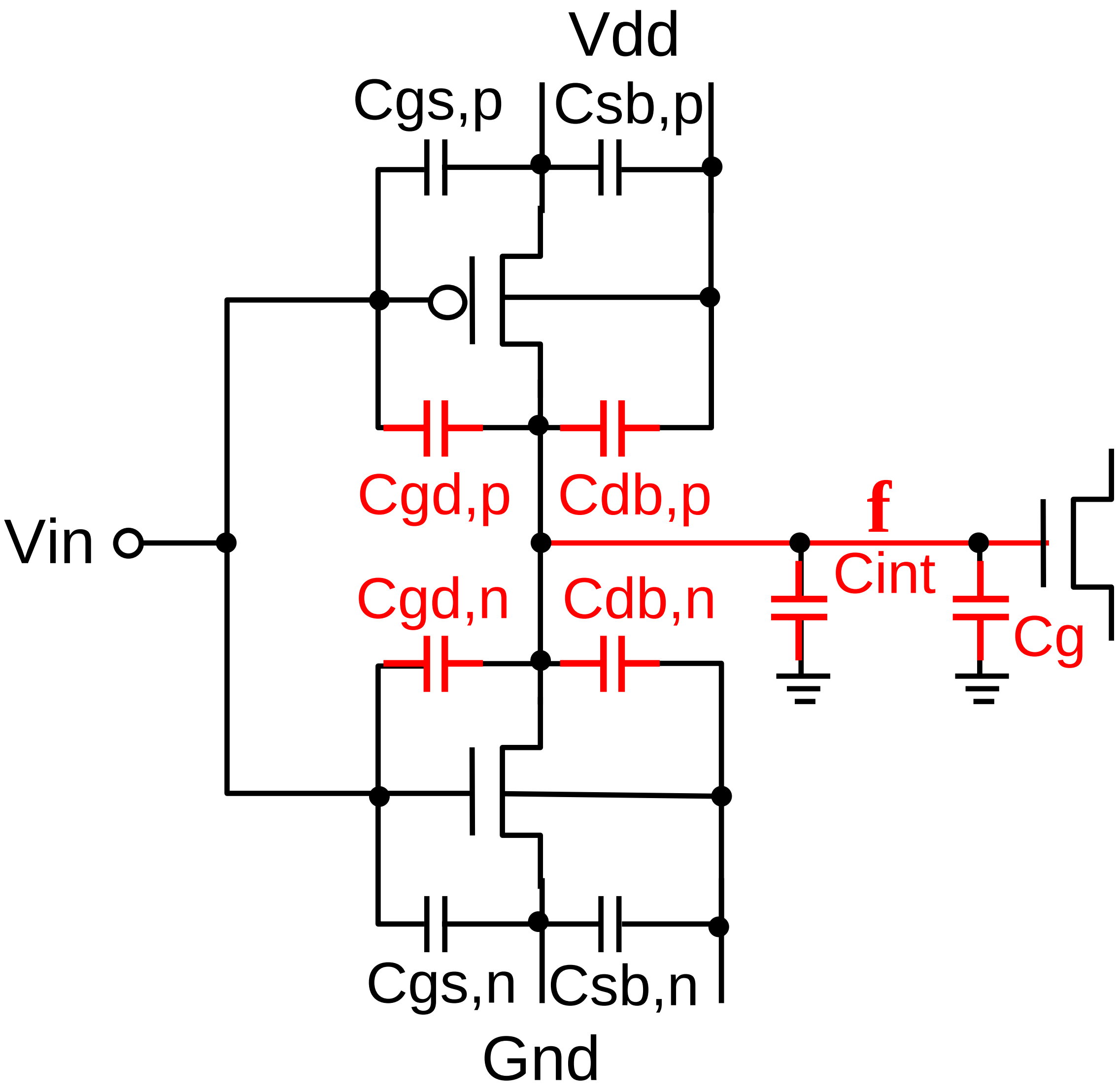
$$I = C\frac{dV}{dt}$$

- **Consider the discretized version:** $I = C\frac{\Delta V}{\Delta t}$

- **Rewrite to solve for delay:** $\Delta t = C\frac{\Delta V}{I}$

- **Only three ways to make faster logic:** $\downarrow$**C,** $\downarrow$**ΔV,** $\uparrow$**I**

CMOS Inverter Capacitances



- Assume input transition is fixed, then delay determined by output

<u>Capacitance on node f (output):</u>

- Junction cap Cdb,p and Cdb,n
- Gate capacitance Cgd,p and Cgd,n
- Interconnect cap
- Receiver gate cap

CMOS Inverter Junction Capacitances

- **Junction capacitances $C_{db,p}$ and $C_{db,n}$:**
  - Equation for junction cap:

$$C_j(V) = \frac{AC_{j0}}{\left(1 - \frac{V}{\phi_0}\right)^m}, \qquad C_{j0} = \left(\frac{\varepsilon q}{2} \frac{N_a N_d}{N_a + N_d} \frac{1}{\phi_0}\right)^m$$

  - Non-linear, depends on voltage across junction
  - Use K_{eq} factor to get equivalent capacitance for a voltage transition

$$C_{db} = AK_{eq}C_j + PK_{eqsw}C_{jsw}$$

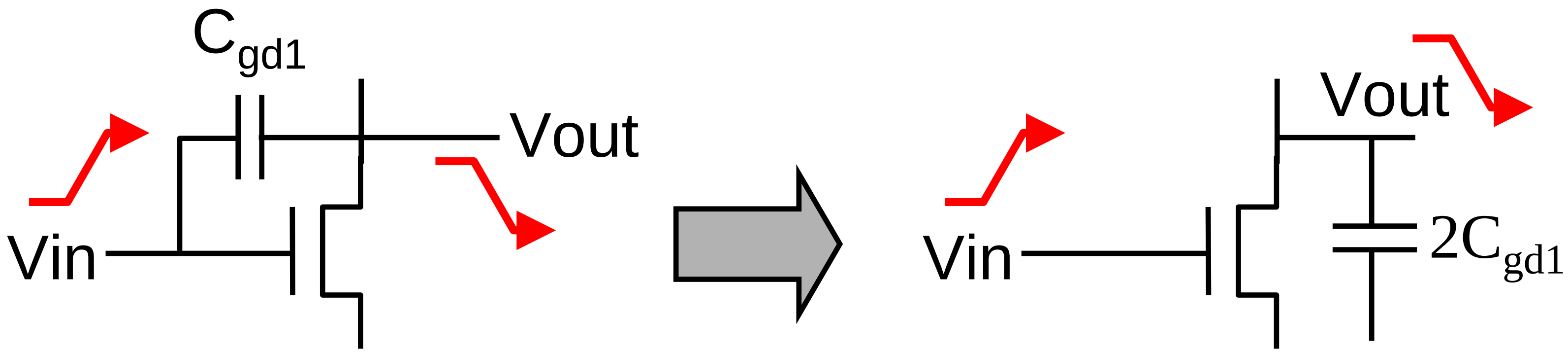
CMOS Inverter Gate Capacitances

- **Gate capacitances $C_{GD,p}$ and $C_{GD,n}$:**
  - Just after the input switches($t = 0^+$), what regions are transistors in?
  - One is in cutoff: C_{GD} = Overlap Cap
  - One is in Saturation: C_{GD} = Overlap Cap
  - Therefore, gate-to-drain capacitance is due to overlap capacitance :

$$C_{gd,p} = C_{gd,n} = C_{ox} W L_D$$

However, also need to consider ***Miller effect*** ...

CMOS Inverter Capacitances: Miller Effect



- **When input rises by ΔV, output falls by ΔV**
  - Change in stored charge: $\Delta Q = C_{gd1}\Delta V - (-C_{gd1}\Delta V)$
  - Effective voltage change across C_{gd1} is $2\Delta V$
  - Effective capacitance to ground is *twice* C_{gd1}
- **Including Miller effect:**

$$C_{gd,p} = C_{gd,n} = 2C_{ox}WL_D$$ (For transistor in Cutoff)

CMOS Inverter Capacitances: Receiver

- **Receiver gate capacitance**
  - Includes all capacitances of gate(s) connected to output node
  - Unknown region of operation for receiver transistor: total gate cap varies from (2/3)WLC_{ox} to WLC_{ox}
  - Ignore Miller effect (taken into account on output)
  - Assume worst-case value, include overlap

$$C_g = WL_{eff}C_{ox} + 2WL_DC_{ox}$$

$$\mathrm{C_g = WL\ C_{ox}}$$

Inverter Capacitances: Analysis

- **Simplify the circuit: combine all capacitances at output into one lumped linear capacitance:**

  C_{load} = 2*Cgd,n + 2*Cgd,p + Cdb,n + Cdb,p + Cint + Cg

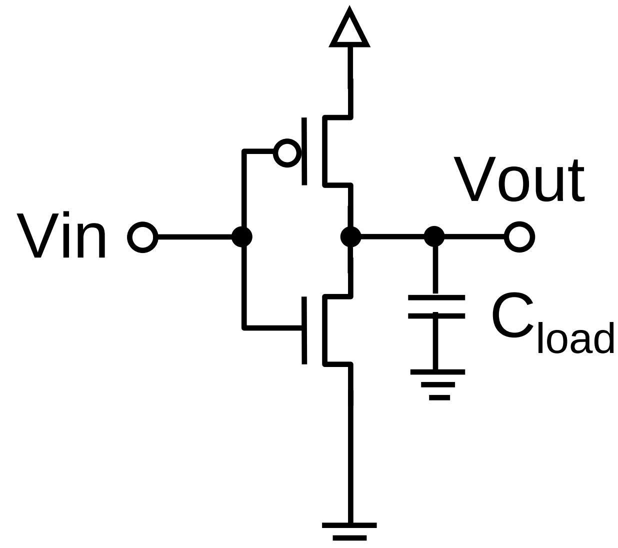
  Miller effect

- **Csb,n = Csb,p = 0**

- **Cgs,n and Cgs,p are not connected to the load. These are part of the gate capacitance Cg**

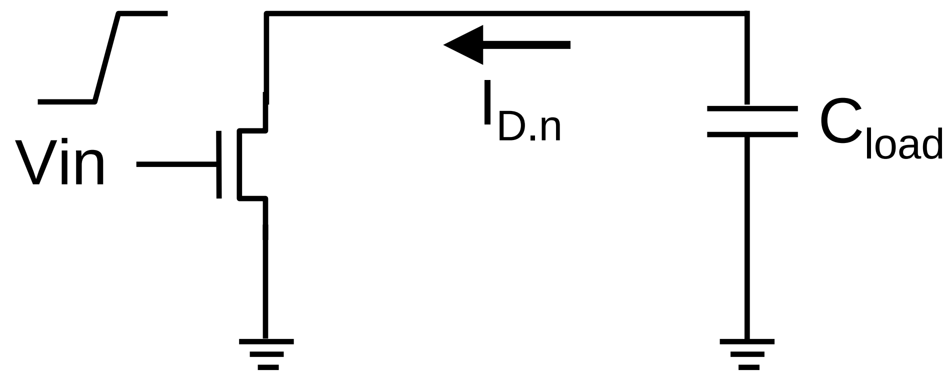
First-Order Inverter Delay

- **Suppose ideal voltage step at input**
- **Assume: Current charging or discharging capacitance C_{load} is nearly constant I_{avg}**



- $t_{PHL} = C_{load}\ (Vdd - Vdd/2)\ /\ I_{avg}$
- $t_{PLH} = C_{load}\ (Vdd/2 - Vss)\ /\ I_{avg}$

Inverter Delay: Falling

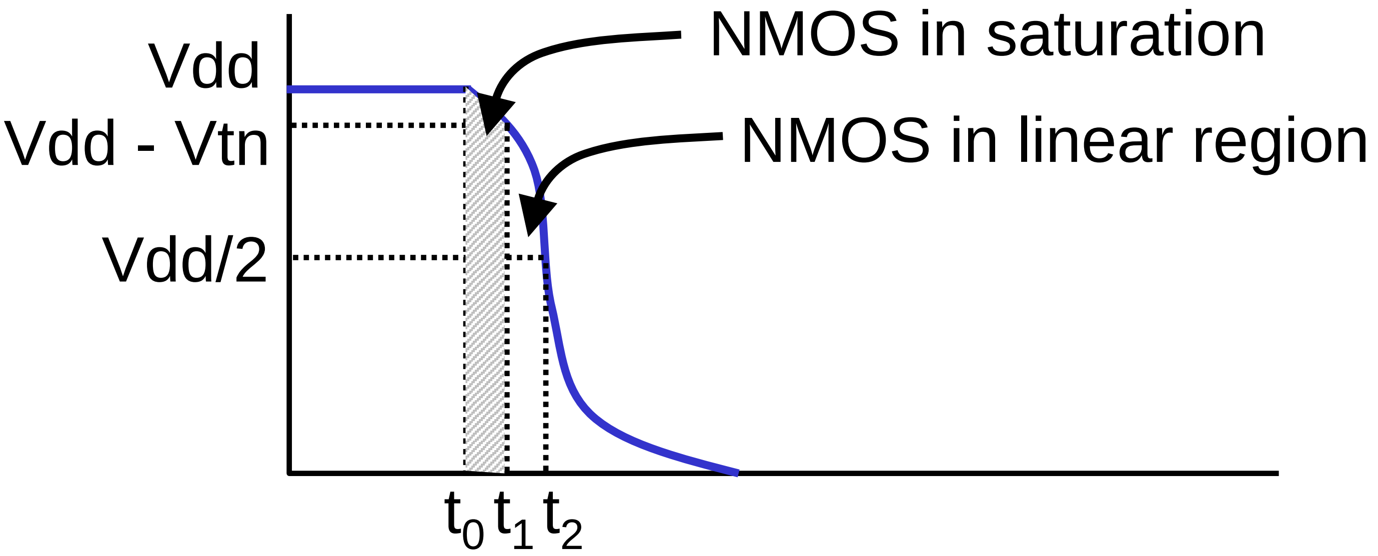


- **Assume PMOS fully off (ideal step input, $I_{D,p} = 0$)**

$$I = C\frac{dV}{dt}$$

$$I_{D,n} = C_{load}\frac{dV_{out}}{dt} \quad \Longrightarrow \quad \text{Need to determine } I_{D,n}$$

Inverter Delay: Falling



- **From t_0 to t_1: NMOS in saturation**
- **From t_1 to t_2: NMOS in linear region**
- **Find I_D in each region**

Inverter Delay: Falling t_1-t_0

- **Assumption: Input fast enough to go through transition before output voltage changes**
- **V_{out} drops from V_{OH} to V_{DD}-V_{TN} (NMOS saturated)**

$$I_{DS} = k_n (V_{in} - V_{T0,n})^2 / 2 = k_n (V_{OH} - V_{T0,n})^2 / 2$$

$$\int_{t_0}^{t_1} dt = \frac{-2C_L}{k_n (V_{OH} - V_{T0,n})^2} \int_{V_{OH}}^{V_{OH} - V_{T0,n}} dV_{out}$$

$$t_1 - t_0 = \frac{2C_L V_{T0,n}}{k_n (V_{OH} - V_{T0,n})^2}$$

Inverter Delay: Falling t_2-t_1

- V_{out} drops from (V_{OH}-$V_{T0,n}$) to $V_{DD}/2$
- NMOS in linear region

$$I_{DS} = k_n\left[(V_{OH} - V_{T0,n})V_{out} - \tfrac{1}{2}V_{out}^2\right]$$

$$t_2 - t_1 = -C_L \int_{V_{OH}-V_{T0,n}}^{(V_{OH}+V_{OL})/2} \frac{dV_{out}}{k_n\left[(V_{OH} - V_{T0,n})V_{out} - \tfrac{1}{2}V_{out}^2\right]}$$

$$t_2 - t_1 = \frac{C_L}{k_n(V_{OH} - V_{T0,n})} \ln\left[\frac{2(V_{OH} - V_{T0,n}) - (V_{OH} + V_{OL})/2}{(V_{OH} + V_{OL})/2}\right]$$

Inverter Delay: Falling, Total

- **Total fall delay = $(t_1 - t_0) + (t_2 - t_1)$**

$$t_{PHL} = \frac{C_L}{k_n (V_{OH} - V_{T0,n})} \left[\frac{2V_{T0,n}}{V_{OH} - V_{T0,n}} + \ln\left(\frac{4(V_{OH} - V_{T0,n})}{V_{OH} + V_{OL}} - 1 \right) \right]$$

Inverter Delay: Rising

- **Similar calculation as for falling delay**
- **Separate into regions where PMOS is in linear, saturation**

$$t_{PLH} = \frac{C_L}{k_p(V_{OH} - V_{OL} - |V_{T0,p}|)}\left[\frac{2|V_{T0,p}|}{V_{OH} - V_{OL} - |V_{T0,p}|} + \ln\left(\frac{4(V_{OH} - V_{OL} - |V_{T0,p}|)}{V_{OH} + V_{OL}} - 1\right)\right]$$

- **Note: to balance rise and fall delays (assuming $V_{OH} = V_{DD}$, $V_{OL} = 0V$, and $V_{T0,n}=V_{T0,p}$) requires**

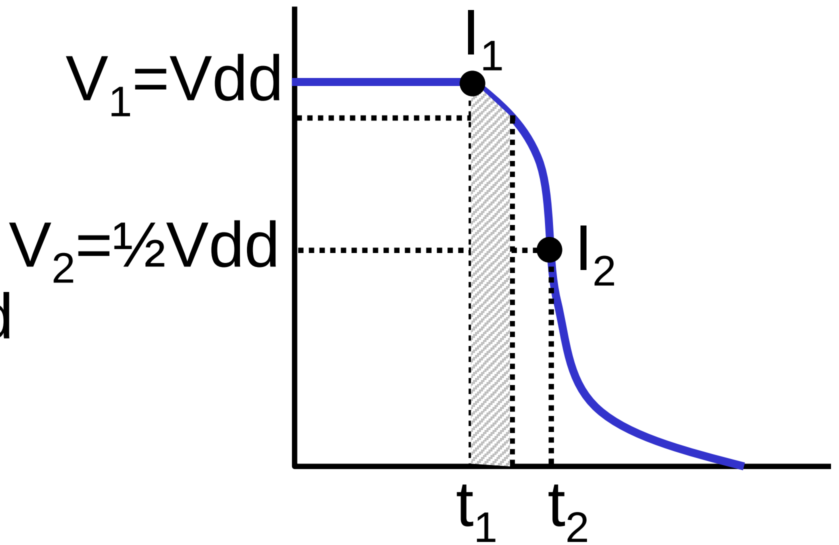
$$\frac{k_p}{k_n} = 1 \qquad \frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} = \frac{\mu_n}{\mu_p} \approx 2.5$$

Inverter Rise, Fall Times

- **Summary -- Exact method: separate into two regions**
  - t_1
    - V_{out} drops from $0.9V_{DD}$ to V_{DD}-$V_{T,n}$ (NMOS in saturation)
    - V_{out} rises from $0.1V_{DD}$ to $|V_{T,p}|$ (PMOS in saturation)
  - t_2
    - V_{out} drops from V_{DD}-$V_{T,n}$ to $0.1V_{DD}$ (NMOS in linear region)
    - V_{out} rises from $|V_{T,p}|$ to $0.9\ V_{DD}$ (PMOS in linear region)
  - $t_{f,r} = t_1 + t_2$

CMOS Inverter Delay

- **Review of approximate method**
  - Assume a constant average current for the transition
  - I_{avg} = average of drain current at beginning and end of transition



$I_{avg} = \frac{1}{2}(I_1+I_2)$

$$t_{PHL} = \frac{C_{load}}{I_{avg}}\left(V_{DD} - \tfrac{1}{2}V_{DD}\right)$$

$$t_{PLH} = \frac{C_{load}}{I_{avg}}\left(\tfrac{1}{2}V_{DD} - V_{SS}\right)$$

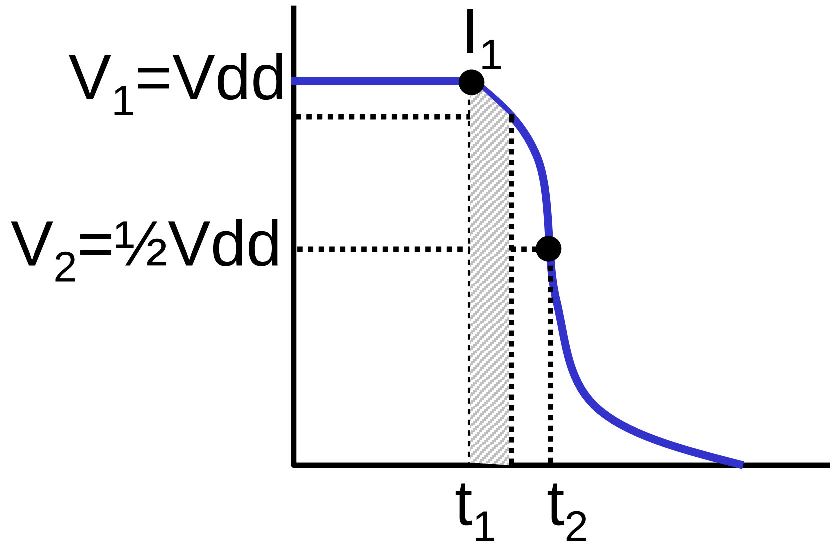
CMOS Inverter Delay: 2nd Approximation

- **Another approximate method:**
  - Again assume constant I_{avg}
  - I_{avg} = current I_1 at start of transition

$$t_{PHL} = \frac{C_{load} V_{DD}}{k_n \left(V_{DD} - V_{Tn}\right)^2}$$

$$t_{PLH} = \frac{C_{load} V_{DD}}{k_p \left(V_{DD} - \left|V_{TP}\right|\right)^2}$$

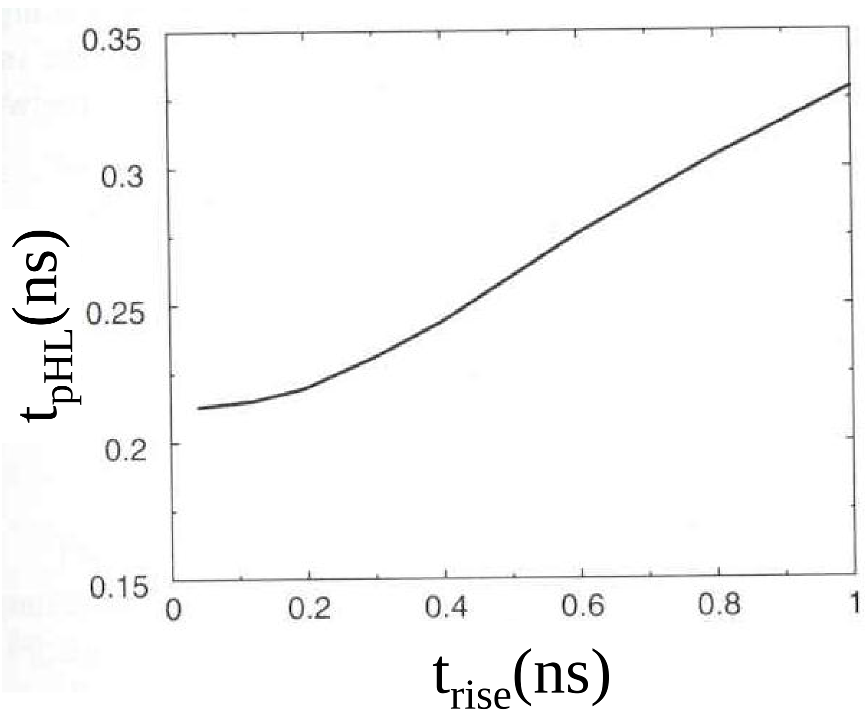
  - Why is this a good approximation (esp. for deep submicron)?



$I_{avg} = I_1$

CMOS Inverter Delay: Finite Input Transitions

- **What if input has finite rise/fall time?**
  - Both transistors are on for some amount of time
  - Capacitor charge/discharge current is reduced



Empirical equations:

$$t_{phl}(actual) = \sqrt{t_{phl}^2(step) + \left(\frac{t_r}{2}\right)^2}$$

$$t_{plh}(actual) = \sqrt{t_{plh}^2(step) + \left(\frac{t_f}{2}\right)^2}$$

How to Improve Delay?

- **Minimize load capacitances**
  - Small interconnect capacitance
  - Small Cg of next stage
- **Raise supply voltage**
  - Increases current faster than increased swing ΔV
- **Increase transistor gain factor**
  - Increase transistor drive current for charging/discharging output capacitance
- **Use low threshold voltage devices**
  - More subthreshold leakage power dissipation

Inverter Power Consumption

- **Static power consumption (ideal) = 0**
  - Actually DIBL (Drain-Induced Barrier Lowering), gate leakage, junction leakage are still present
- **Dynamic power consumption**

$$P_{avg} = \frac{1}{T}\int_0^T v(t)i(t)dt$$

$$P_{avg} = \frac{1}{T}\left[\int_0^{T/2} V_{out}\left(-C_{load}\frac{dV_{out}}{dt}\right)dt + \int_{T/2}^{T}\left(V_{DD} - V_{out}\right)\left(C_{load}\frac{dV_{out}}{dt}\right)dt\right]$$

$$P_{avg} = \frac{1}{T}\left[\left(-C_{load}\frac{V_{out}{}^2}{2}\right)\Bigg|_0^{T/2} + \left(V_{DD}V_{out}C_{load} - \frac{1}{2}C_{load}V_{out}{}^2\right)\Bigg|_{T/2}^{T}\right]$$

$$P_{avg} = \frac{1}{T}C_{load}V_{DD}^2 = C_{load}V_{DD}^2 f$$

Next Time: Combinational Logic and Layout

- **Combinational MOS Logic**
  - DC Characteristics, Equivalent Inverter method
  - AC Characteristics, Switch Model
- **Combinational Logic Layout**