EEC 116 Lecture #1: Course Overview

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- **Slides 13-17 Adapted from CSE477 VLSI Digital Circuits Lecture Slides by Vijay Narayanan and Mary Jane Irwin, Penn State University**

Outline

- **Administrative Details**
- **Survey of Digital IC Technology**
- **MOS Fabrication**
- **Layout Overview**
- **MOSFET Overview**

Personnel

- **Prof. Raj Amirtharajah (Instructor)**
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  Please put EEC 116 in email subject line.
  Office Hours: F 2 - 3 PM or by appointment.
- **Stanley Hsu**
  Email: swhsu@ucdavis.edu
  Office Hours: Tu 2-4 2107 Kemper
- **Labs**
  Wednesdays 6 PM – 9 PM 2107 Kemper

Course Materials

- **Textbook**

  Digital Integrated Circuits (2nd ed.)
  by J. Rabaey, A. Chandrakasan, and B. Nikolic

- **Suggested References**

  CMOS Digital Integrated Circuits (3rd ed.) Kang and Leblebici
  CMOS VLSI Design (4th ed.) Weste, Harris (or earlier editions)

- **Handouts**

  Labs, lab report cover sheets, slides, and lecture notes available on course web page in PDF format.

- **Web Page**

  http://www.ece.ucdavis.edu/~ramirtha/EEC116/F11/F11.html
  Linked from SmartSite

Grading

- **Letter**
- **A: 100 - 90%**
- **B: 90 - 80%**
- **C: 80 - 70%**
- **D: 70 - 60%**
- **F: below 60%**

- **Expect class average to be around B- / C+**
- **Curving will only help you**

Weighting

- **Labs 35%**
- **Weekly Homework 5%**

  Scale for each problem: 0 = poor effort, 1 = close, but fundamental problem, 2 = correct
- **Quizzes 10%**

  Four throughout the quarter (approx. every other week), lowest score dropped (April 11, April 25, May 18, May 25)
- **Midterm 20%**

  Monday, October 31, in class
- **Final 30%**

  Wednesday, December 7, 1:00 - 3:00 PM

  Cumulative, but emphasizes material after midterm

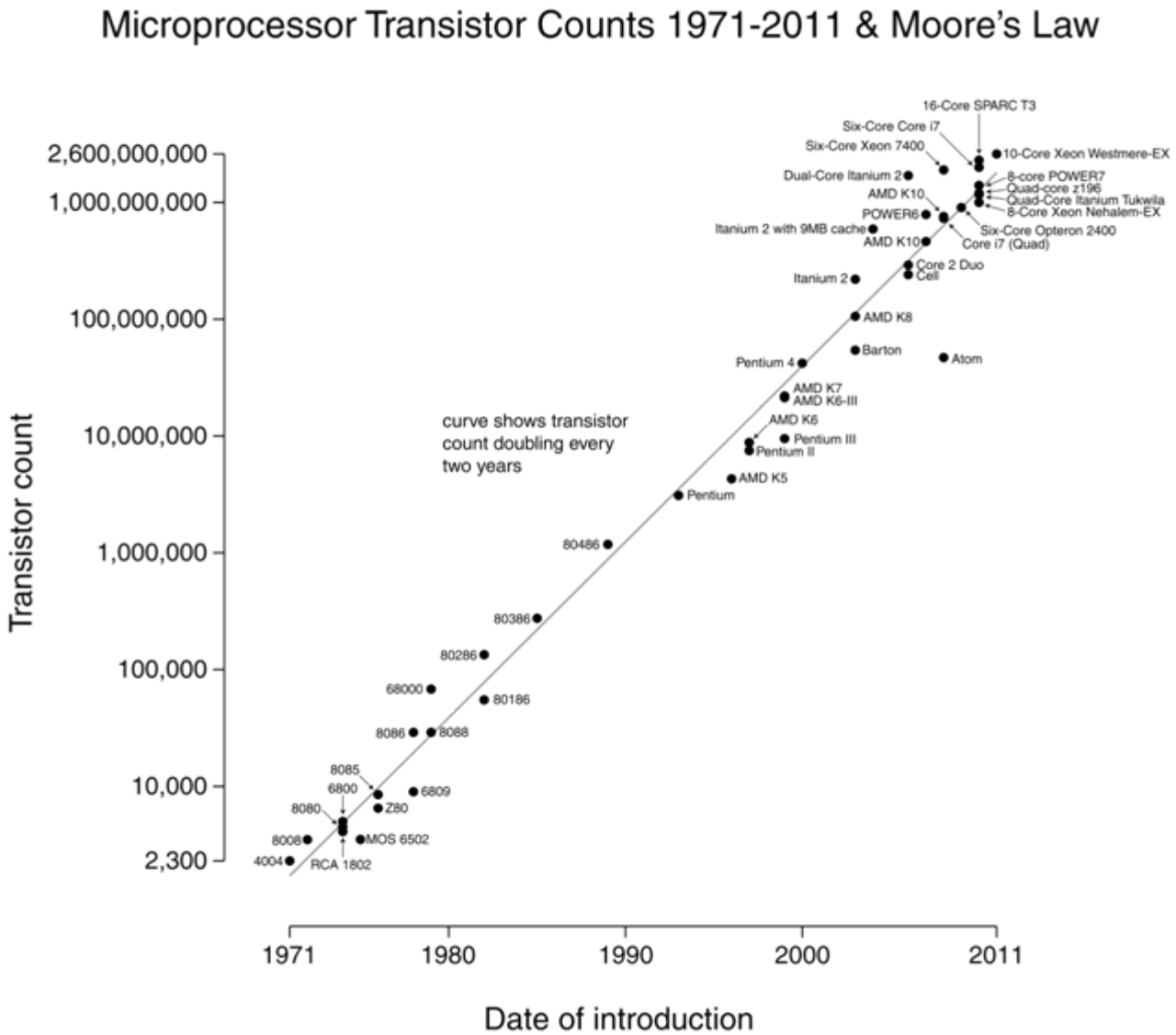
Colored Pencils

- **Buy colored pencils or pens whose colors match Cadence layout tool layer colors**
  - green
  - brown (orange next closest?)
  - red
  - blue
  - purple
- **Used for “stick diagrams”**
- **Slightly transparent pencils or pens work best**

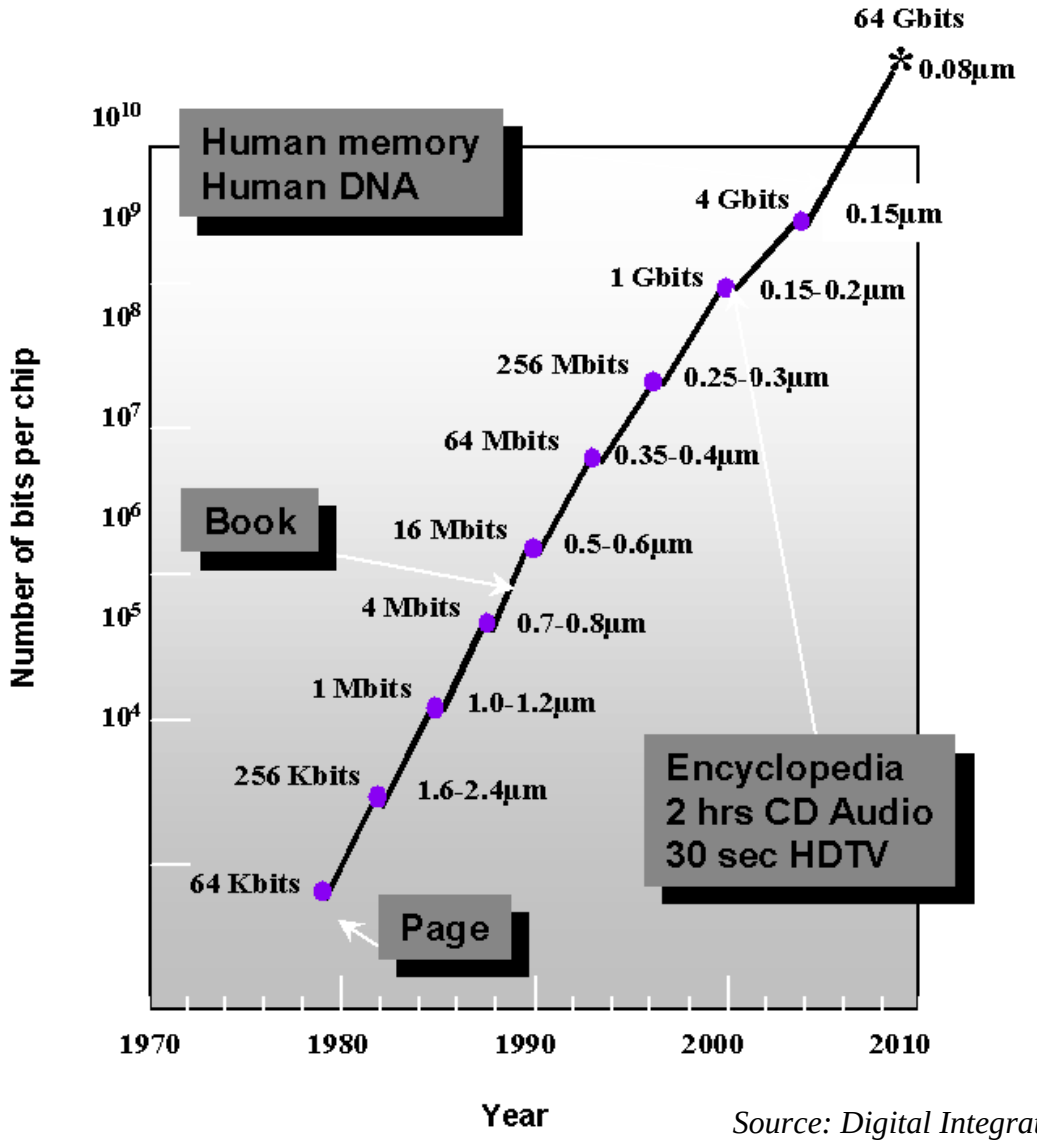
Labs and CAD Software Usage

- **Need to know/learn Cadence/Spectre – Circuit Simulation**
- **Can work on labs remotely using VNC, etc.**

Moore's Law


Microprocessor Transistor Counts 1971-2011 & Moore's Law
Transistor count
2,600,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
2,300
curve shows transistor count doubling every two years
16-Core SPARC T3
Six-Core Core i7
Six-Core Xeon 7400
10-Core Xeon Westmere-EX
Dual-Core Itanium 2
8-core POWER7
Quad-core z196
AMD K10
Quad-Core Itanium Tukwila
POWER6
8-Core Xeon Nehalem-EX
Itanium 2 with 9MB cache
Six-Core Opteron 2400
AMD K10
Core i7 (Quad)
Core 2 Duo
Cell
Itanium 2
AMD K8
Barton
Pentium 4
Atom
AMD K7
AMD K6-III
AMD K6
Pentium III
Pentium II
AMD K5
Pentium
80486
80386
80286
68000
80186
8086
8088
8085
6800
6809
8080
Z80
8008
MOS 6502
4004
RCA 1802
1971
1980
1990
2000
2011
Date of introduction

Advances in Memory Density



Source: Digital Integrated Circuits, 2nd ©

Hybrid to Monolithic Trend

- **We continue to integrate multiple functions on a single chip**
  - Mixture of Analog, Radio Frequency (RF), Digital
  - Graphics/Motherboard chipset an example of this
- **Cost and Performance driving market**
  - Higher performance achieved on chip than off chip
  - Lower cost due to a single die versus multi-chip design
  - Saves on packaging, total area by eliminating redundant functions
- **System-on-a-Chip (SOC) concept**

Education Demand for Circuit Design

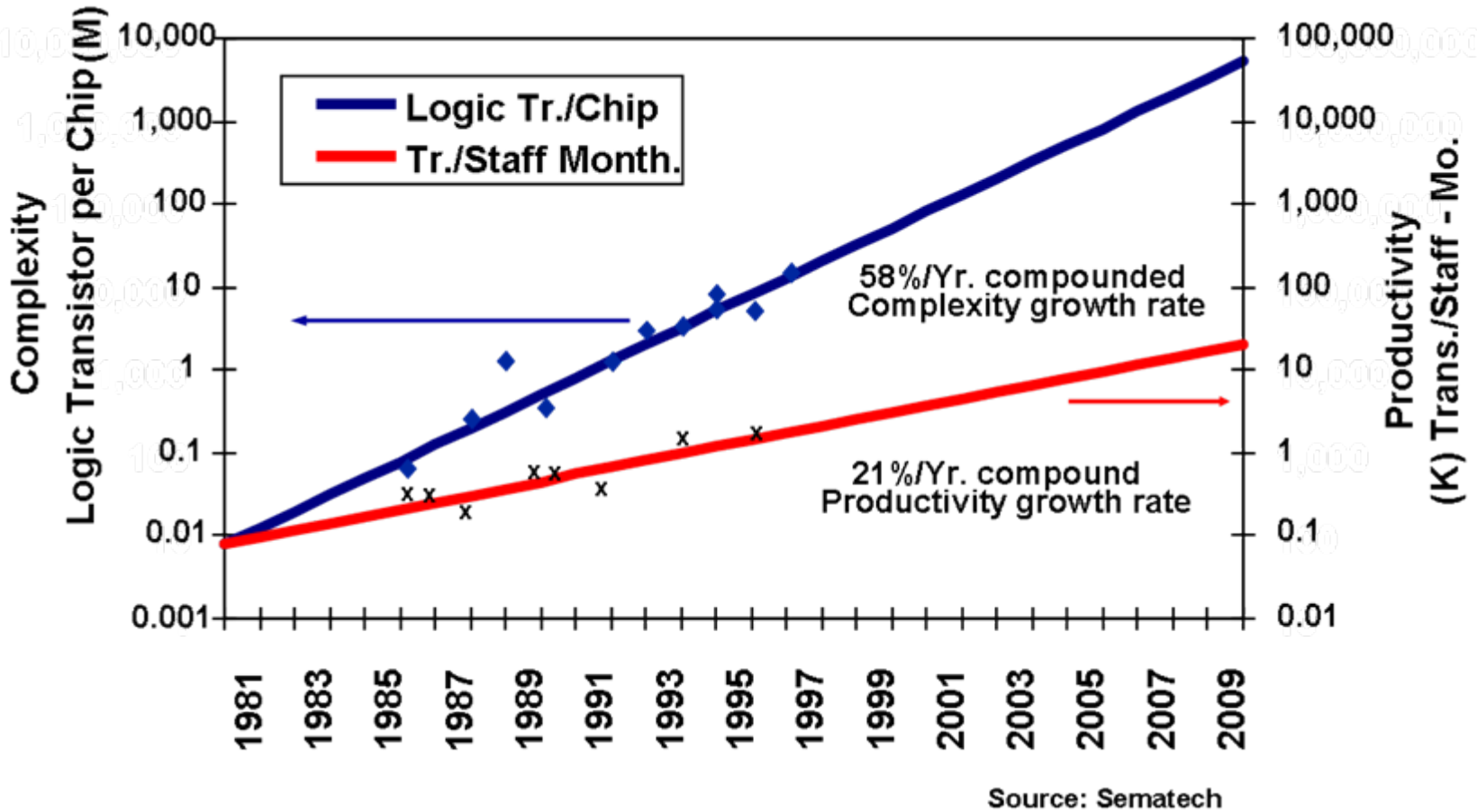
- **Industry needs circuit designers**
  - Not just logic designers
    - Must understand operation at transistor level
  - Not just digital designers
    - Must understand analog effects
  - Not just analog designers
    - Must be able to comprehend Deep Sub-Micron (DSM) effects (<0.13um)
- **Fundamental circuit knowledge critical**
  - Similar techniques for bipolar transistors, NMOS (even relays and vacuum tubes!)
  - Must be able to exploit nanoscale devices in future

Education Demand for System Design

- **Industry needs system designers**
  - Need to understand system implications of your design
    - Power Delivery, Clock Loading – What do you need
  - Need to design from the system point of view
    - Communication protocol – how to effectively talk with other blocks
    - What should be added into your block to meet system design requirements(i.e. comprehend soft block methodology for optimization of area, interconnect, etc.)

You must operate at both levels!

Productivity Trends



Complexity outpaces design productivity

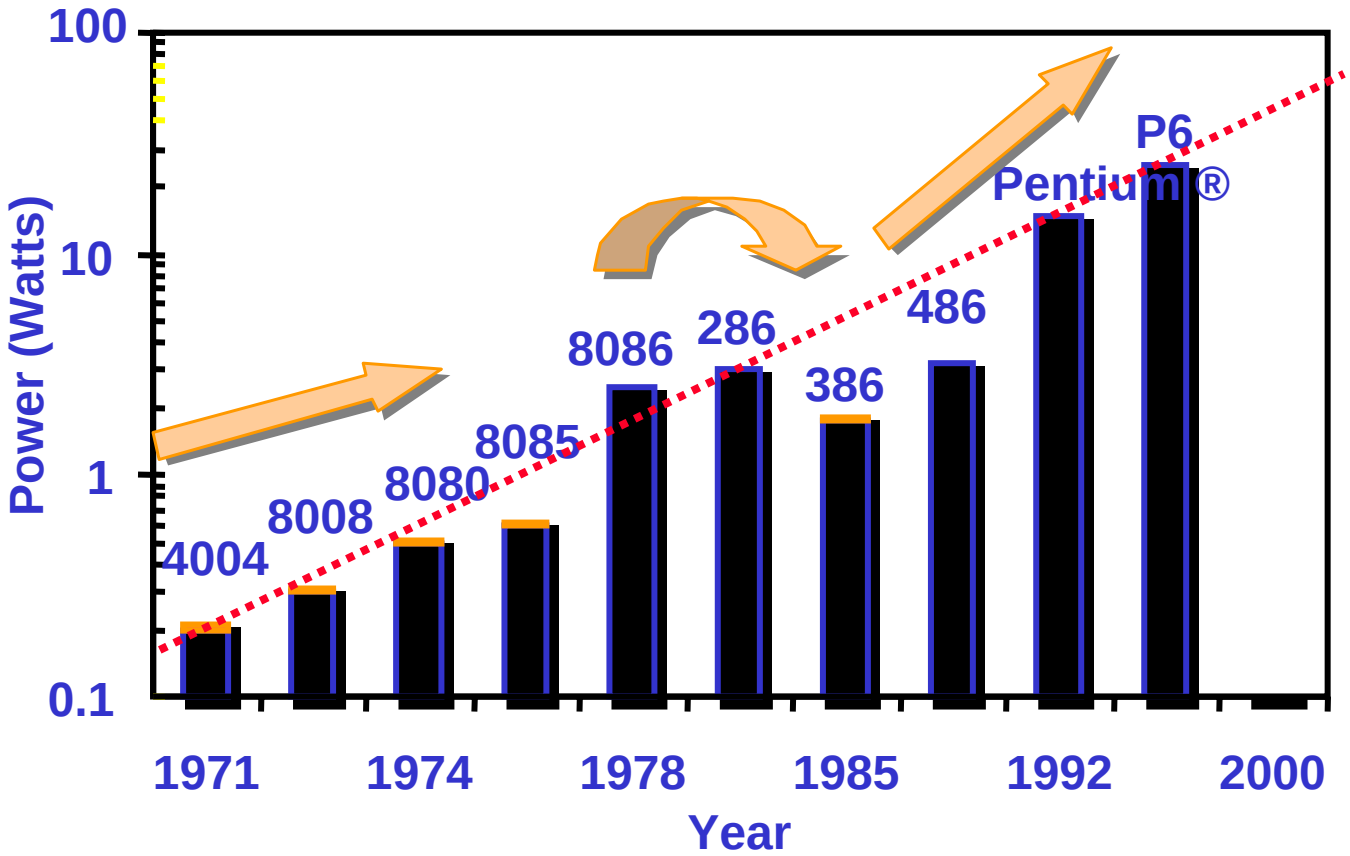
Courtesy, ITRS Roadmap

What are the issues facing the industry ?

- **Growth of transistors is exponential**
- **Growth of operating frequency is (was?) exponential**
  - Reaching a limit due to power dissipation (see current generation Pentiums and Itaniums)
- **Complexity continues to grow**
  - Trend is toward multiple cores on one chip
  - Design teams cannot keep up with trend
- **Power dissipation a concern**
  - Power delivery, thermal issues, long term reliability
- **Manufacturing providing us with lots of transistors**
  - How do we use them effectively (besides large caches)?

Why worry about power? Power Dissipation

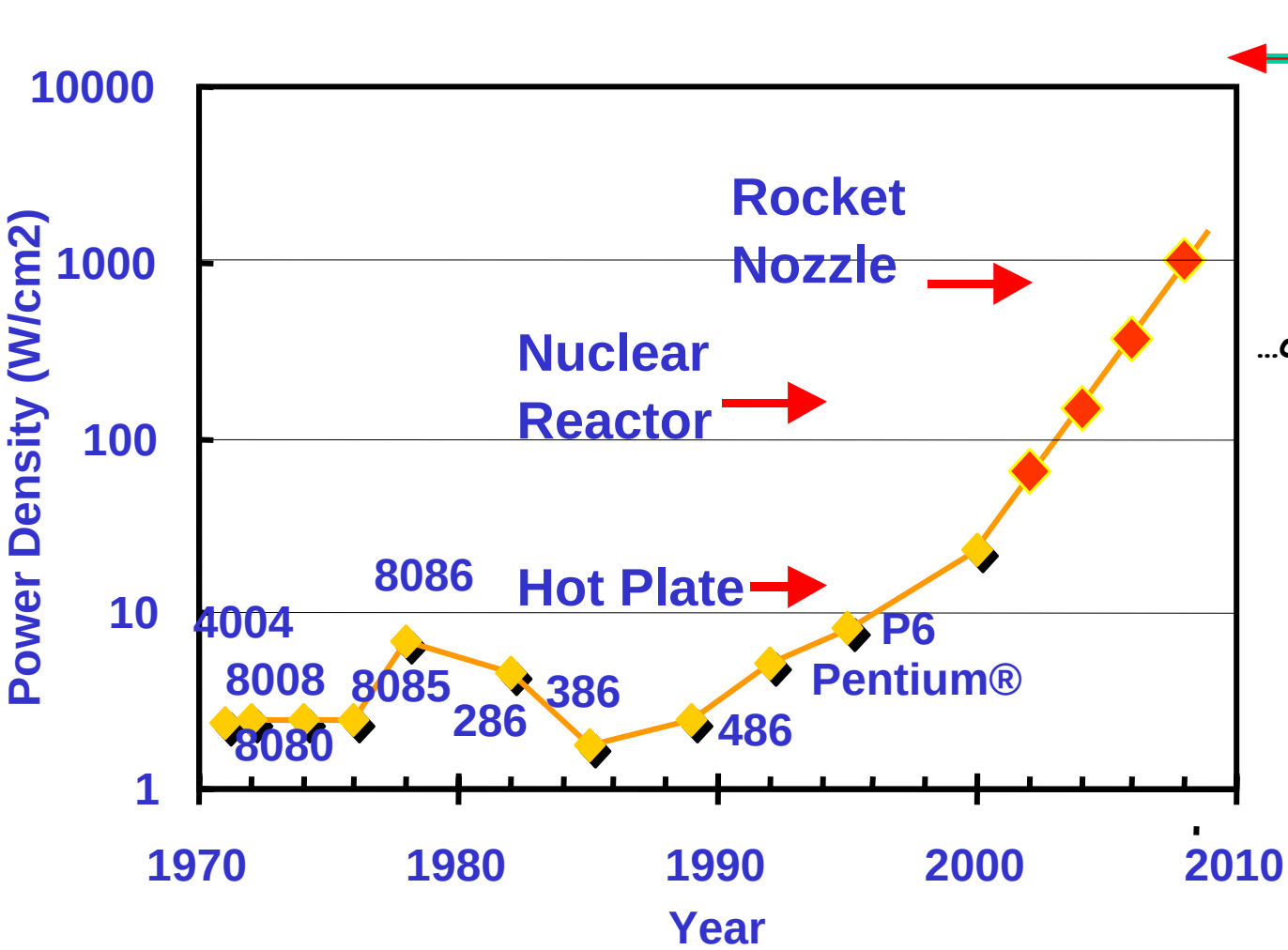
Lead microprocessors power continues to increase



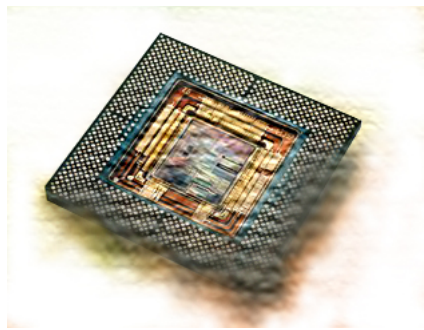
Power delivery and dissipation will be prohibitive

Source: Borkar, De Intel®

Why worry about power? Chip Power Density

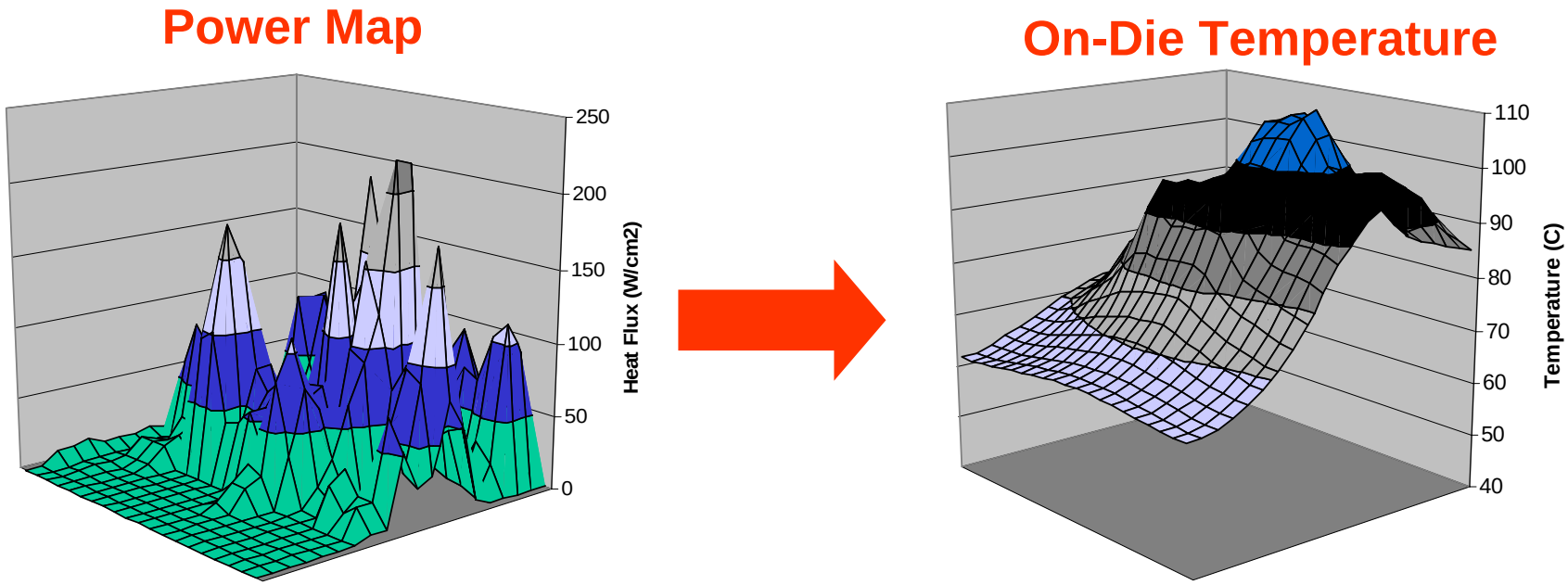


…chips might become hot…



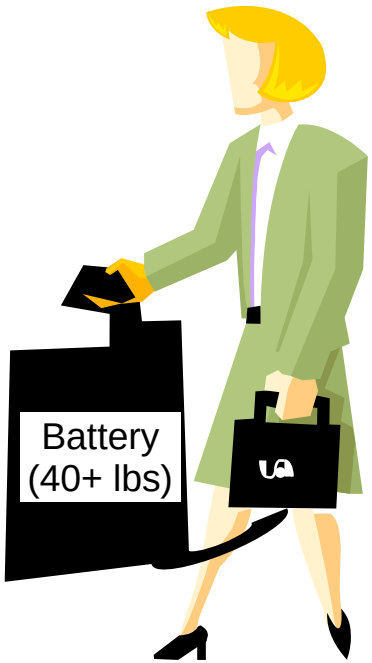
Source: Borkar, De Intel®

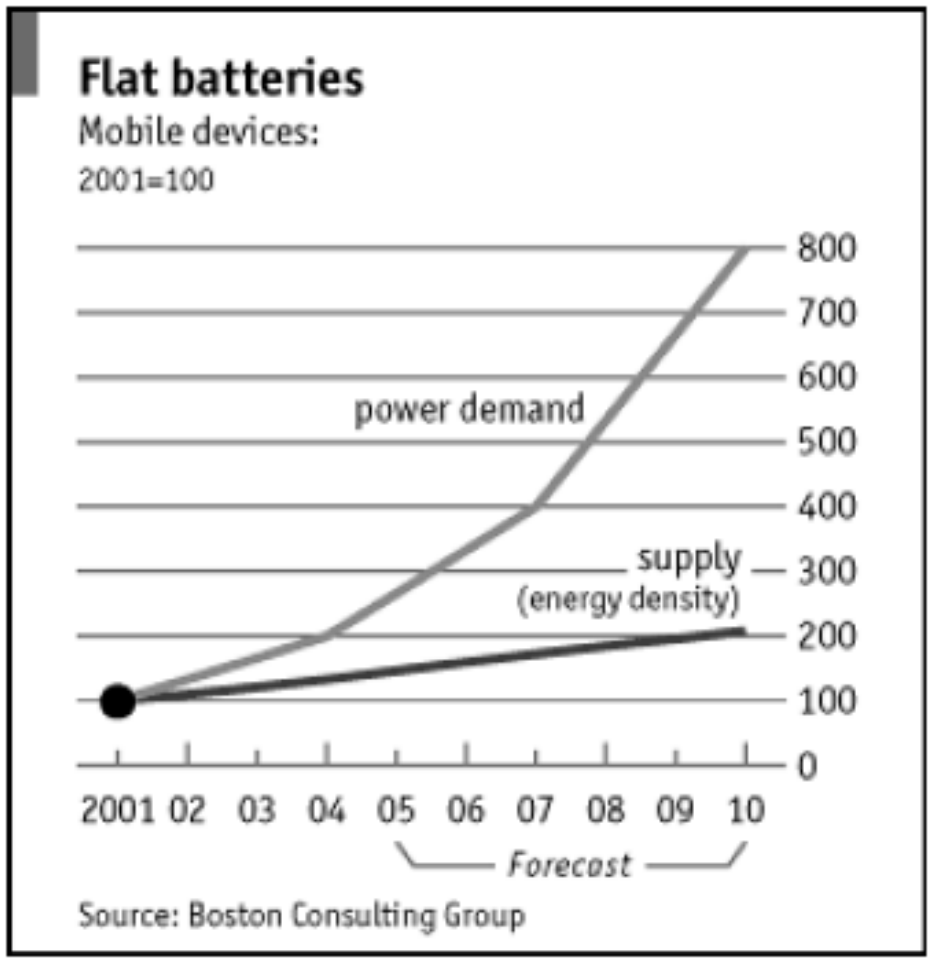
Chip Power Density Distribution



- **Power density is not uniformly distributed across the chip**
- **Silicon not the best thermal conductor (isotopically pure diamond is)**
- **Max junction temperature is determined by hot-spots**
  - Impact on packaging, cooling

Recent Battery Scaling and Future Trends



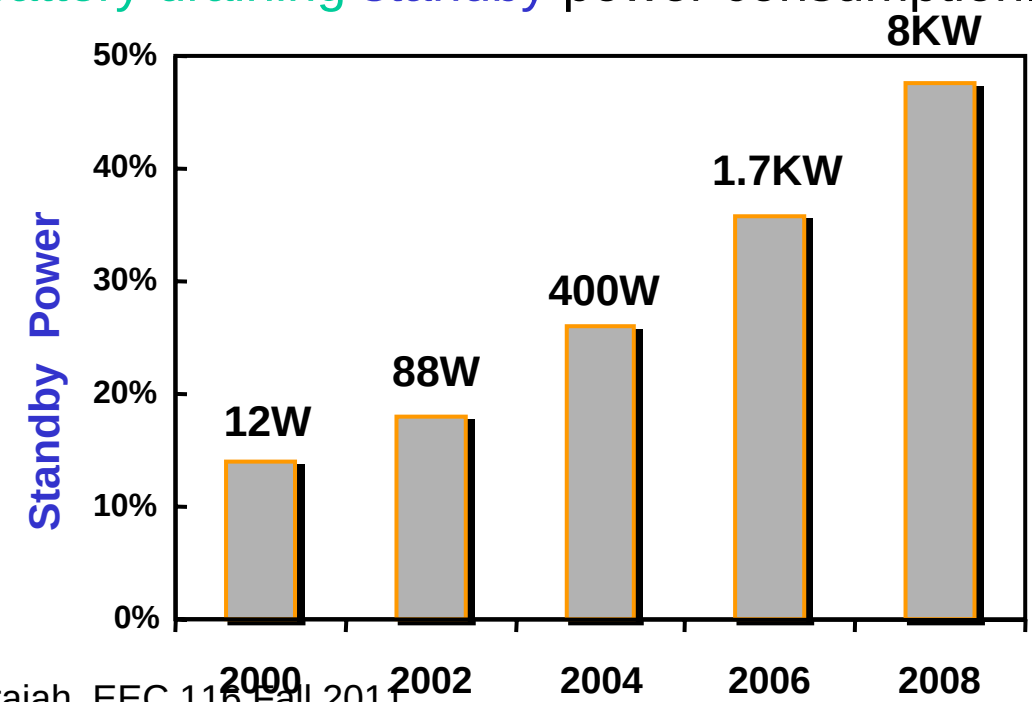


- **Battery energy density increasing 8% per year, demand increasing 24% per year (Economist, January 6, 2005)**

Why worry about power? Standby Power

Year	2002	2005	2008	2011	2014
Power supply V_{dd} (V)	**1.5**	**1.2**	**0.9**	**0.7**	**0.6**
Threshold V_T (V)	**0.4**	**0.4**	**0.35**	**0.3**	**0.25**

- Drain leakage will increase as V_T decreases to maintain noise margins and meet frequency demands, leading to excessive battery draining standby power consumption.

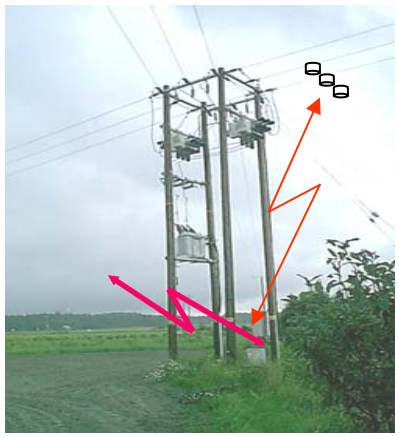


…and phones leaky!

Source: Borkar, De Intel®

Emerging Microsensor Applications

Industrial Plants and Power Line Monitoring (courtesy ABB)

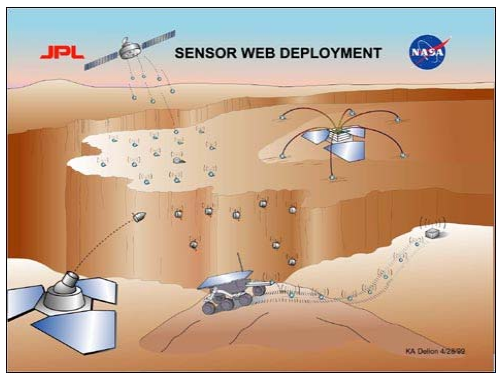


Operating Room of the Future (courtesy John Guttag)

Target Tracking & Detection (Courtesy of ARL)

Location Awareness (Courtesy of Mark Smith, HP)

NASA/JPL *sensorwebs*



Chip Design Styles

- **Field-Programmable Gate Array (FPGA)**
  - Regular structure. Not all transistors are usable.
  - Programmed via software (configurable wiring)
- **Gate Array**
  - Regular structure. Higher usage of transistors than FPGA
  - Two step manufacturing process.
    - Diffusion and poly initially. Design must be fairly stable
    - Metal layers fabricated once design is finalized
- **Cell based design**
  - All transistors used (may have spares to fill in area)
  - Each cell is fixed height so that they can be placed in rows
- **Full Custom**
  - Highest level of compactness and performance
  - Manually intensive. Not conducive to revision (ECO)

Logic Design Families

- **Static CMOS Logic**
  - Good power delay product (energy)
  - Good noise margin
  - Not as fast as dynamic
- **Dynamic Logic**
  - Very fast but inefficient in use of power
  - Domino, CPL, OPL
- **Pass Transistor Logic**
  - Poor noise margin
  - Sometimes static power dissipation
  - Less area than static CMOS

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  - Less area than static CMOS

Design Parameters

- **Reliability (Dealt with when relating to layout)**
  - Factors that dictate reliable operation of the circuit
    - Electromigration, thermal issues, hot electrons, noise margins
- **Performance (Not dealt with in this class)**
  - Not just measured in clock speed. Power-Delay Product (PDP, equivalent to energy) is a better measure
- **Area**
  - Directly affects cost

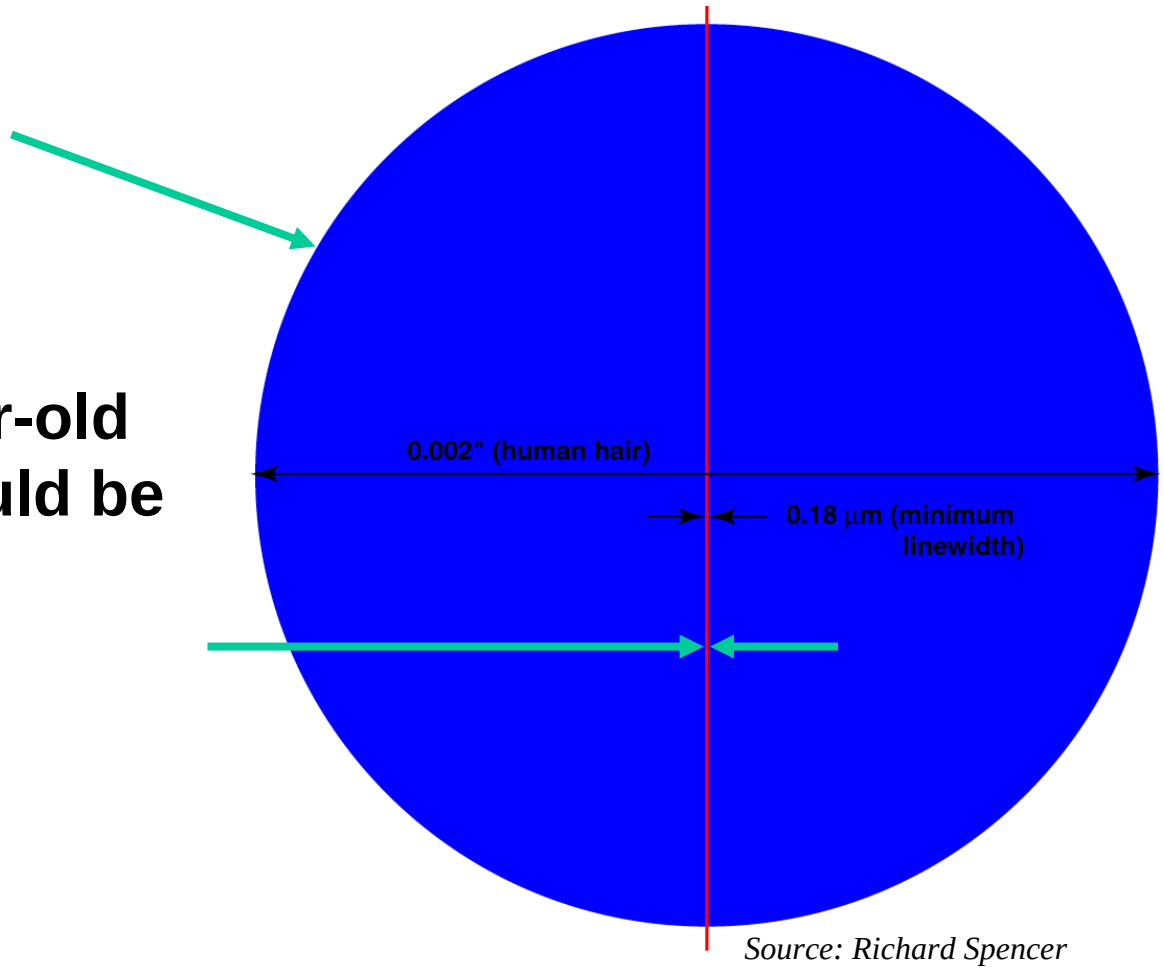
Current State of the Art

- **Intel Core® @ 4 GHz (1 or 2 cores/chip going to 4+)**
  - 800 - 1066 MHz system bus
  - AGP 8x graphics (533 MHz bus)
  - Memory bus at 533 MHz (DDR)
- **Complex Designs demand resources**
  - Design teams resource limited due to logistics and cost
  - Cannot afford to miss issues due to cost of product recall
  - Emphasis on pre-silicon verification as opposed to post silicon testing

How Large Are Transistors?

- **If a human hair were this large…**

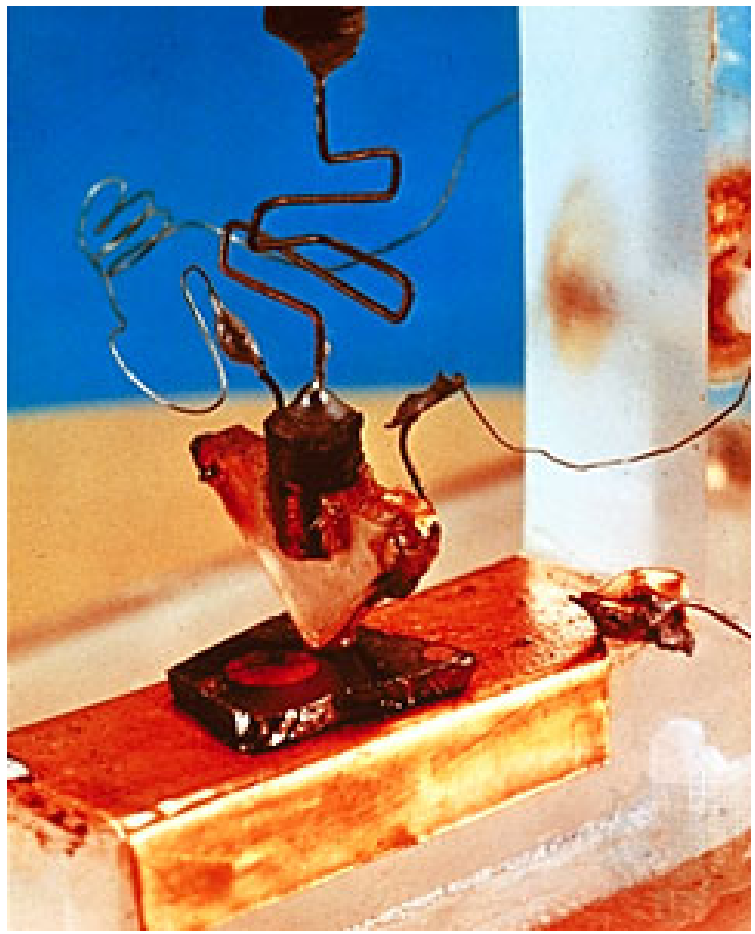
A several-year-old transistor would be this long…



Source: Richard Spencer

The First Transistor

- **Fabricated at Bell Labs on December 16, 1947. The inventors won the Nobel prize in physics in 1956 for the invention.**



Source: Richard Spencer

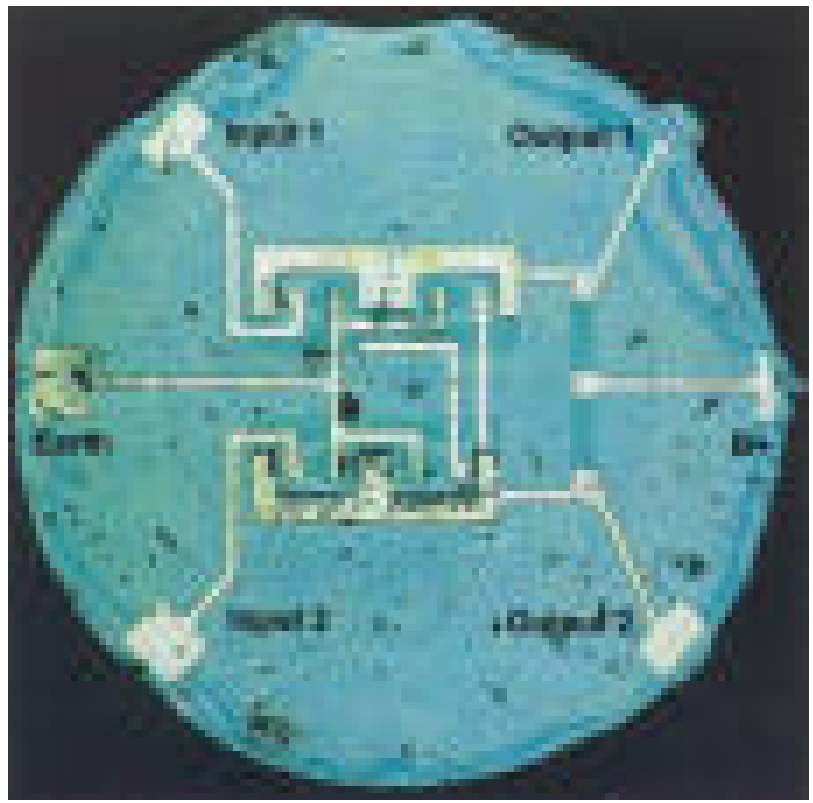
The First Integrated Circuit

- **This is the first IC made by Jack Kilby of Texas Instruments. It was built in 1958.**

Source: Richard Spencer

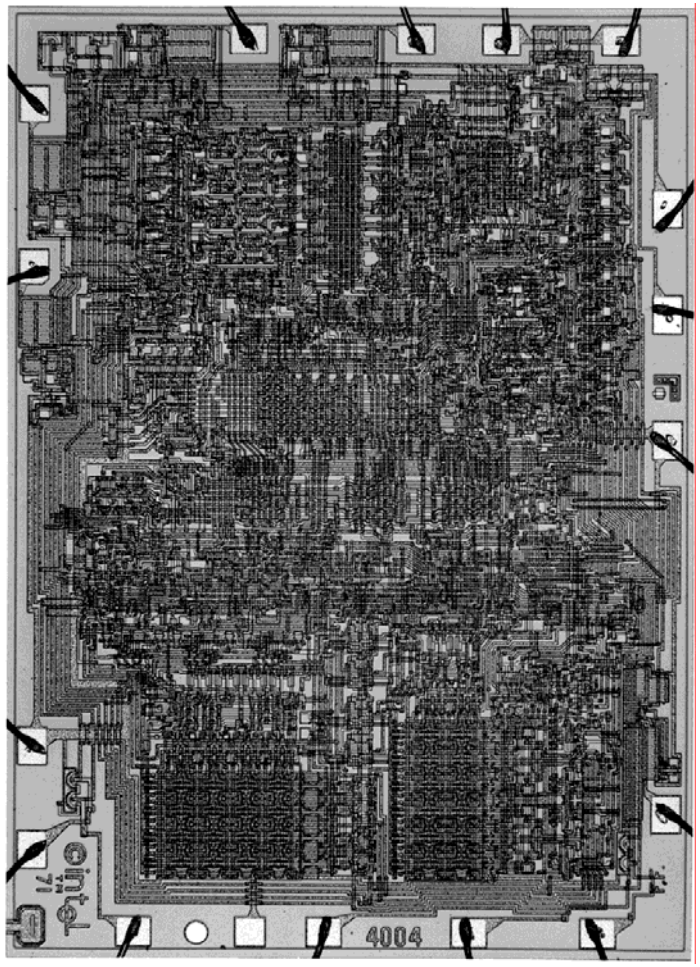
An Early “Planar” IC

- **This is an early planar IC from Fairchild.**



Source: Richard Spencer

Intel 4004 Micro-Processor

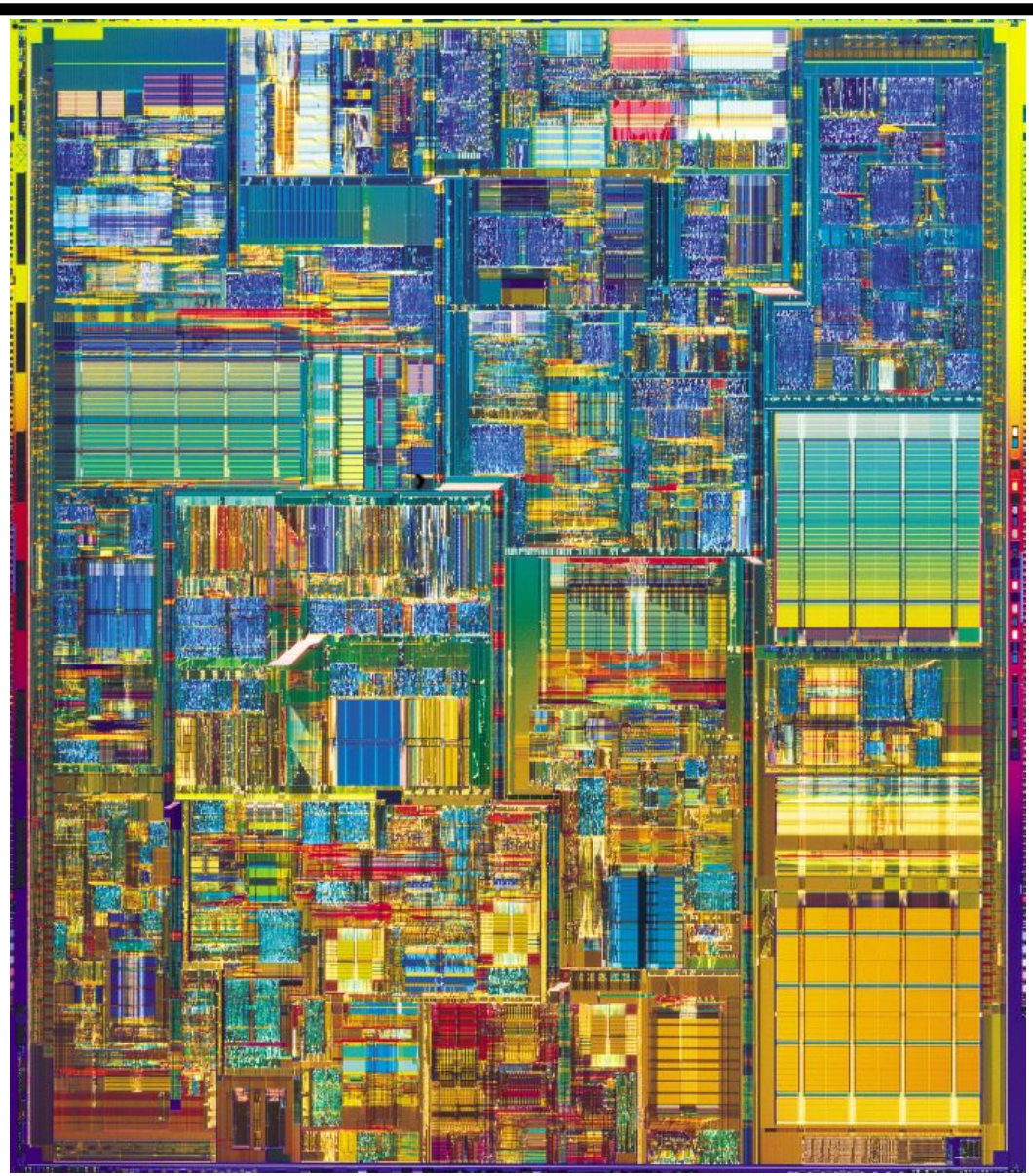


1971
1000 transistors
1 MHz operation

Source: Digital Integrated Circuits, 2nd ©

Intel Pentium 4 Microprocessor

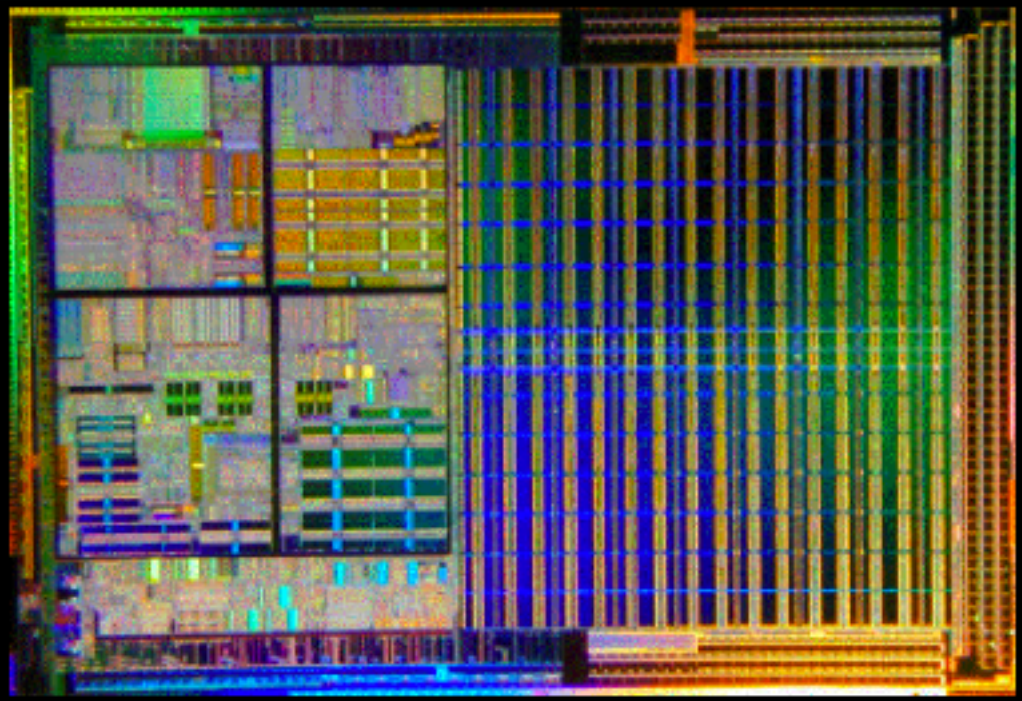
- **Introduced in 2000**
  - 42 million transistors
  - 0.18 µm CMOS



Source: Intel
http://www.intel.com/museum/online/hist_micro/hof/

Product Application: AMD's Opteron X86-64

Modern Microprocessor (> 100,000,000 transistors) 2003



One centimeter

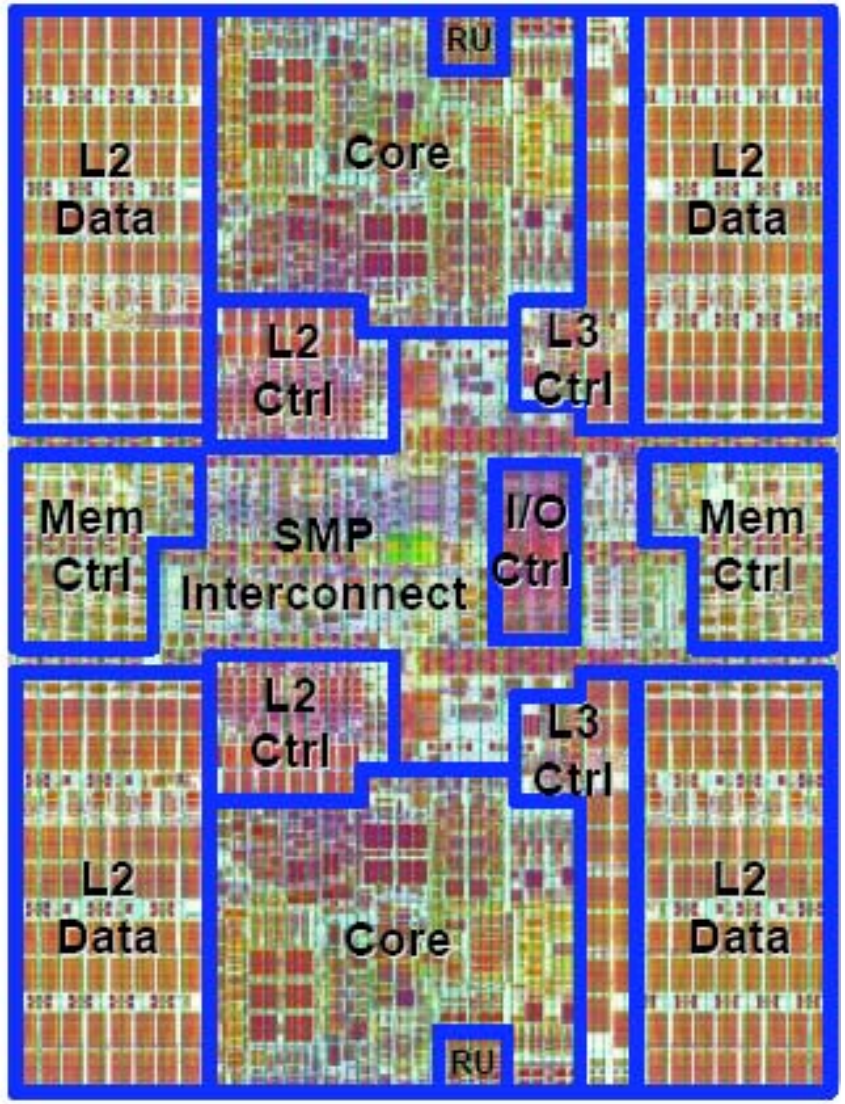
- 8th generation processor (SledgeHammer) w/ 1MB L2 Cache
- Working on 1st (SOI) silicon; > 100 million transistors
- ~180mm² on 130nm technology with Cu metallization and low k

IBM POWER6

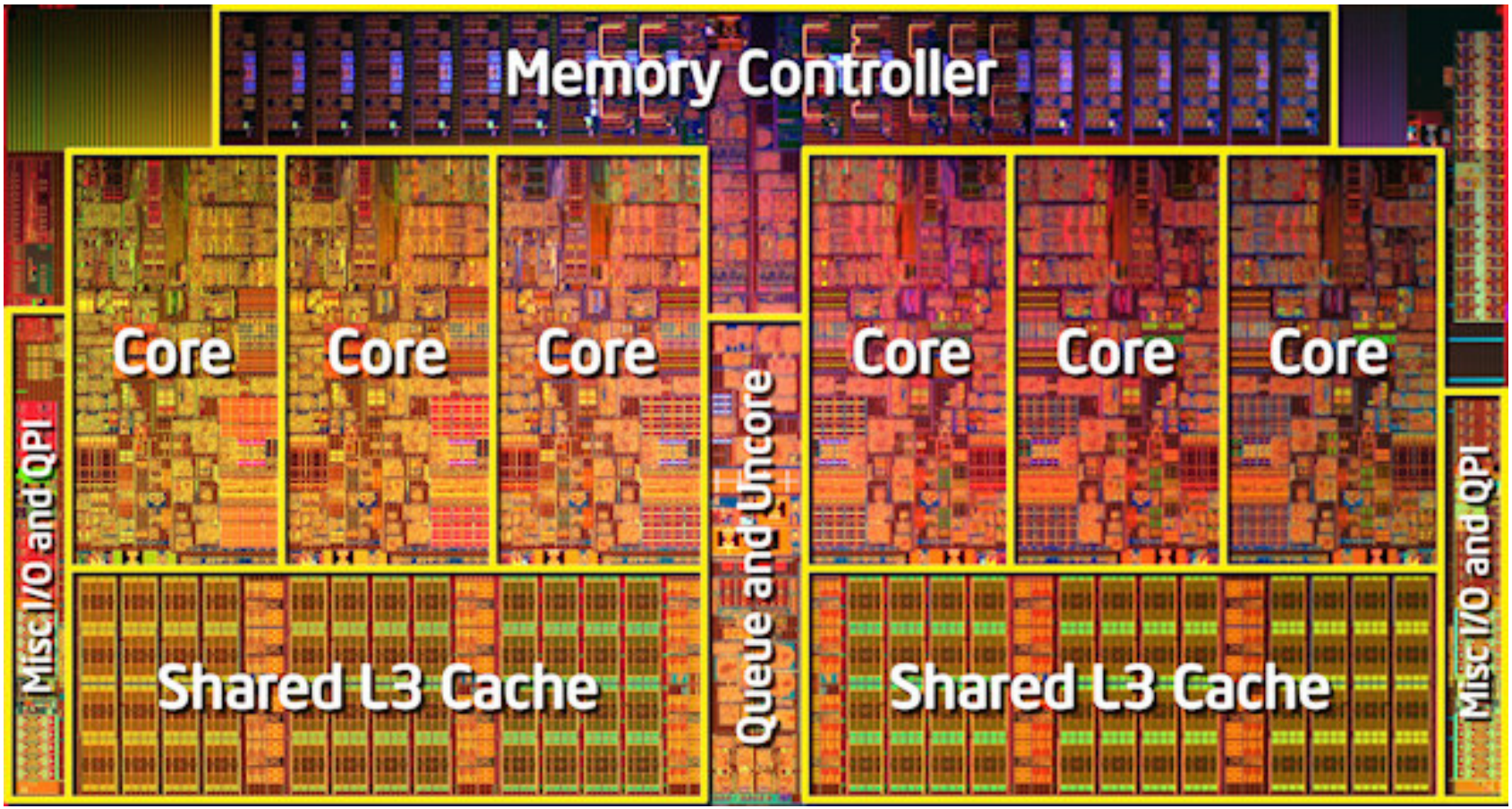
- Ultra-high frequency dual-core chip
  - 7-way superscalar, 2-way SMT core
  - 9 execution units
    - 2LS, 2FP, 2FX, 1BR, 1VMX,1DFU
  - 790M transistors
  - Up to 64-core SMP systems
  - 2x4MB on-chip L2
  - 32MB On-chip L3 directory and controller
  - Two memory controllers on-chip
  - Recovery Unit
- Technology
  - CMOS 65nm lithography, SOI
- High-speed elastic bus interface at 2:1 freq
  - I/Os: 1953 signal, 5399 Power/Gnd

Reick et al., Hot Chips 19, 2007

Modern Multicore Microprocessor (790,000,000 transistors) 2007



Intel Westmere 6-Core Microprocessor



- **Introduced in 2010**
  - 1.17 billion transistors, 32 nm CMOS

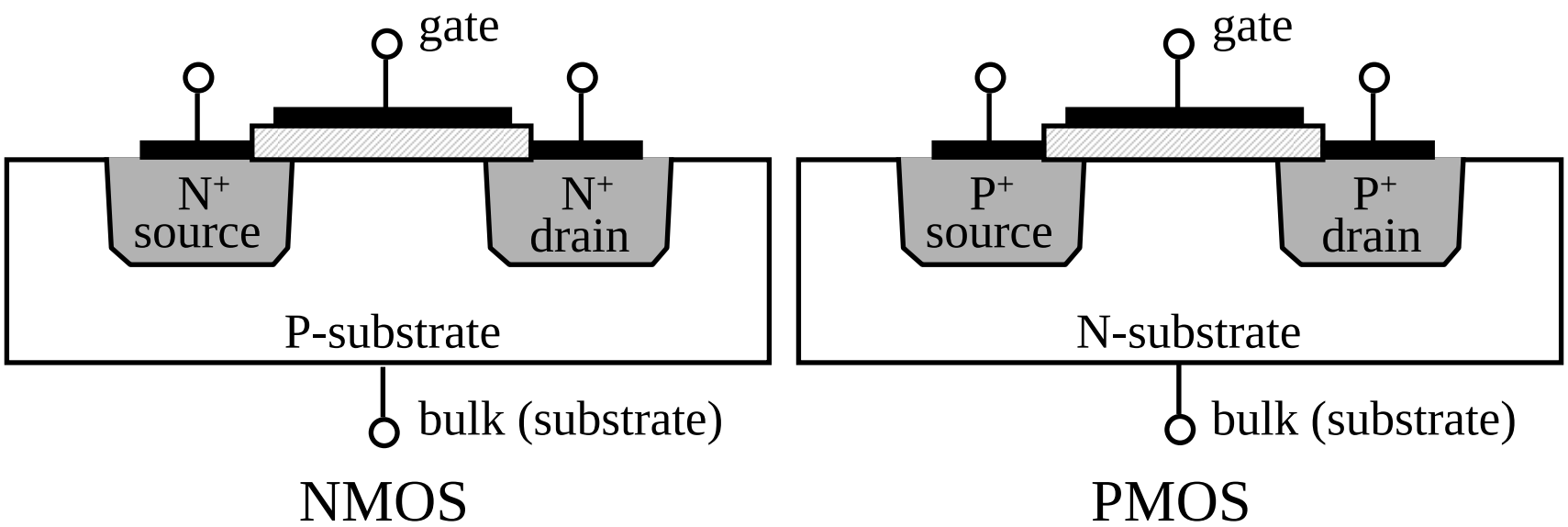
Source: Intel

Expectations

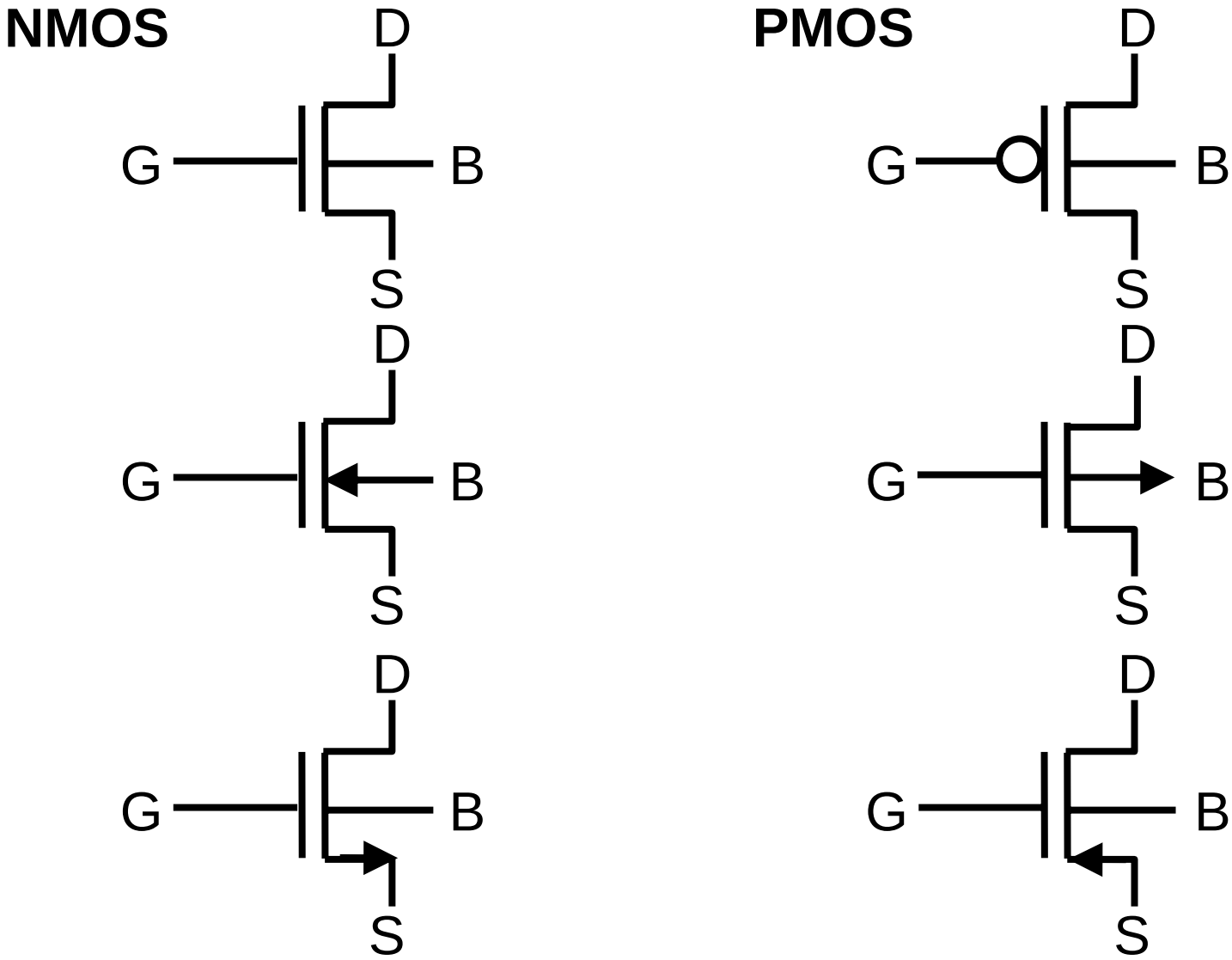
- **You should already know**
  - Solid State – (i.e. PN junctions, semiconductor physics, ..)
- **What we will cover**
  - MOS Transistors Fabrication and Equations
  - CMOS logic at the transistor and physical level
  - Sequential logic
  - Memory
  - Arithmetic Circuits
  - Interconnect
  - Design Styles
- **Framework**
  - Course to use PowerPoint for the most part
  - Bring PowerPoint slides to class and write notes on them

MOS Transistor Types

- **Rabaey Ch. 3 (Kang & Leblebici Ch. 3)**
- **Two transistor types (analogous to bipolar NPN, PNP)**
  - NMOS: p-type substrate, n^+ source/drain, electrons are charge carriers
  - PMOS: n-type substrate, p^+ source/drain, holes are charge carriers

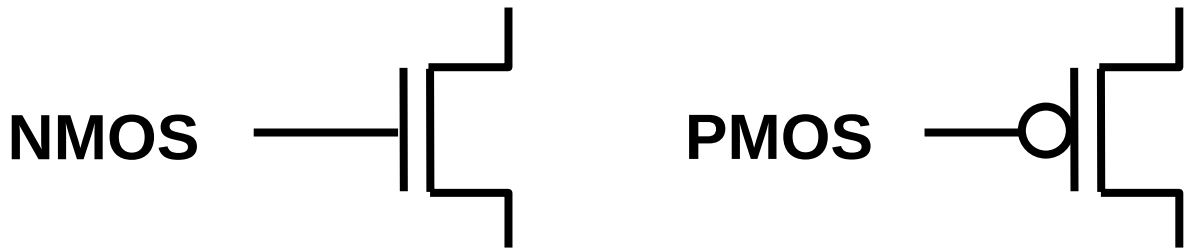


MOS Transistor Symbols



Note on MOS Transistor Symbols

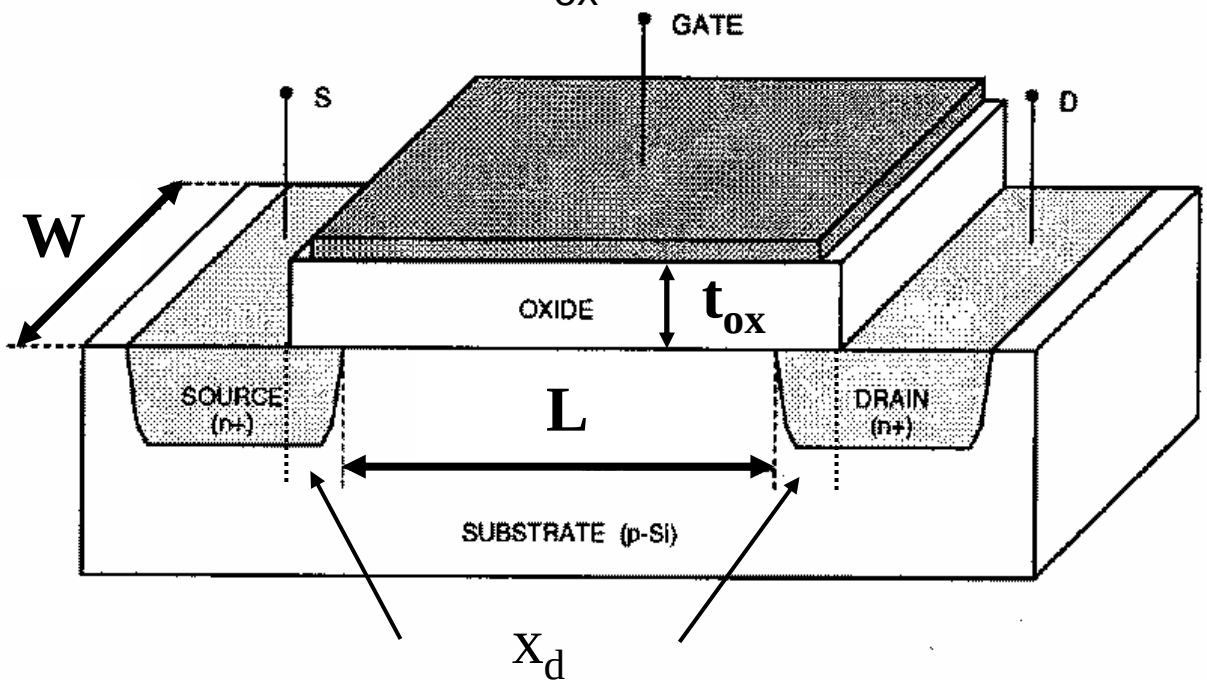
- **All symbols appear in literature**
  - Symbols with arrows are conventional in analog papers
  - PMOS with a bubble on the gate is conventional in digital circuits papers
- **Sometimes bulk terminal is ignored – implicitly connected to supply:**



- **Unlike physical bipolar devices, source and drain are usually symmetric**

MOS Transistor Structure

- **Important transistor physical characteristics**
  - Channel length $L = L_D - 2x_d$ (K&L $L = Lgate - 2L_D$)
  - Channel width W
  - Thickness of oxide t_{ox}



MOS Transistor Regions of Operation

- **Three main regions of operation**
- **<u>Cutoff</u>: $V_{GS} < V_T$**
  No inversion layer formed, drain and source are isolated by depleted channel. $I_{DS} \approx 0$
- **<u>Linear (Triode, Ohmic)</u>: $V_{GS} > V_T$, $V_{DS} < V_{GS}-V_T$**
  Inversion layer connects drain and source. Current is almost linear with V_{DS} (like a resistor)
- **<u>Saturation</u>: $V_{GS} > V_T$, $V_{DS} \geq V_{GS}-V_T$**
  Channel is "pinched-off". Current saturates (becomes independent of V_{DS}, to first order).

MOSFET Drain Current Overview

Saturation: $$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_T\right)^2\left(1 + \lambda V_{DS}\right)$$

Linear (Triode, Ohmic):

$$I_D = \mu C_{ox}\frac{W}{L}\left(\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

Cutoff: $$I_D \approx 0$$

"Classical" MOSFET model, will discuss deep submicron modifications as necessary (Rabaey, Eqs. 3.25, 3.29)

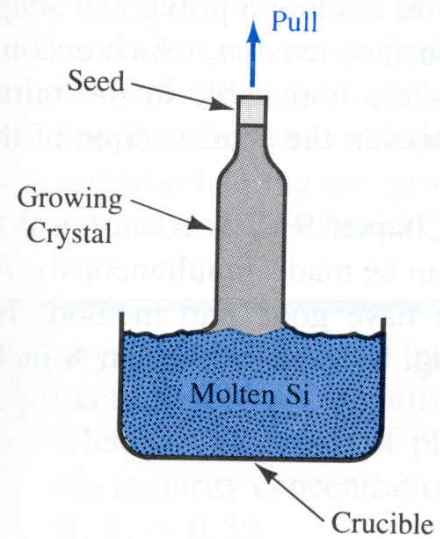
Logic Gate Examples

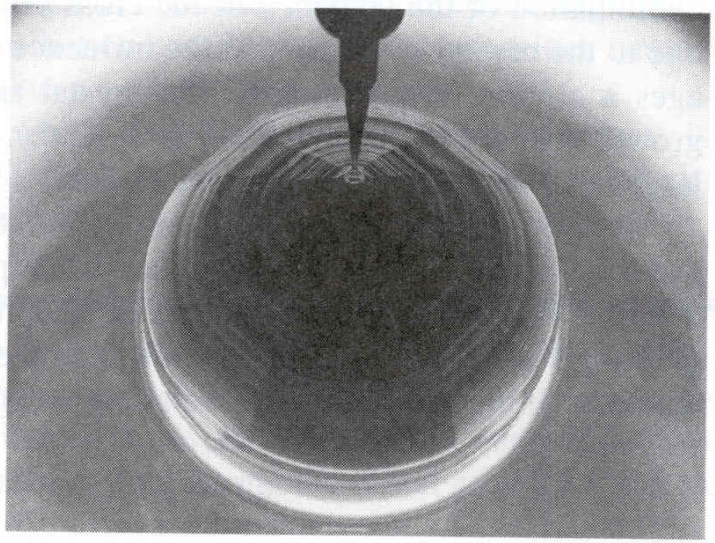
- **CMOS Inverter**
- **Two Input NAND**
- **Two Input NOR**

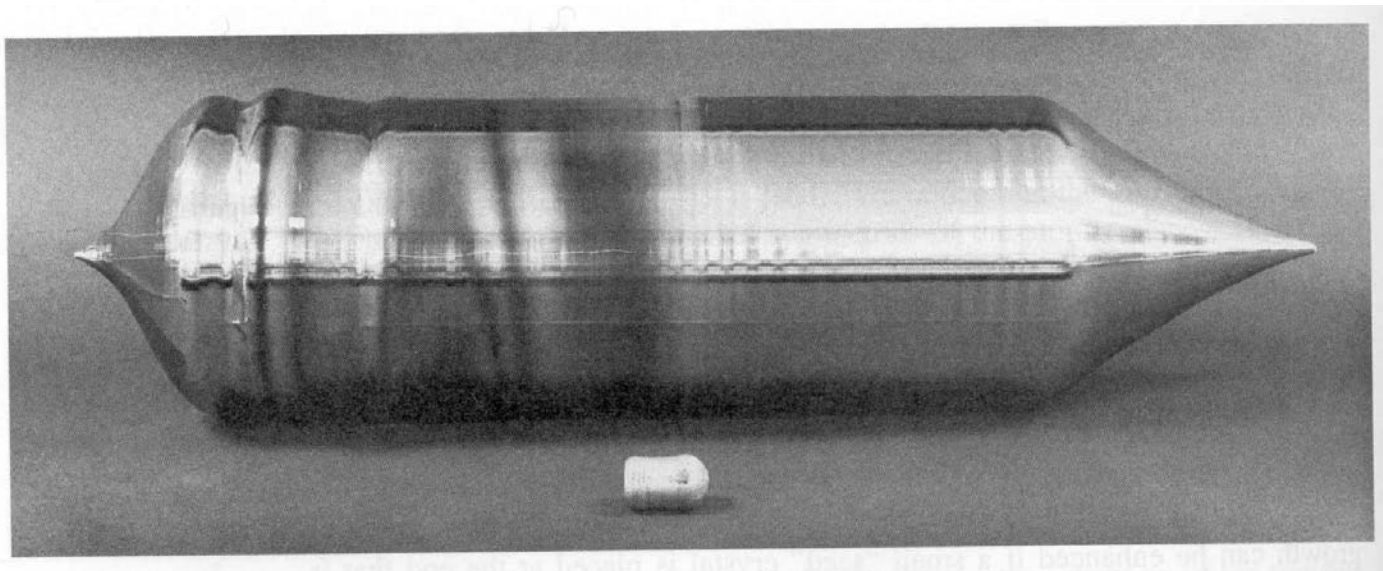
Fabrication Process

- **Substrate is grown and then cut**
  - Round silicon wafers are used
  - Purity emphasized to prevent impurities from affecting operation (99.9999% pure)
- **Each layer deposited separately**
- **Some layers used as masks for later layers**
- **Planar process is important**
  - Requires minimum percent usage of metal to ensure flatness

Silicon Substrate Manufacturing







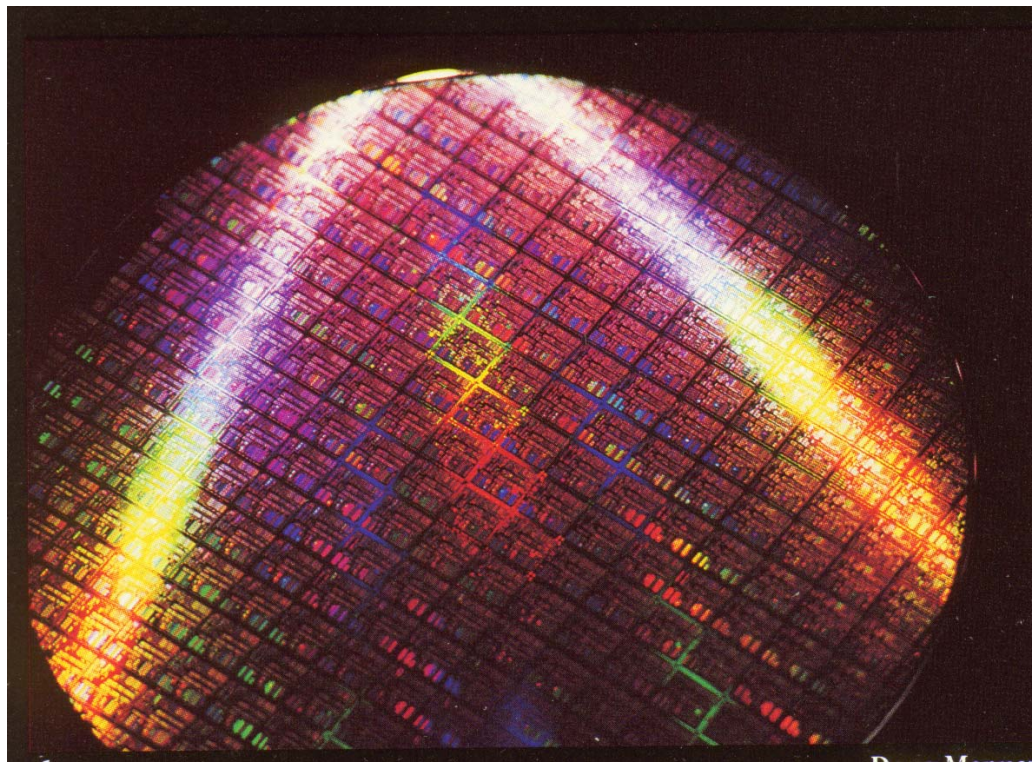
Silicon

- **Silicon is the second most common element in the Earth's crust.**
- **Semiconductor-grade Si is 99.999999 % pure.**
- **Ingots like this one weigh several hundred pounds and cost $16,000**
- **The ingot will be sliced into very thin wafers.**

Source: Richard Spencer

A Silicon Wafer

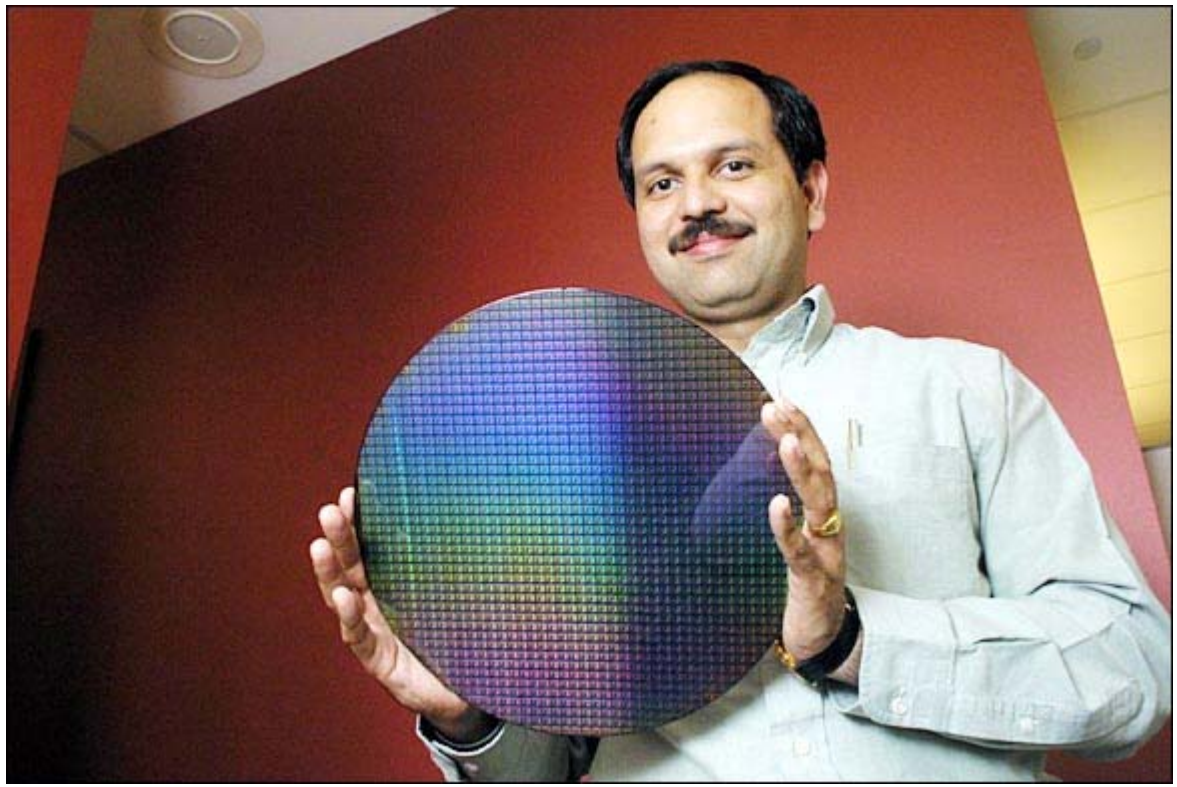
- **This 8-inch wafer contains about 200 Pentium II chips (1997).**
- **Each chip contains more than 20 million transistors.**
- **More than 1 billion microprocessors are made each year.**



Source: Richard Spencer

A State-of-the-art Wafer

- **300 mm diameter wafer**

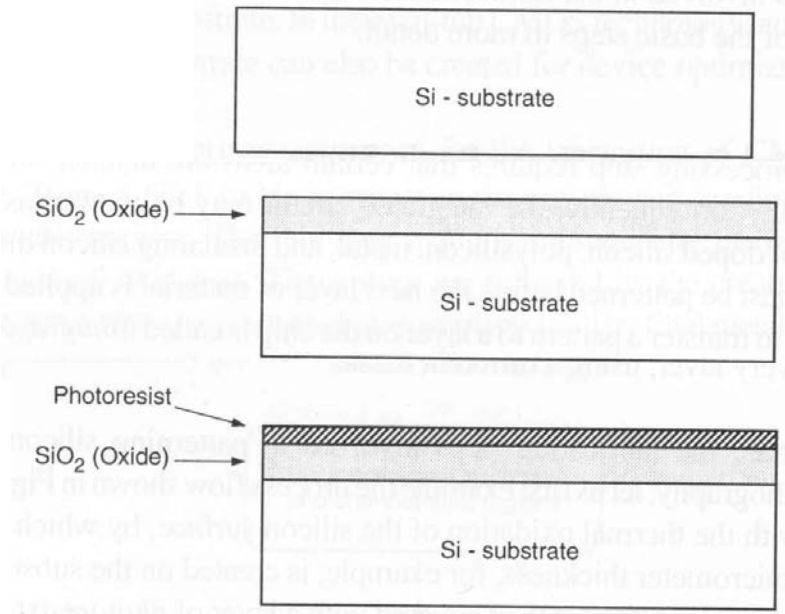


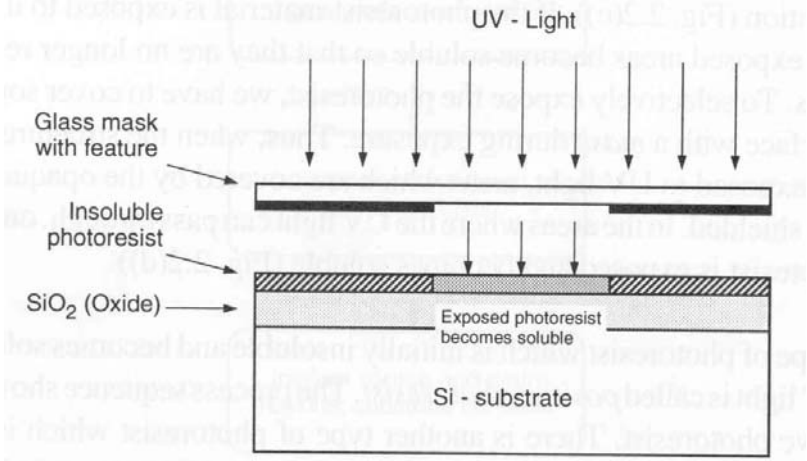
Source: IBM

Building a Golf Course with Similar Process

- **Plane drops materials from the air**
  - Sand, then dirt, then grass seeds, then trees
  - Certain masks applied during process to prevent material from hitting particular areas
  - For instance: After Sand, mask placed over areas where sand trap will exist. Mask later taken off at end of process to reveal sand trap.

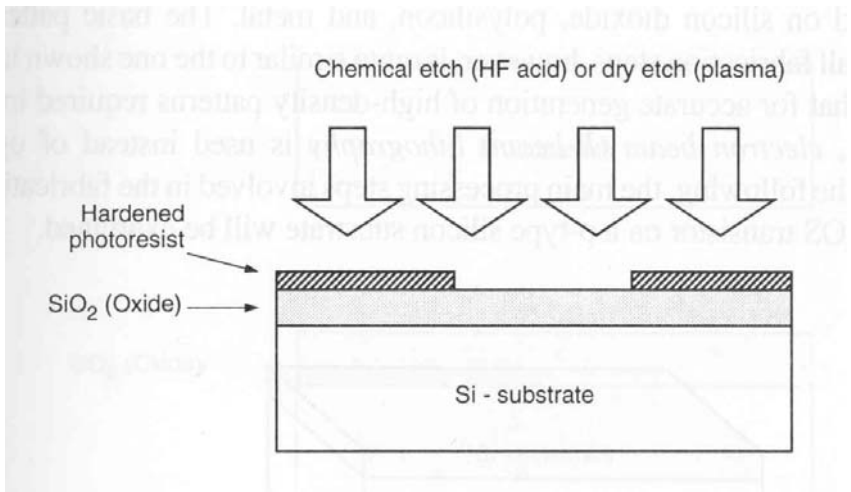
Fabrication: Patterning of SiO_2 Step I

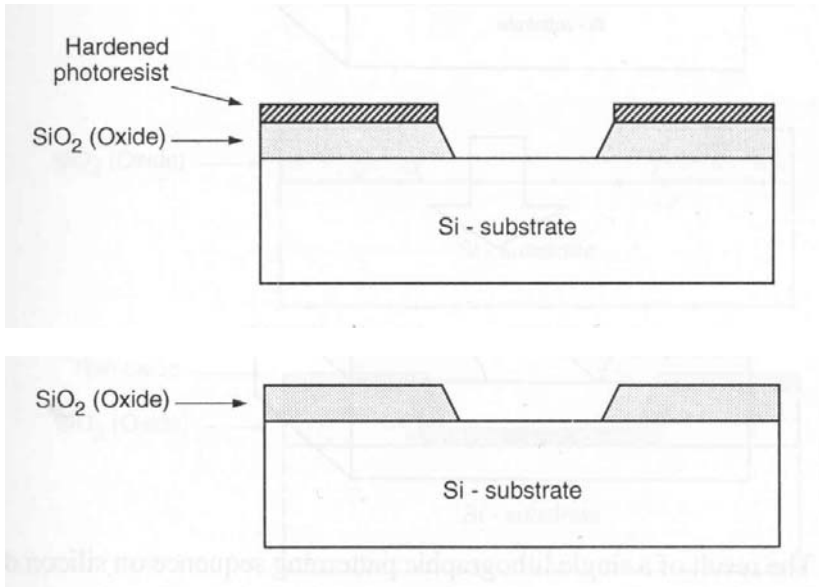




- **Grow SiO_2 on Si by exposing to O_2**
  - High temperature accelerates this process
- **Cover surface with photoresist (PR)**
  - Sensitive to UV light (wavelength determines feature size)
  - Positive PR becomes soluble after exposure
  - Negative PR becomes insoluble after exposure

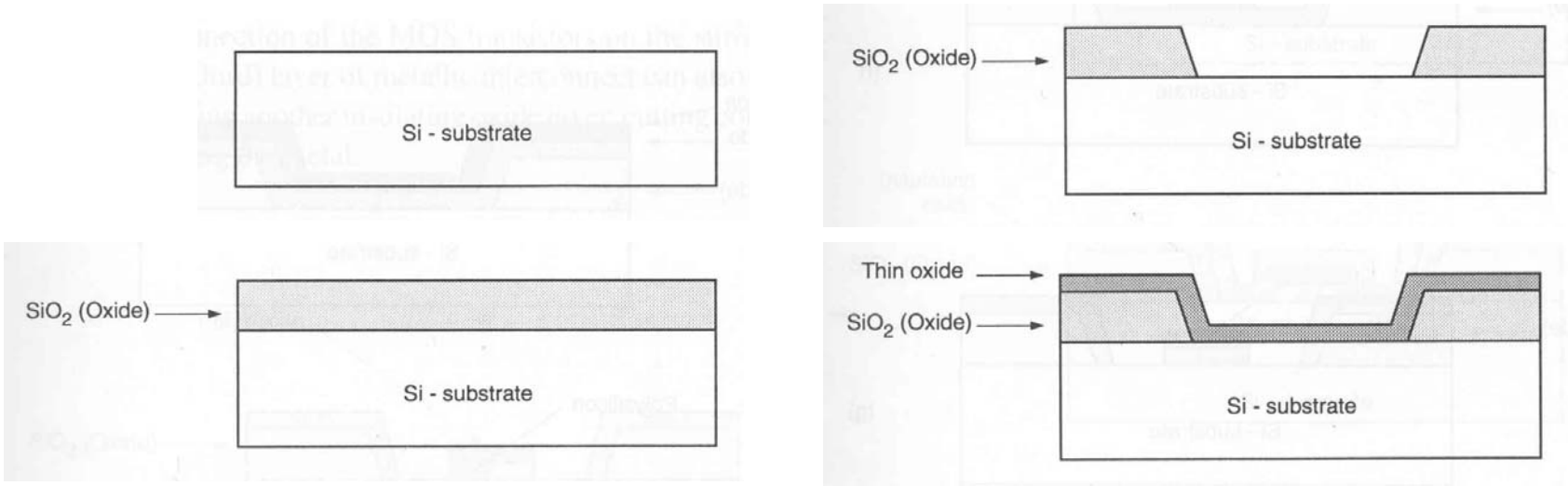
Fabrication: Patterning of SiO_2 Step II





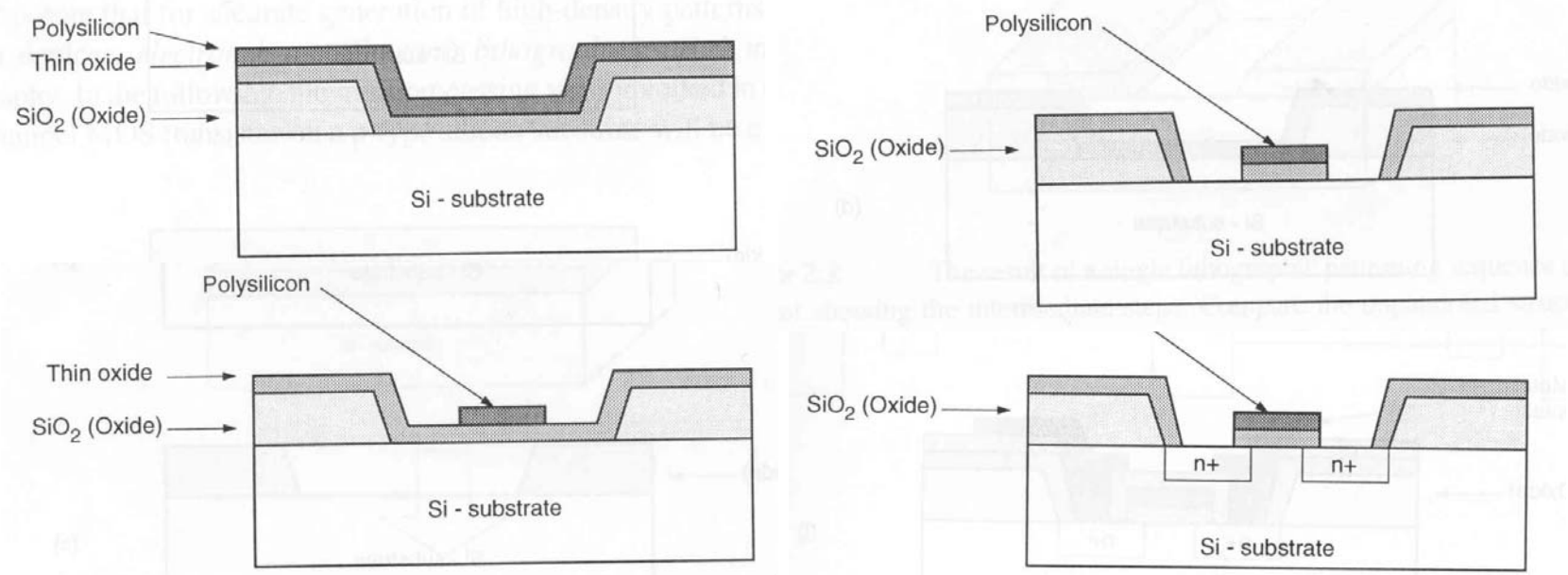
- **Exposed PR removed with a solvent**
- **SiO_2 removed by etching (HF – hydrofluoric acid)**
- **Remaining PR removed with another solvent**

NMOS Transistor Fabrication



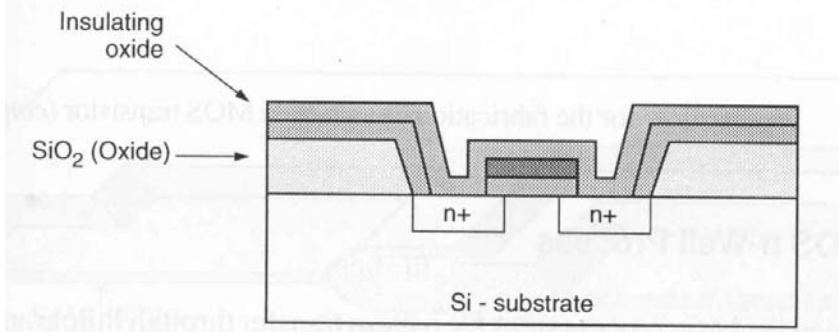
- **Thick field oxide grown**
- **Field oxide etched to create area for transistor**
- **Gate oxide (high quality) grown**

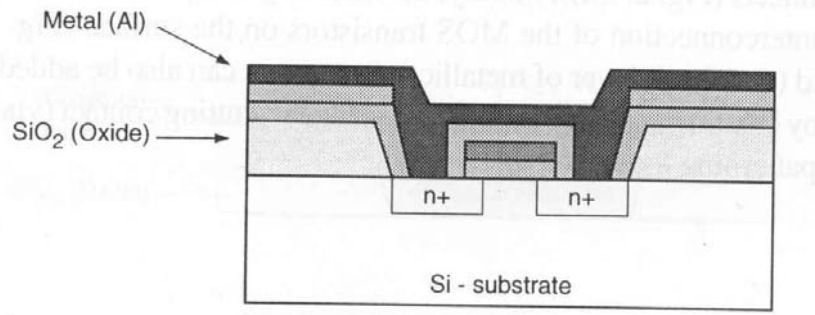
NMOS Transistor Fabrication

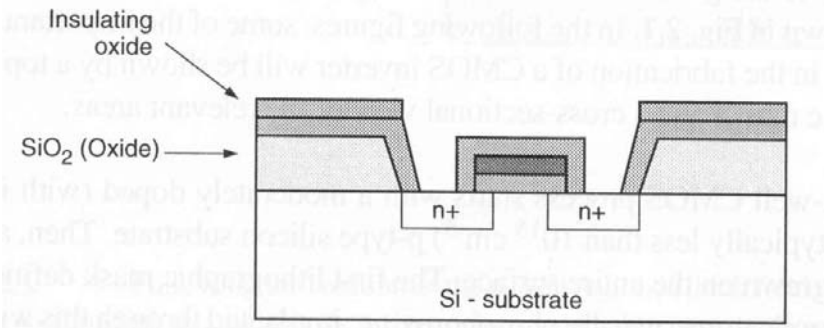


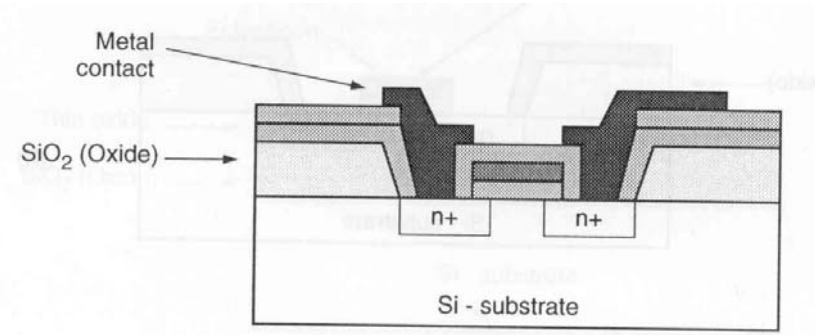
- **Polysilicon deposited (doped to reduce resistance R)**
- **Polysilicon etched to form gate**
- **Gate oxide etched from source and drain**
  - Self-aligned process because source/drain aligned by gate
- **Si doped with donors to create n+ regions**

NMOS Transistor Fabrication



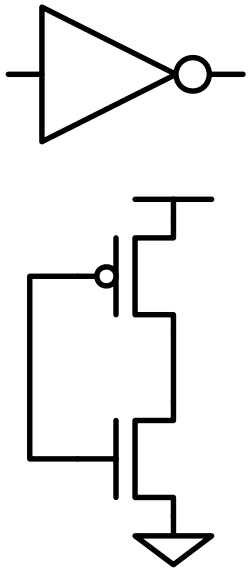


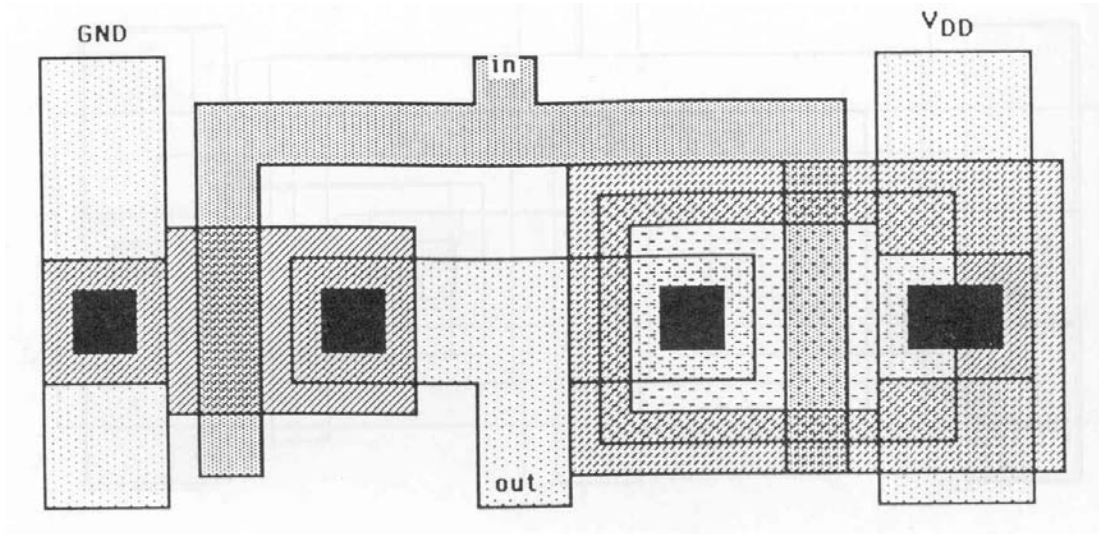




- **Insulating SiO_2 grown to cover surface/gate**
- **Source/Drain regions opened**
- **Aluminum evaporated to cover surface**
- **Aluminum etched to form metal1 interconnects**

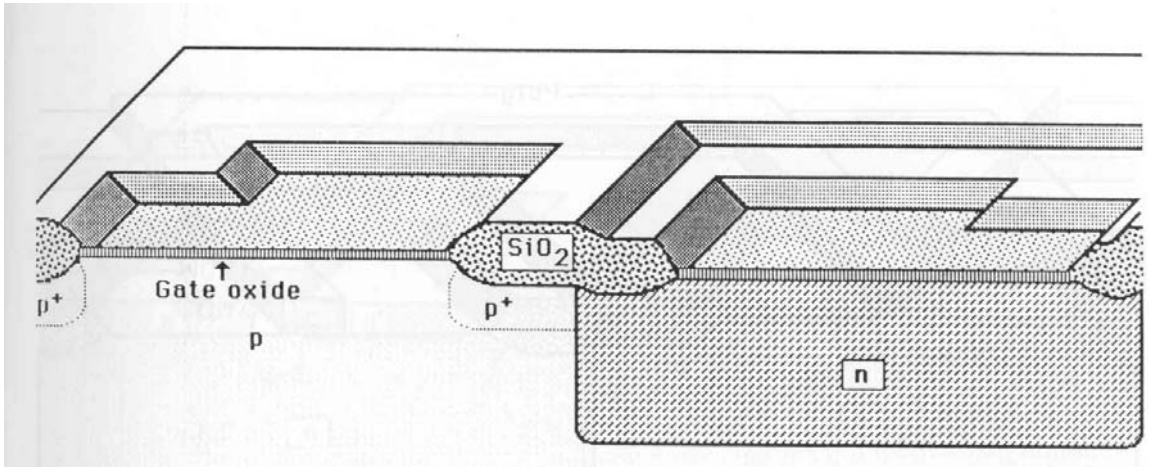
Inverter Fabrication: Layout





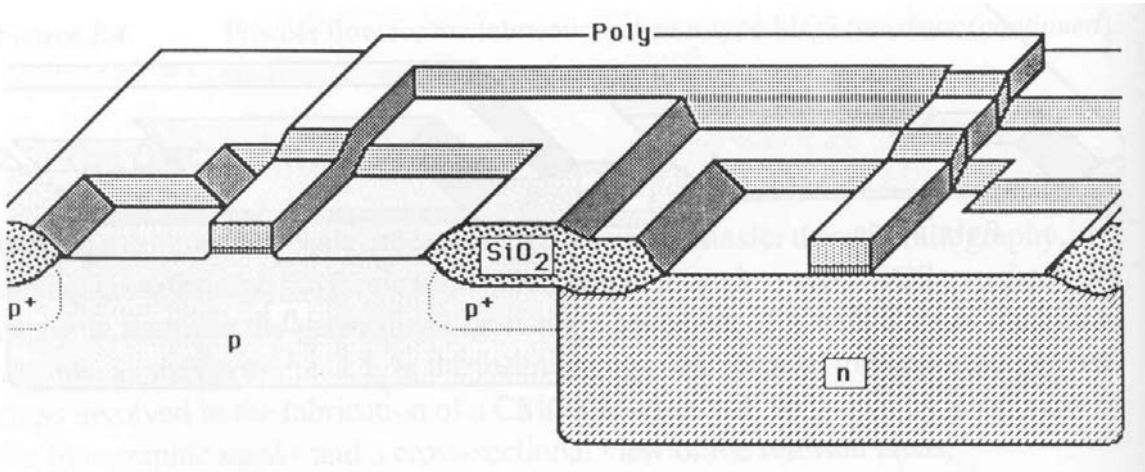
- **Inverter**
  - Logic symbol
  - CMOS inverter circuit
  - CMOS inverter layout (top view of lithographic masks)

Inverter Fabrication: NWELL and Oxides



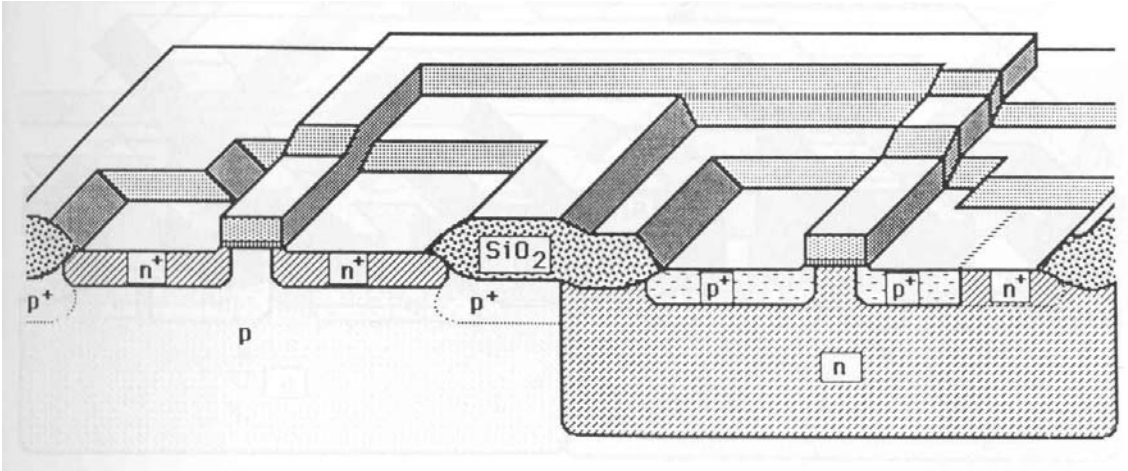
- **N-wells created**
- **Thick field oxide grown surrounding active regions**
- **Thin gate oxide grown over active regions**

Inverter Fabrication: Polysilicon



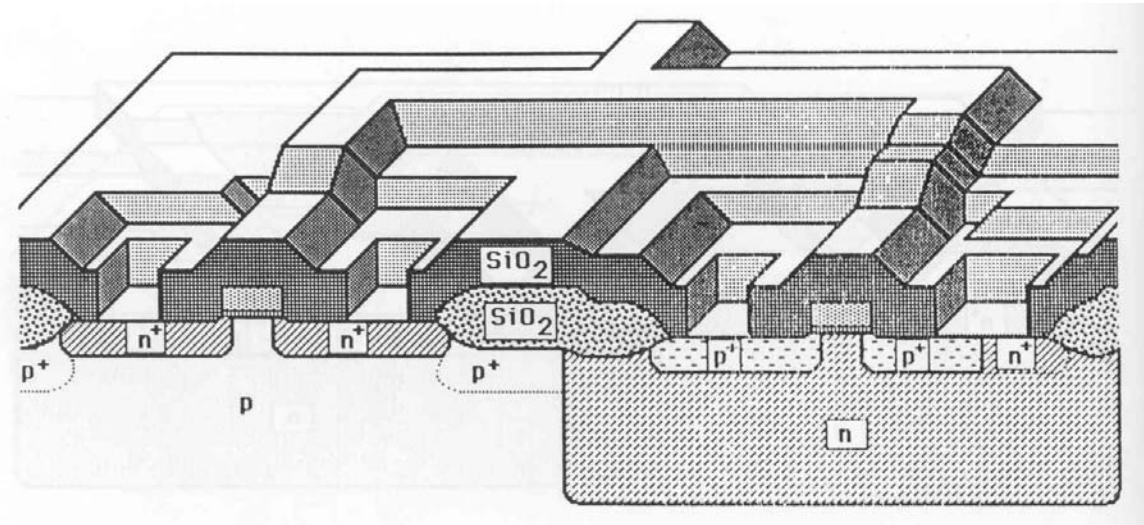
- **Polysilicon deposited**
  - Chemical vapor deposition (Places the Poly)
  - Dry plasma etch (Removes unwanted Poly)

Inverter Fabrication: Diffusions



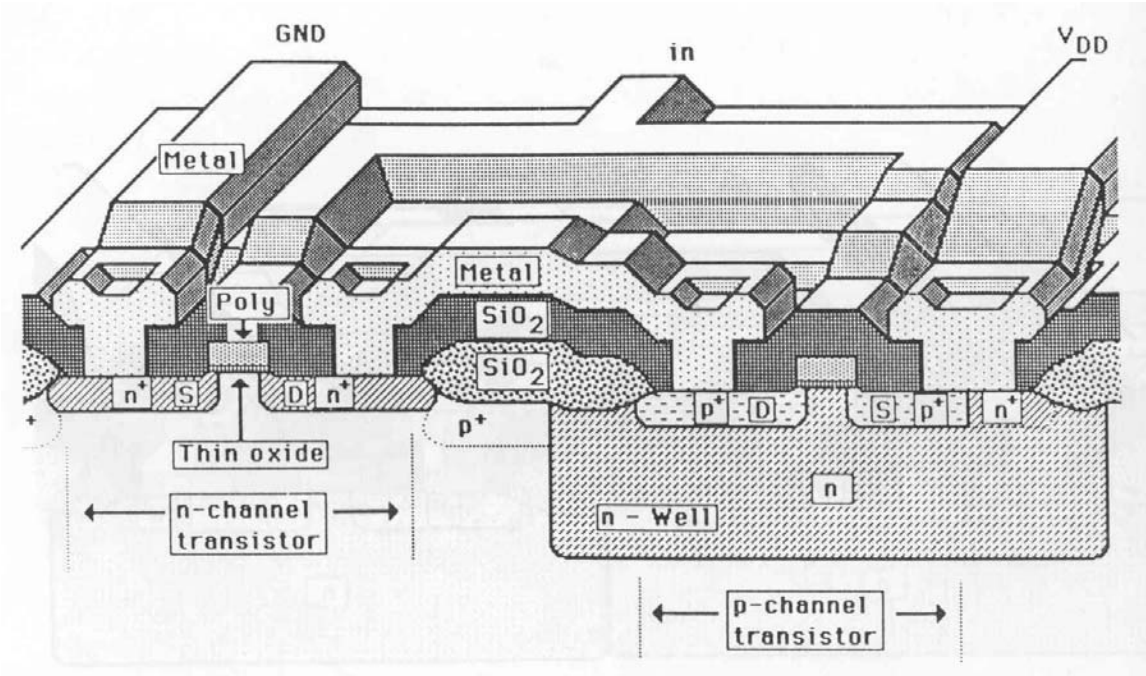
- **N+ and P+ regions created using two masks**
  - Source/Drain regions
  - Self-aligned process since gate is already fabricated
  - Substrate contacts

Inverter Fabrication



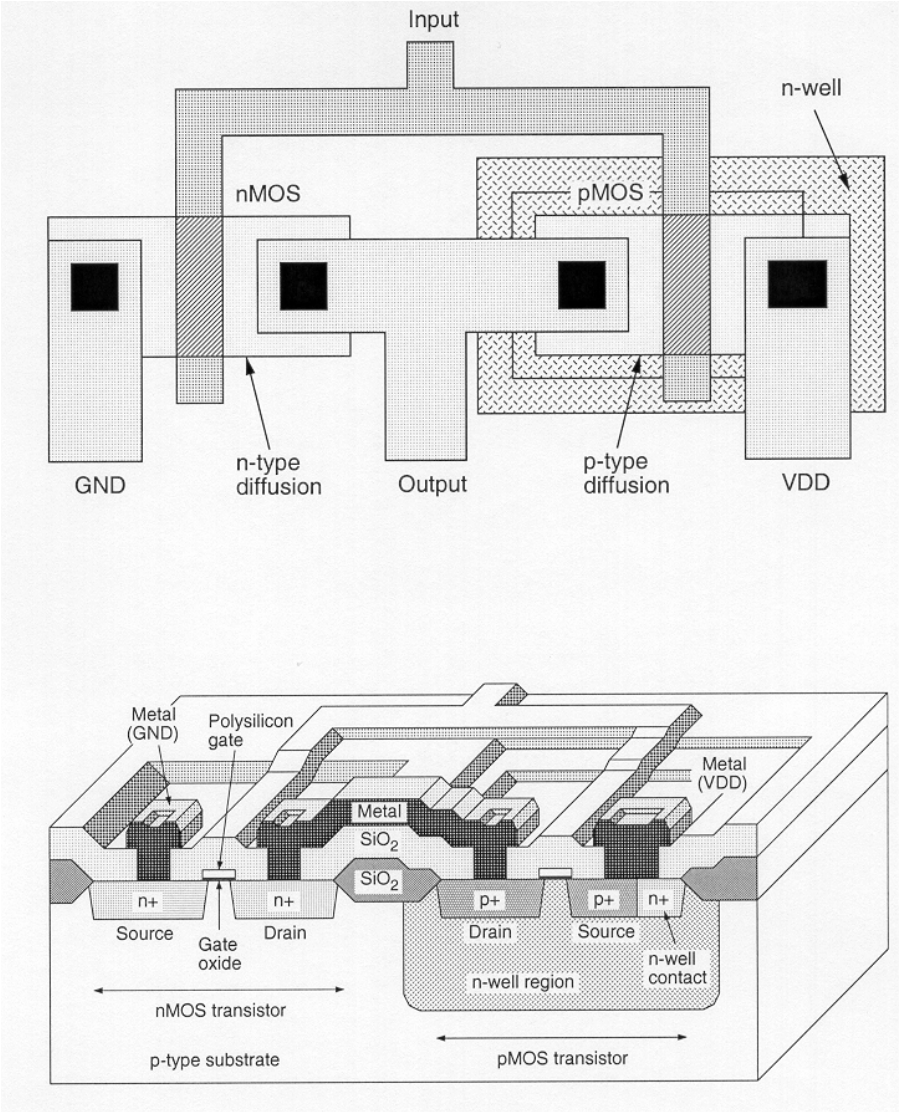
- **Insulating SiO_2 deposited using chemical vapor deposition (CVD)**
- **Source/Drain/Substrate contacts exposed**

Inverter Fabrication



- **Metal (Al, Cu) deposited using evaporation**
- **Metal patterned by etching**
- **Copper is current metal of choice due to low resistivity**

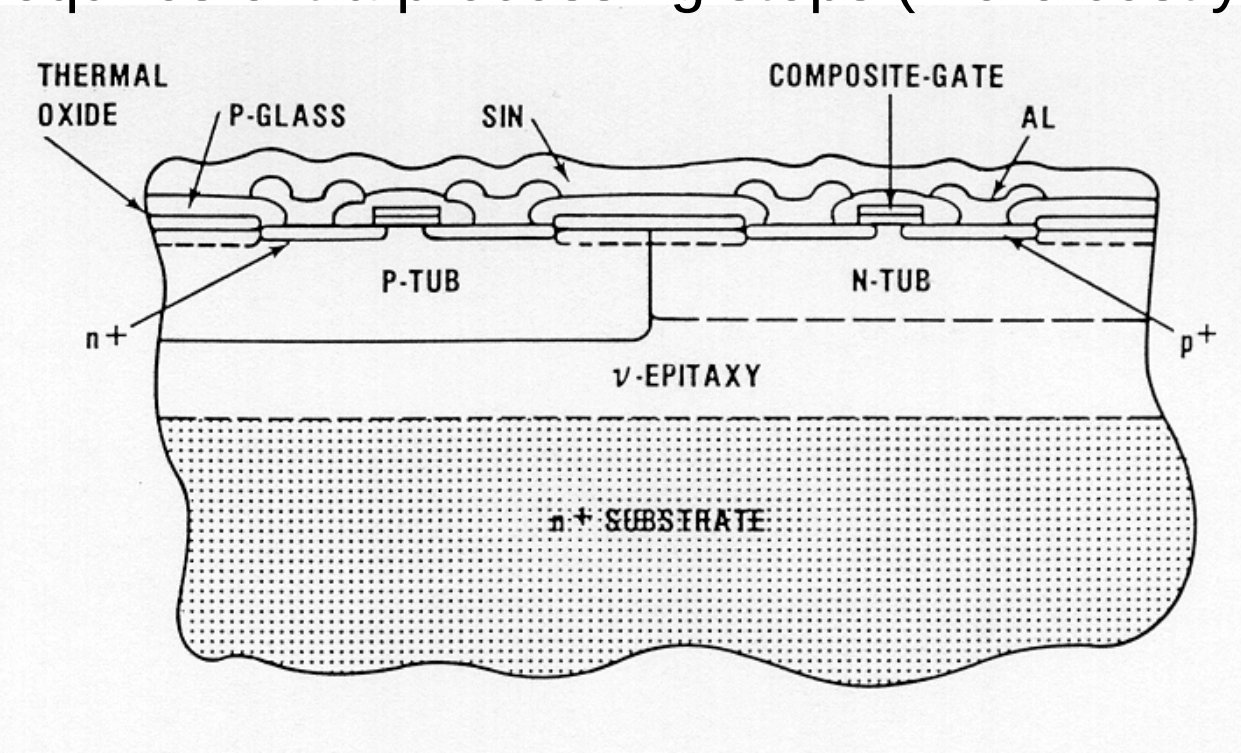
NWELL MOS Process



- **MOS transistors use PN junctions to isolate different regions and prevent current flow.**
- **NWELL is used in P-substrate so that PMOS transistors are isolated and don't share currents.**

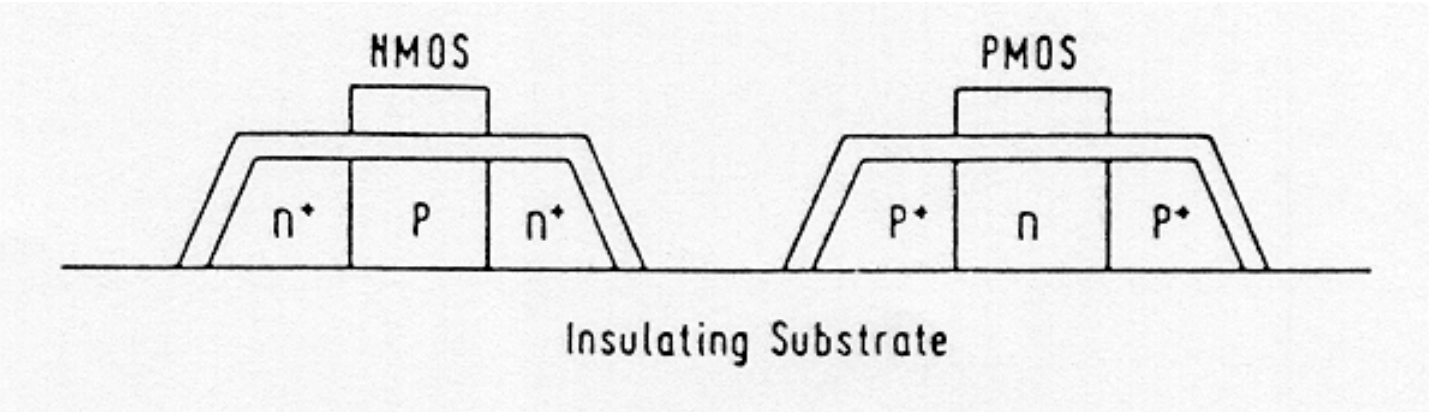
More Complex Processes

- **Twin Well CMOS Process**
  - Can help to avoid body effect
  - Allows for Vt and channel transconductance tuning
  - Requires extra processing steps (more costly)



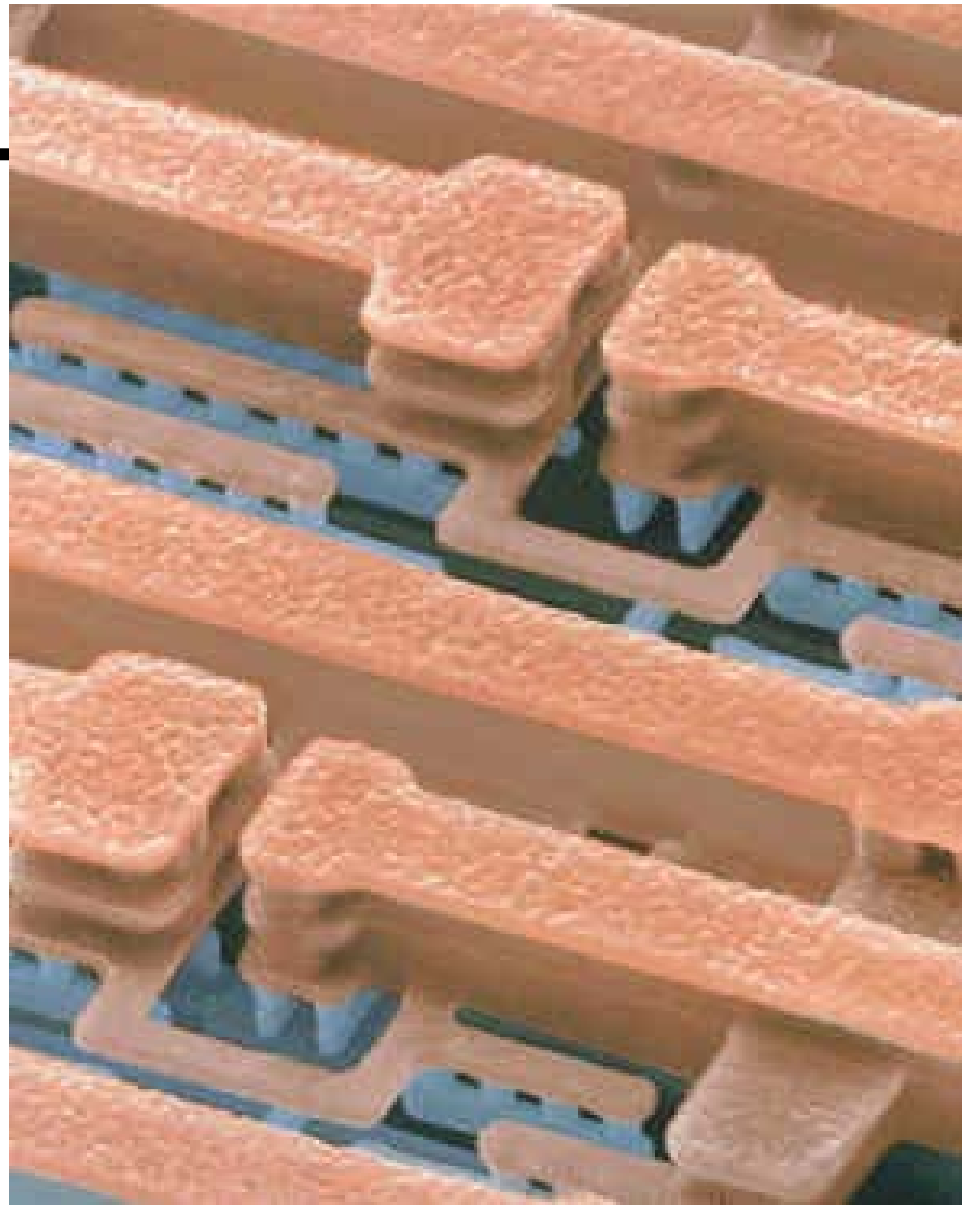
Silicon-On-Insulator (SOI) Process

- **Both transistors built on insulating substrate**
  - Allows for tight compaction of design area
  - Some of the parasitic capacitances seen in bulk CMOS disappear
  - Wafer cost is high (IBM produces SOI, Intel doesn't)



Wires

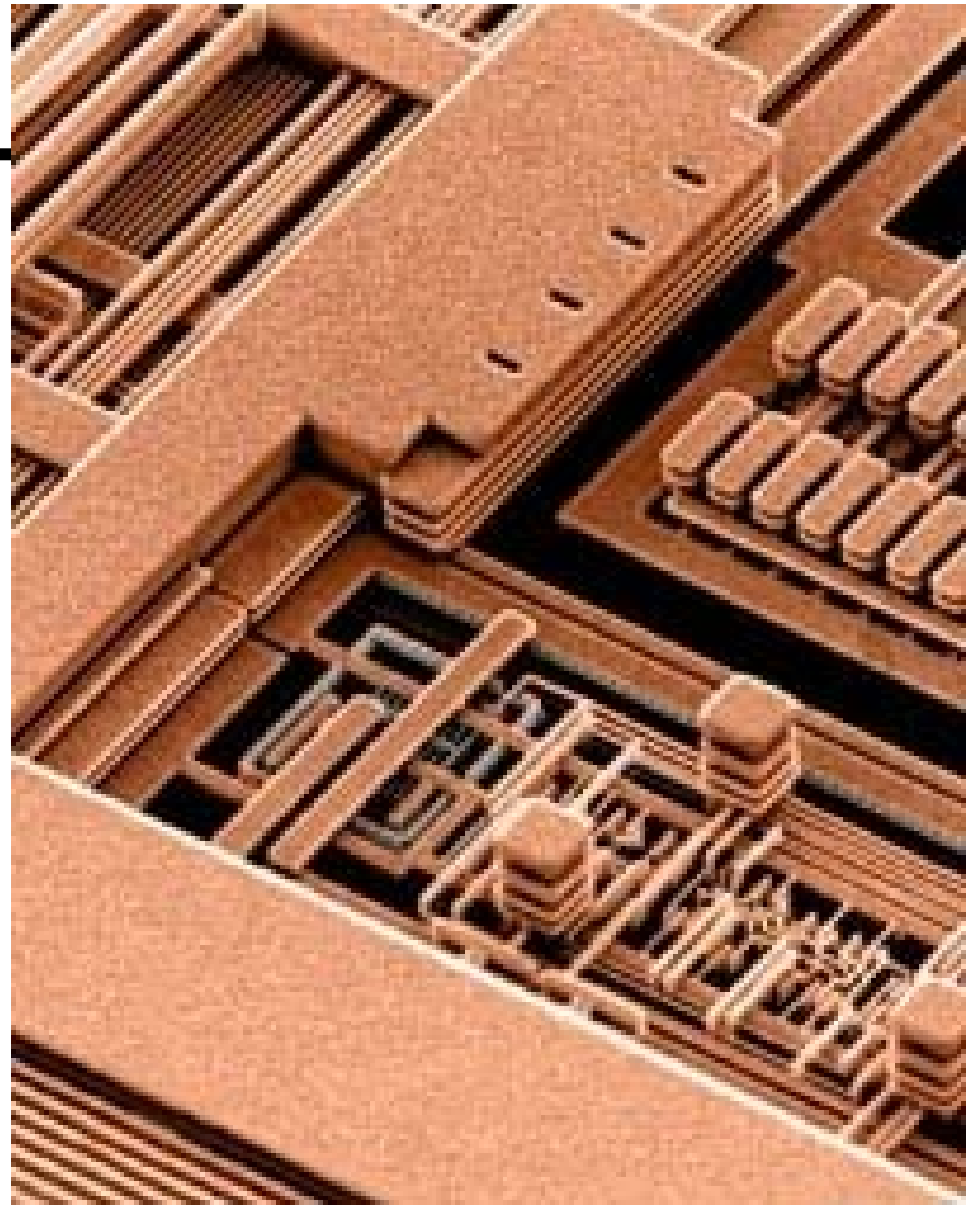
- **Four levels of wires shown here**
- **Designers specify each layer and connections between layers**



Source: IBM

Chip Wires

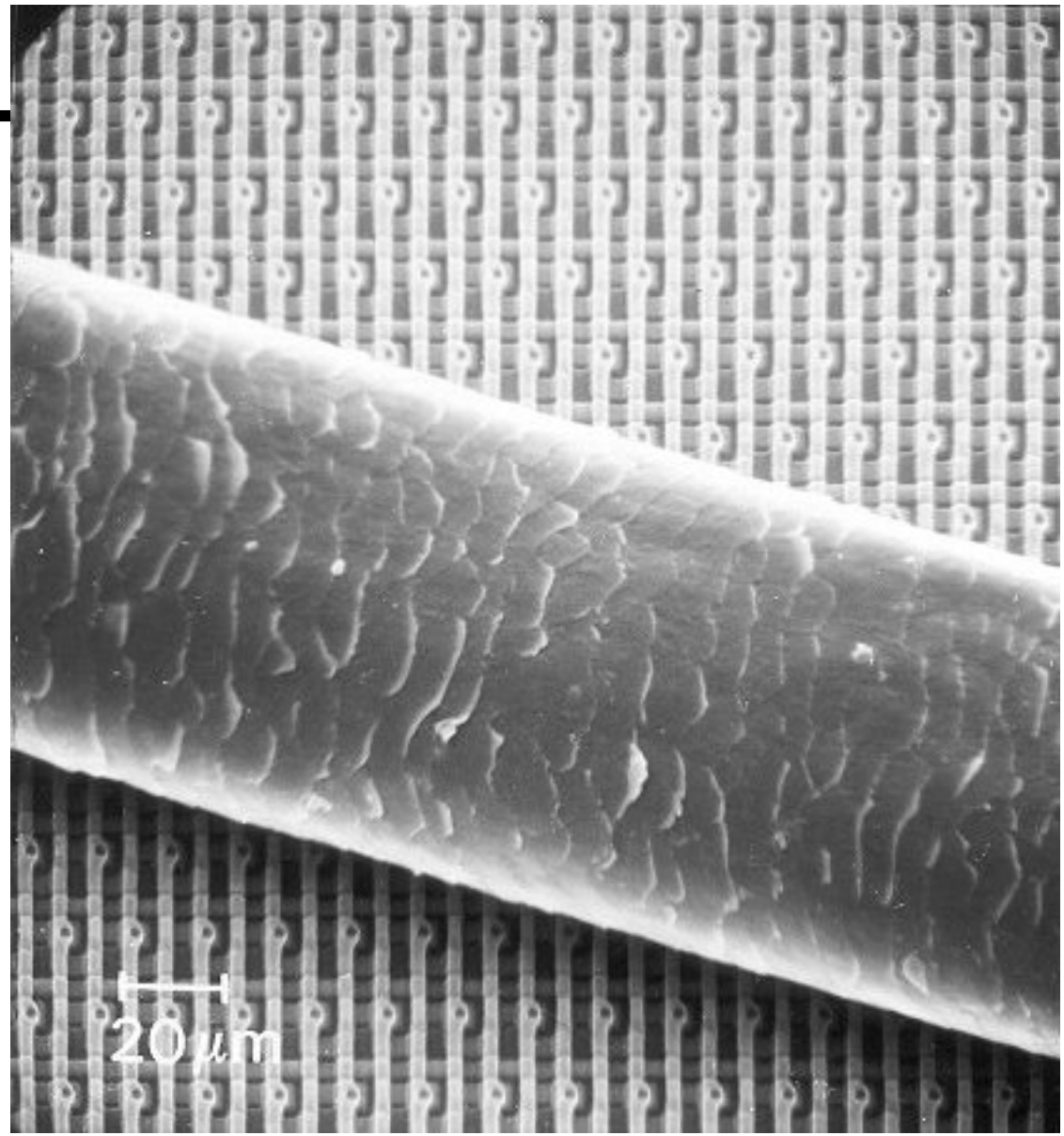
- **Modern chips have up to 8 layers of wires**



Source: IBM

Memory Array

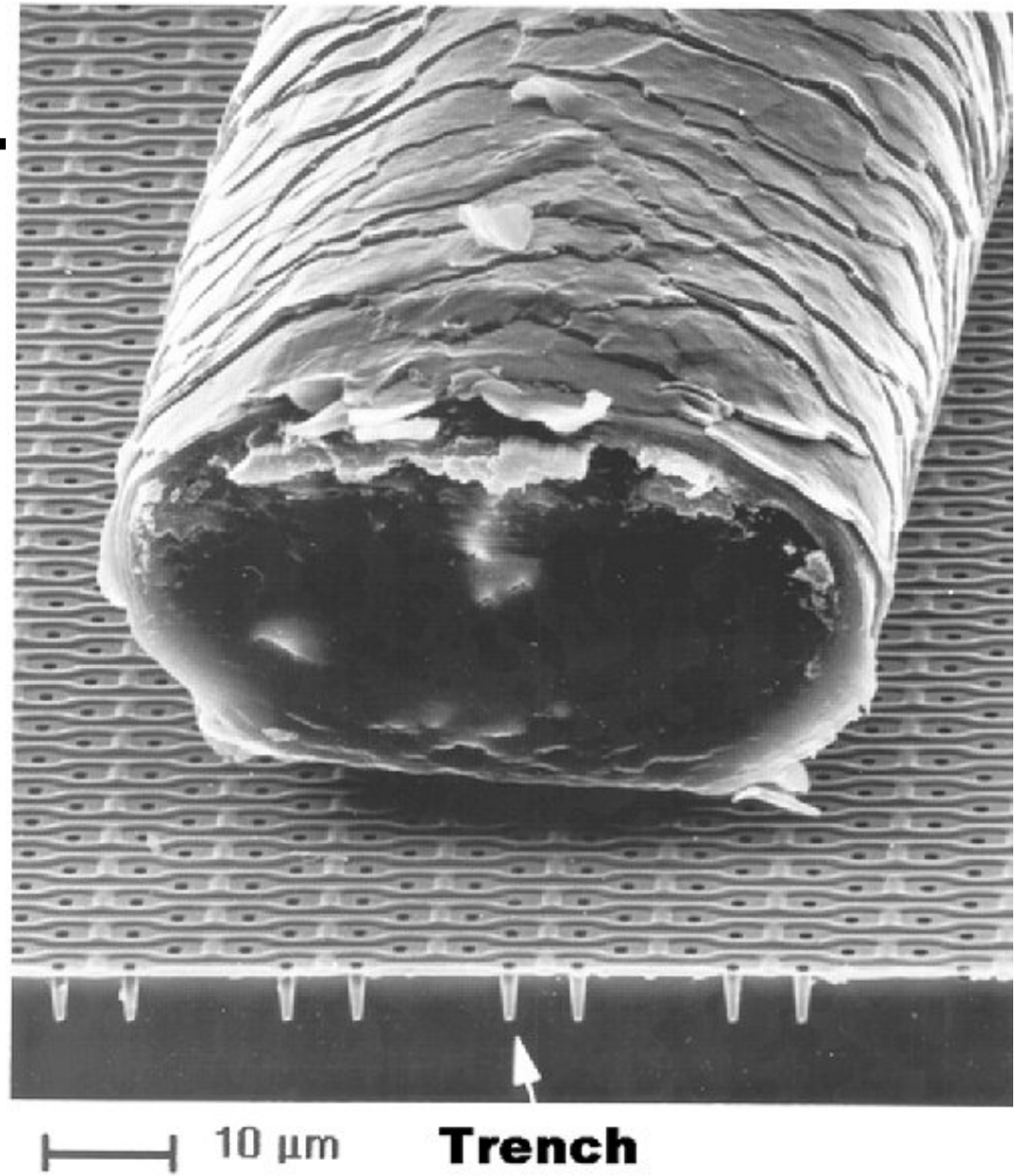
- **Human hair on a 256 Kbit memory chip**



Source: Helmut Föll

Memory Array

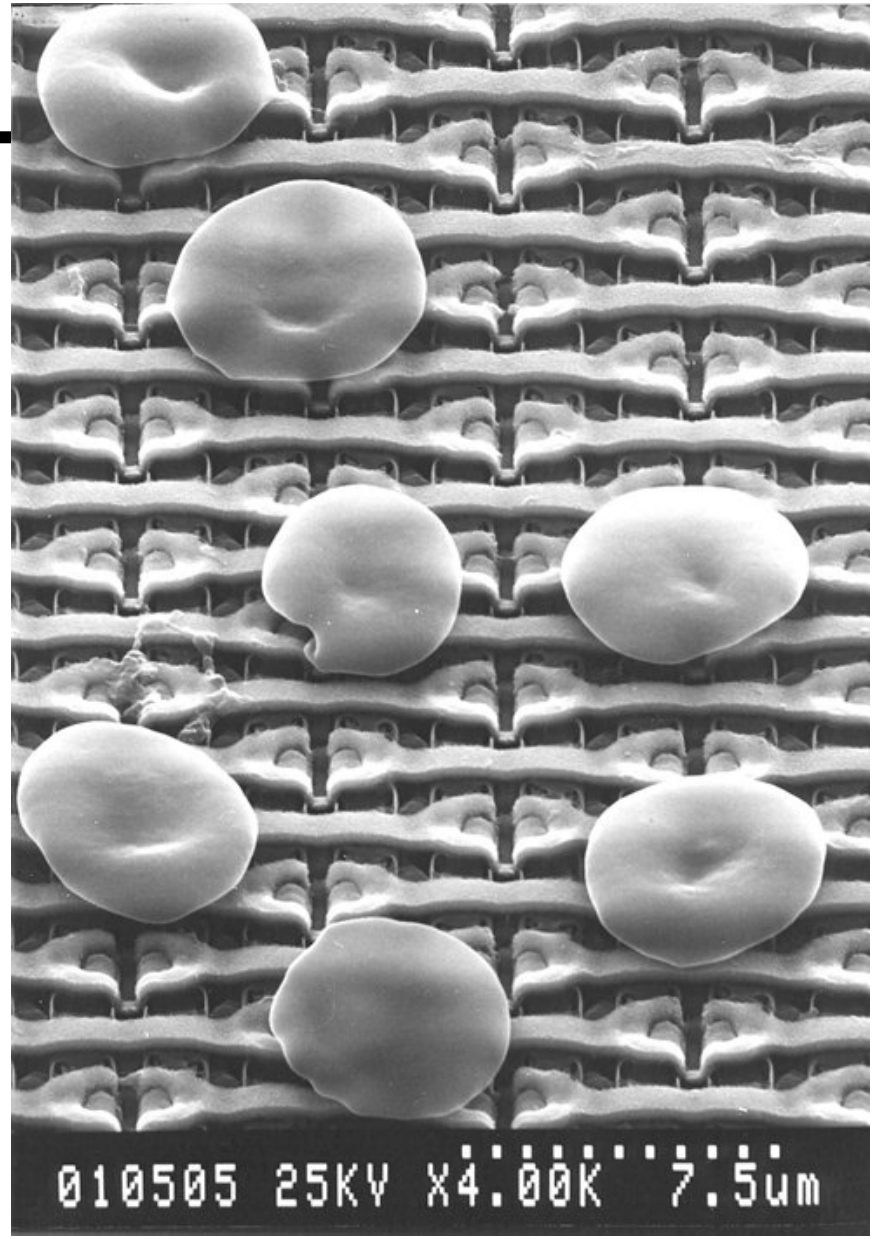
- **Human hair on a 4 Mbit memory chip**
- **Note DRAM trench capacitors**



Source: Helmut Föll

Memory Array

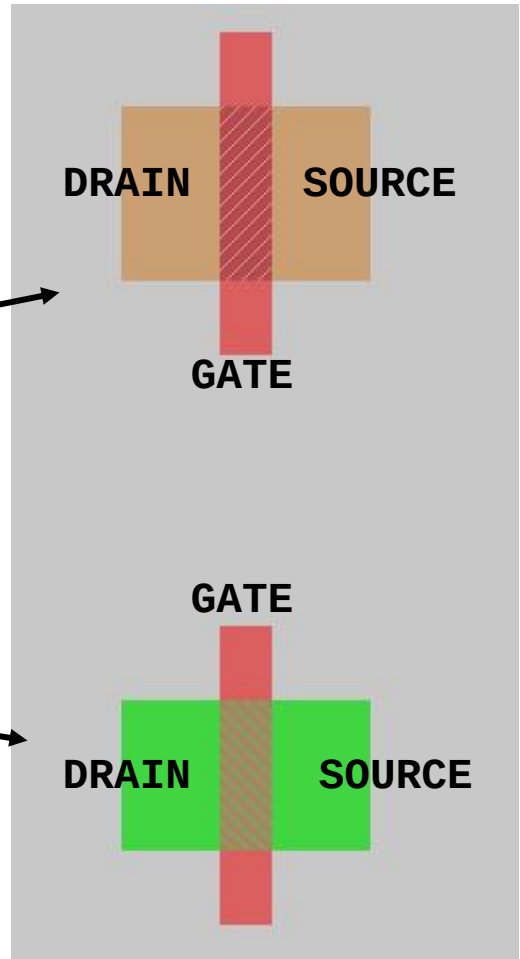
- **Red blood cells on a 1 Mbit memory chip**



Source: Helmut Föll

Transistor Layout

- **Drawing a transistor is this easy!**



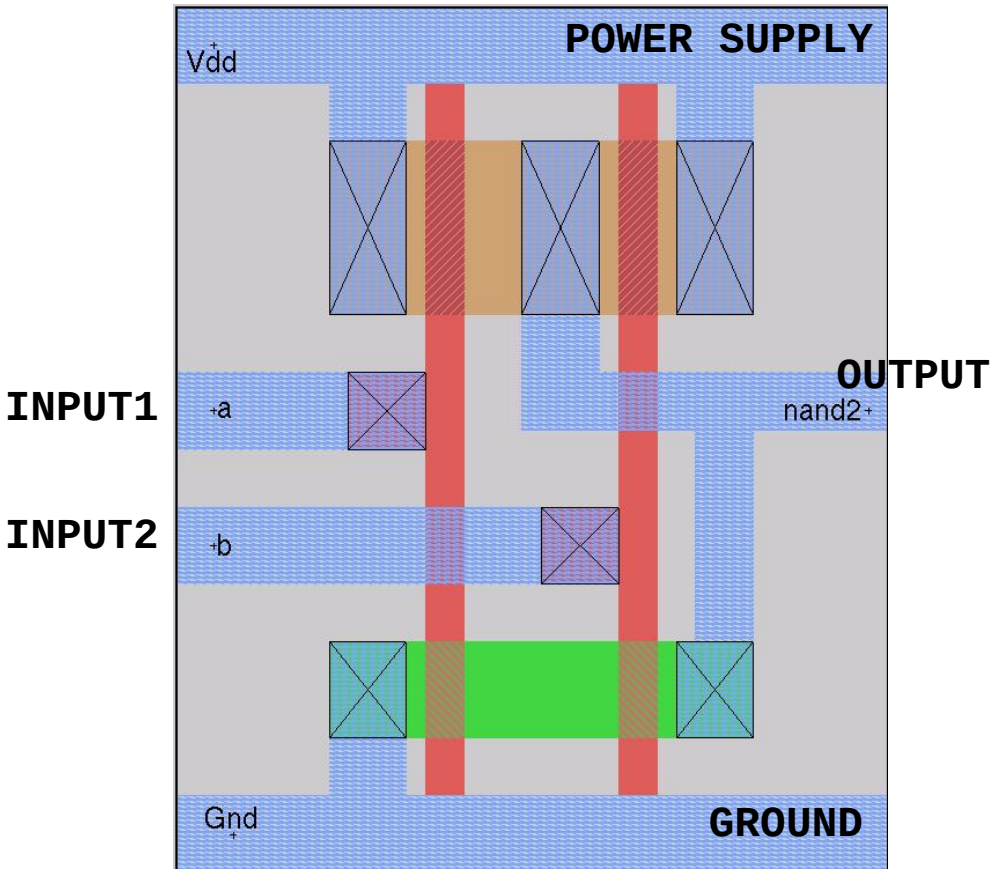
PMOS transistor

NMOS transistor

Source: Mike Lai

AND Gate Layout

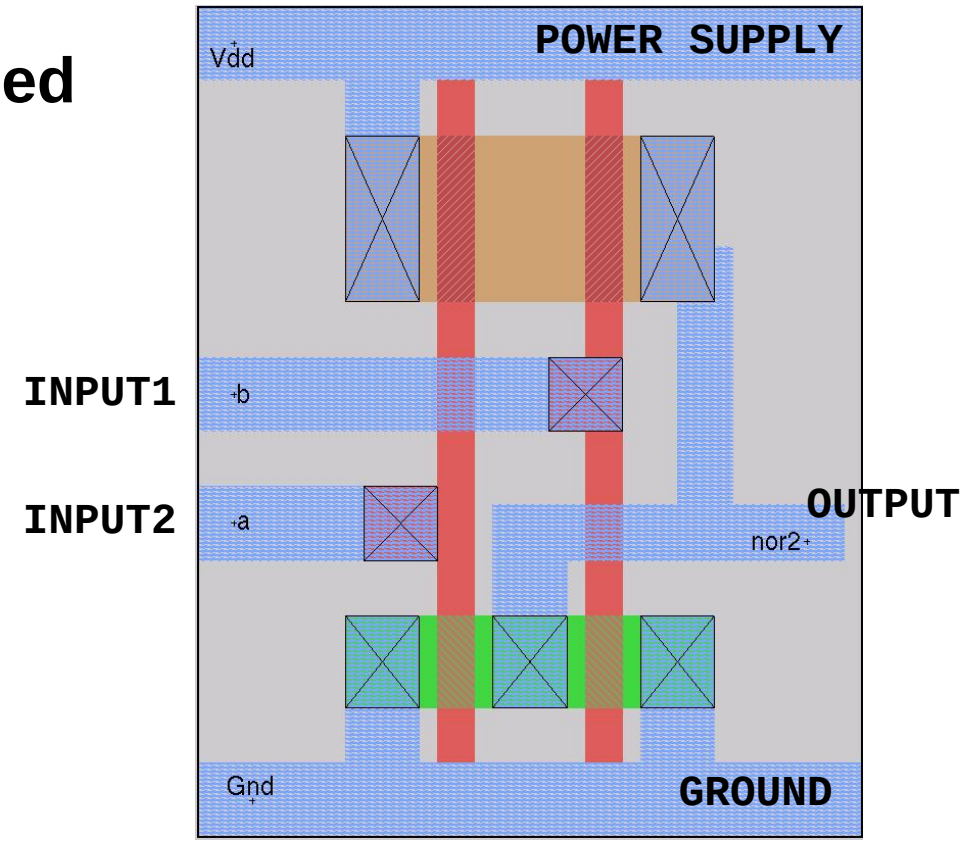
- **Here is an AND gate (with an inverted output, which is called a NAND)**



Source: Mike Lai

OR Gate Layout

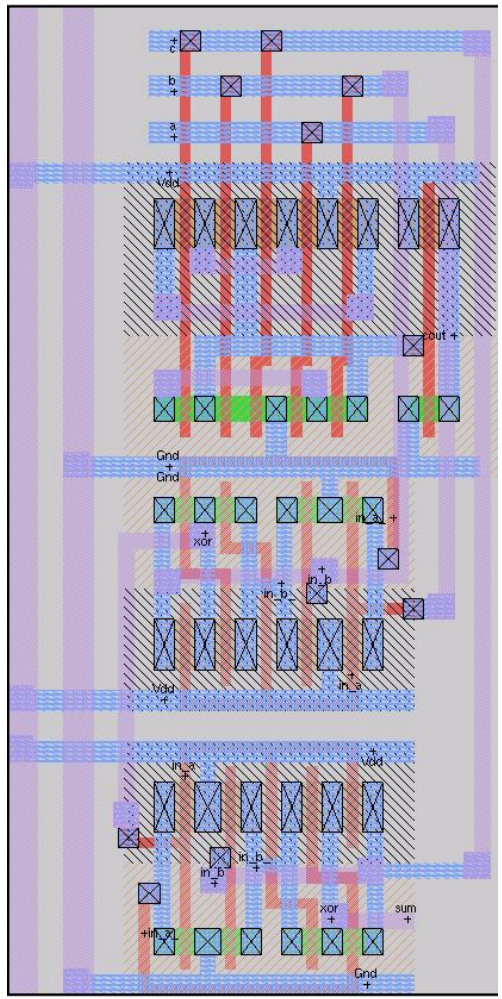
- **Here is an OR gate (with an inverted output, which is called a NOR)**



Source: Mike Lai

Full Adder Layout

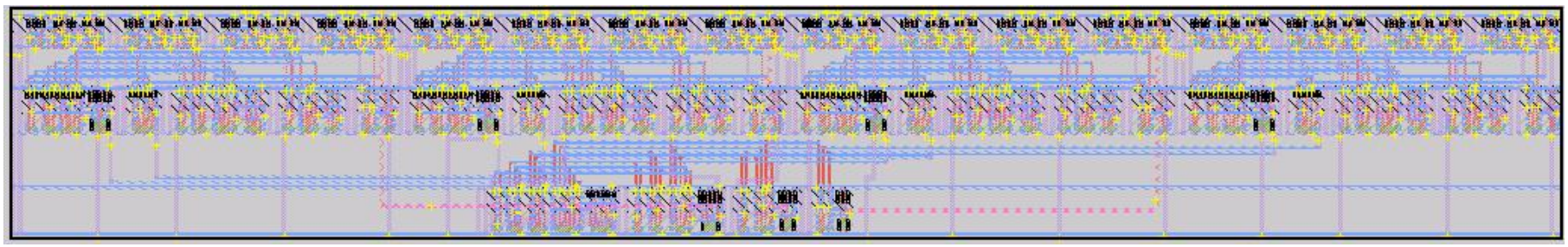
- **Here is a Full Adder**



Source: Mike Lai

16-bit Adder Layout

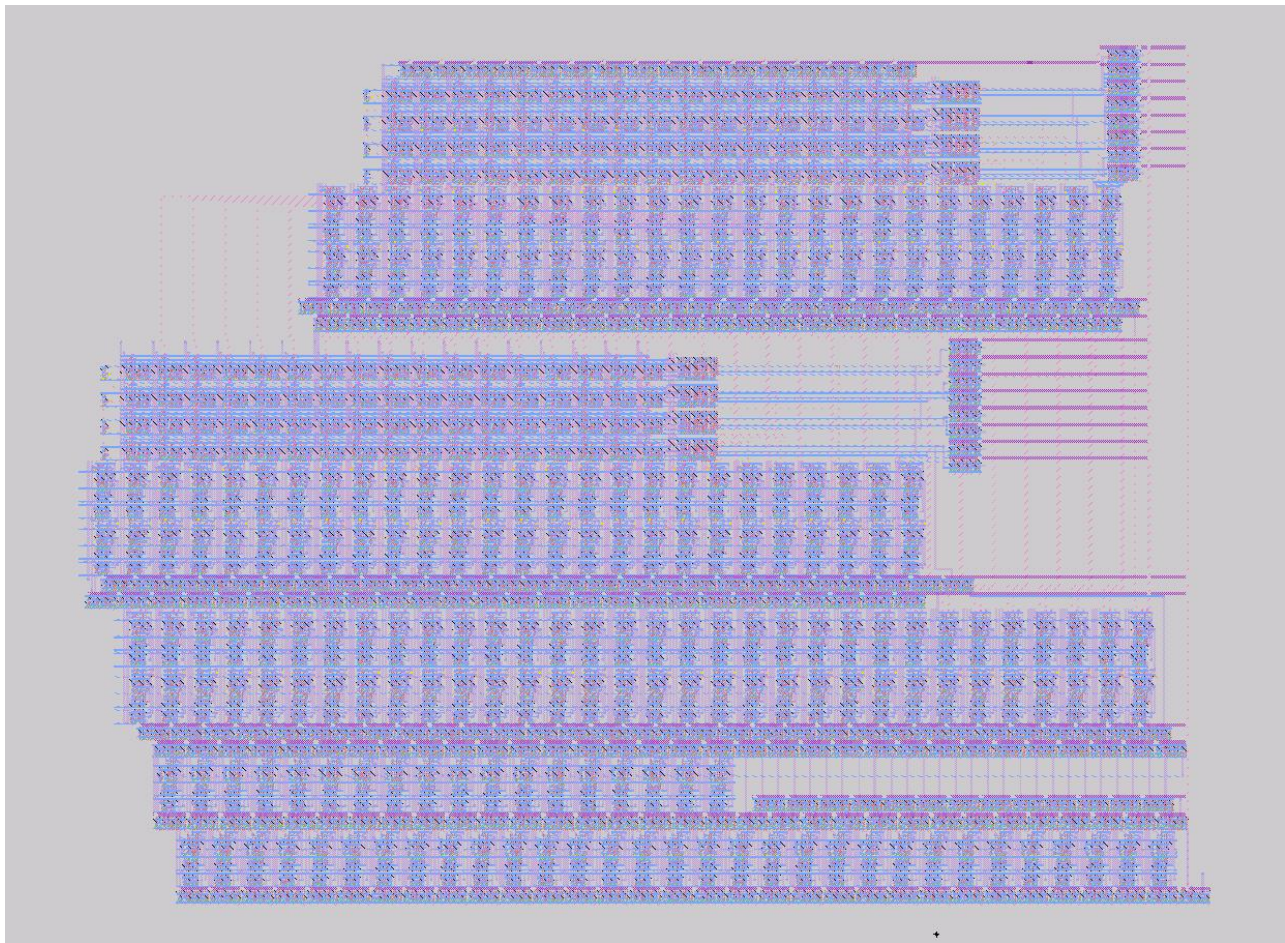
- **Here is a complete 16-bit adder (it adds two numbers where each input can range from –32,000 to +32,000)**
- **This adder contains 16 full adders (essentially) plus additional circuits for fast addition**



Source: Mike Lai

16-bit Multiplier Layout

- **Here is a complete 16-bit x 16-bit multiplier (each input can range from –32,000 to +32,000)**



Source: Mike Lai

Next Topic: MOSFETs and Inverters

- **Inverter Layout**
- **MOS Structure**
- **Inverter Characteristics**
  - Transfer functions, noise margins
- **CMOS Inverters**