EEC 116 Fall 2011 Prelab #5

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Reading: Rabaey Chapters 7.1-7.3 [1].
Reference: Kang and Leblebici Chapters 7 and 8 [2].

For **all** problems in this prelab assignment, assume we are using enhancement-type NMOS and PMOS transistors which have the characteristics shown in Table 1, unless otherwise specified. Also, assume **minimum** length devices unless otherwise specified.

Parameter	NMOS	PMOS
V_{T0}	0.5 V	-0.55 V
μC_{ox}	350 μA/V^2	125 μA/V^2
γ	0	0
L_{min}	0.180μm	0.180μm
W_{min}	0.450μm	0.450μm
λ	0.0 V^{-1}	0.0 V^{-1}
C_g	13.5 fF/μm^2	13.5 fF/μm^2
C_d,C_s	5.28 fF/μm	5.28 fF/μm
V_{DD}	1.8 V	

Table 1: Assumed Transistor Parameters.

1 Edge-Triggered Flip-Flop Design

For this problem, use the device parameters in Table 1.

Problem 1.1 Redraw the schematic of Figure 1 at the transistor level and label the D, clk, $\overline{clk}$, and Q signals on the schematic such that the circuit operates as a **static positive edge-triggered flip-flop.**

Problem 1.2 Choose sizes for the transistors in your schematic from Problem 1.1 based on equalizing the CMOS inverter rise and fall times. Make sure your sizes are integer multiples of $\lambda = 90$nm.

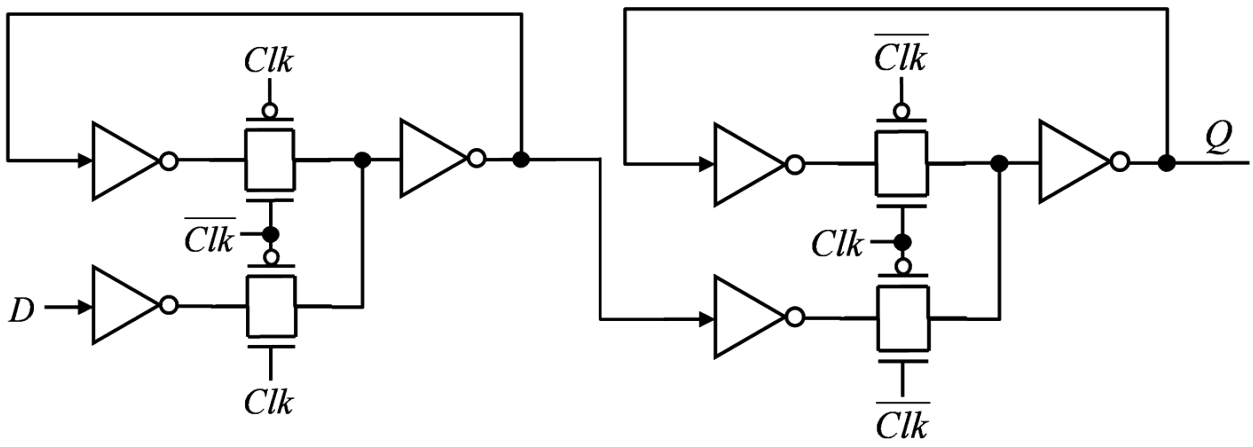

Figure 1: Negative Edge-Triggered Flip-Flop.

Problem 1.3 Calculate the setup time t_{setup} and clock-to-Q propagation delay t_{clkQ} for the flip-flop you designed in Problem 1.2. Assume ideal step inputs for D and the true and complement versions of the clock. Assume a gate capacitance per unit area to ground C_g and a drain/source capacitance per unit width to ground C_d/C_s as shown in Table 1 and neglect all other capacitances. Use the average current method at the beginning and end points of the appropriate transitions.

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.