1 Edge-Triggered Flip-Flop Design

For this problem, use the device parameters in Table 1.

Problem 1.1 Redraw the schematic of Figure 1 at the transistor level and label the $D$, $clk$, $clk$, and $Q$ signals on the schematic such that the circuit operates as a static positive edge-triggered flip-flop.

Problem 1.2 Choose sizes for the transistors in your schematic from Problem 1.1 based on equalizing the CMOS inverter rise and fall times. Make sure your sizes are integer multiples of $\lambda = 90\text{nm}$.
Problem 1.3 Calculate the setup time $t_{\text{setup}}$ and clock-to-$Q$ propagation delay $t_{\text{clkQ}}$ for the flip-flop you designed in Problem 1.2. Assume ideal step inputs for $D$ and the true and complement versions of the clock. Assume a gate capacitance per unit area to ground $C_g$ and a drain/source capacitance per unit width to ground $C_d/C_s$ as shown in Table 1 and neglect all other capacitances. Use the average current method at the beginning and end points of the appropriate transitions.

References
