

Ternary single electron tunneling phase logic element

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(Received 25 January 1999; accepted for publication 4 May 1999)

An analysis of a ternary single electron tunneling phase logic element is presented. The analysis is based on Monte Carlo simulations and an analytical treatment of a resistively loaded tunneling junction at low temperatures. We show that tristable operation can be obtained over a 19% dc bias operating range by optimizing the pump frequency and amplitude. For large ac frequencies, our optimizations also show that simple linear relationships exist between the optimal parameters (the optimal dc bias and pump amplitude) and frequency. Finally, we show that the ternary phase state of a clocked element can be controlled by an input signal provided that the clock turn-on is not too abrupt. The results should be of use in the design of ternary and other multilevel tunneling phase logic families. © 1999 American Institute of Physics. [S0003-6951(99)03826-7]

Digital logic circuitry based on phase locking of single electron tunneling processes in ultrasmall tunneling junctions has recently been proposed.¹ Previous work on this approach, which is referred to as single electron tunneling phase logic (TPL), has focused on the basic operation of bistable elements,² including stability at high operating temperatures.³ Previous work shows that binary TPL offers an attractive approach to realizing ultrasmall devices with ultra-low-power dissipation, thereby making possible the development of circuits with integration levels orders of magnitude beyond those of conventional technologies.² The effective use of such circuits will depend on the ability to deal with various issues, including the severe interconnect bottleneck problem at high integration levels. Thus, the reduction in the number of gates needed for logic operations offered by ternary and higher-order multilevel logic would be highly desirable for TPL circuitry. In this letter, we focus on this possibility.

We have simulated a resistively loaded tunneling junction with a Monte Carlo approach similar to that described by Likharev *et al.*⁴ and obtained current–voltage curves, as shown in Fig. 1, demonstrating phase locking, i.e., the correlation of tunneling events to the pump. By fixing the RC time constant of the circuit, the dc bias determines the rate of tunneling events across the junction. With an externally applied ac signal, the tunneling events are either sped up or slowed down, thus giving rise to a series of steps in the current–voltage curves.

For each curve in Fig. 1, the dc bias is swept and the current is plotted. The simulation is done at zero temperature with a finite but large ($G_T \gg 1/R$) tunneling conductance. The normalized current I is defined as the number of tunneling transitions per ac period τ_p , thus the one-third subharmonic corresponds to a current of $1/3$. For each curve, the ac amplitude has been selected for the largest one-third subharmonic step size at a given ac frequency. The middle curve corresponds to operation at the optimum frequency, where

the operating range (ratio between the step size to the midpoint of the step) is maximum.

The potential across the tunneling junction as a function time under optimum biasing conditions is shown as an inset in Fig. 1, where the top curve shows the pump and the bottom curve shows the existence of three stable, equally separated phase states available for ternary logic. The phase states lock within ten pump periods ($10\tau_p$), and depending on the initial conditions, they may lock into one of three phase states. The sharp transitions in the wave forms correspond to acquiring enough potential across the tunneling barrier for an electron tunneling event to occur. The smaller oscillations in these wave forms correspond to the effect of the pump on the output potential.

In this section we make use of equations previously derived for a single Josephson junction coupled to external radiation (see Ref. 5 and the appendix) to examine the locking range. The equations of the Josephson system are iden-

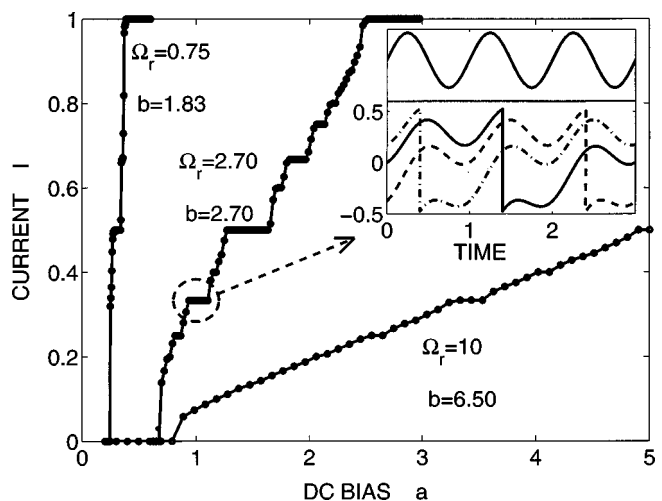


FIG. 1. I - V curves under different pump conditions (ac amplitude b^* , ac frequency Ω_r): left (1.83, 0.75), middle (2.70, 2.70), and right (6.50, 10.0). Inset: Ternary phase states of the $1/3$ subharmonic for operating conditions: dc bias $a^{*\dagger} = 1.0196$, $b^{*\dagger} = 2.7$, and $\Omega_r^\dagger = 2.7$. Time is normalized to the pump period τ_p .

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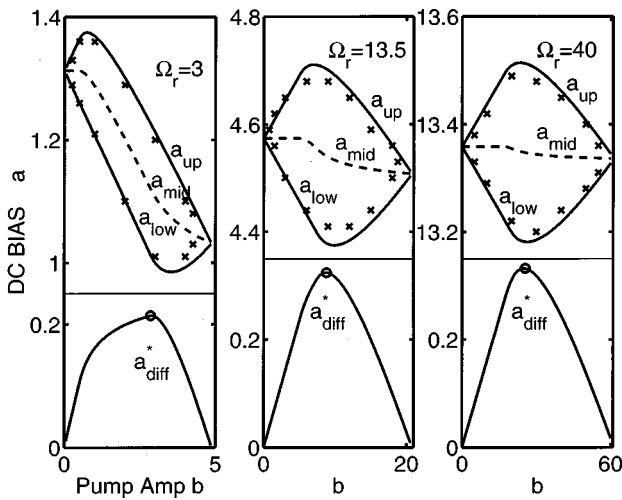


FIG. 2. Top: a_{up} and a_{low} as a function of b , for $\Omega_r=3, 13.5,$ and 40 . Bottom: a_{diff} for each region of stability. Note at higher ac frequencies, the shape of the locking region becomes more symmetrically distributed about its midpoint.

tical to those for the simple deterministic model of single electron tunneling in a resistively loaded junction.¹ Regions of stability (locking) for the ternary state determined from this analysis are plotted in Fig. 2, along with those determined from Monte Carlo simulations. For a given externally applied frequency there is a corresponding region of stability in the dc bias versus ac amplitude (a vs b) parameter space. The vertical cross section delimited by (a_{up}, a_{low}) of each region corresponds to the horizontal step size on the one-third subharmonic as seen previously in Fig. 1. We seek the largest dc bias range (vertical cross-sectional width) for a given frequency. To this end, the width $a_{diff} (\equiv a_{up} - a_{low})$ of the vertical cross section is plotted below its corresponding region of stability (bottom of Fig. 2), from which it can be seen that for a given applied ac frequency, there corresponds an optimal ac amplitude, dc step size, and midpoint denoted by b^*, a_{diff}^* , and a_{mid}^* , respectively.

Next, we seek the optimal operating range which we define as the ratio of the optimal step size to the midpoint of the optimal step, a_{diff}^*/a_{mid}^* . A dc bias operating range as high as 19% is obtained for an ac frequency $\Omega_r = 2.7 \equiv \Omega_r^\dagger$, and amplitude $b^* = 2.7 \equiv b^{*\dagger}$ (bottom of Fig. 3). We make use of this ac frequency (Ω_r^\dagger) and corresponding optimal parameters $b^{*\dagger}$ and $a_{mid}^{*\dagger}$ in the following section. The fast falloff left of the optimum operating frequency Ω_r^\dagger is due to the shrinking step size as the ac frequency approaches 0, and the slow falloff to the right corresponds to the linearly increasing dc bias point (a_{mid}^* linear in Ω_r with slope $m=1/5$) at high ac frequencies while the step size becomes saturated at $1/3$ of the threshold voltage (top of Fig. 3). In the neighborhood of Ω_r^\dagger , however, there is an even tradeoff between the shrinking step size and increasing dc bias point. We note that the optimal ac amplitude b is also linear in Ω_r with slope $m=5/8$, suggesting that simple relationships exist between the optimal parameters and applied frequency which serve as useful initial estimates to the locking regions.

In the previous section, we examined the operating range for tristable states. In this section, we examine the operation of a simple logic gate analogous to the inverter gate in bistable logic: a single TPL element capacitively coupled to

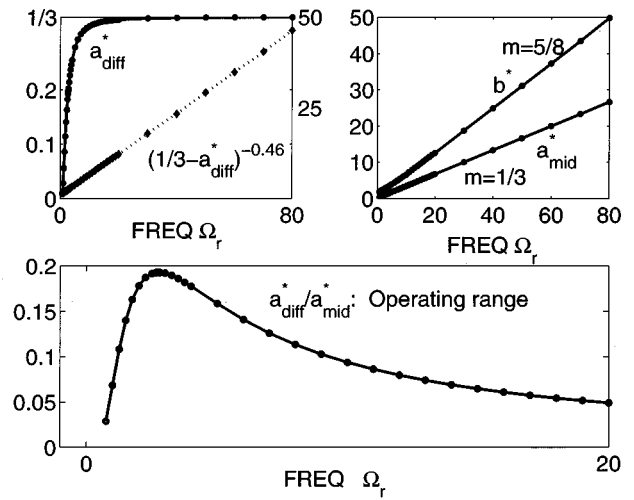


FIG. 3. Top left: a_{diff}^* vs Ω_r and linear approximation. Top right: a_{mid}^* and b^* vs Ω_r . Bottom: a_{diff}^*/a_{mid}^* vs Ω_r .

a driving input signal. We use a sawtooth wave form with phase ϕ_{input} of the same amplitude and period ($3\tau_p$) as the tunneling oscillations to mimic a possible output from a previous stage. The flow of logic is controlled by clocking the gate with a rising dc bias of rise time T_r centered at phase ϕ_{clock} , and the output phase ϕ_{out} is read after it is settled into a stable logic state (control sequence at the top of Fig. 4). A phase map for $T_r=0$ (square) clock signal and coupling ratio $C_{junction}:C_{coupling}=1:1$, chosen so as to make simply connected output phase regions, is shown at the bottom of Fig. 4. From the phase map of the $T_r=0$ case, it can be seen that the state of the gate is a strong function of both the input and clock signals.

While the clock phase dependence seen in Fig. 4 suggests that some type of field-programmable gate array approach may be possible with this device, an insensitivity to the clock phase is desirable for the simplest logic schemes. Thus, we examined phase maps for various clock rise times

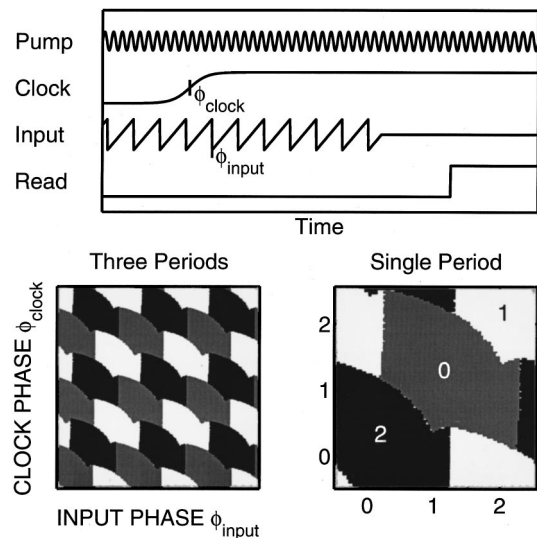


FIG. 4. Top: timing diagram. Bottom: ϕ_{out} as a function of ϕ_{input} and ϕ_{clock} for $T_r=0$, an enlargement of a single section to the right, with regions centered about particular states labeled with arbitrary logic symbols (012), corresponding to the three stable ternary phase states.

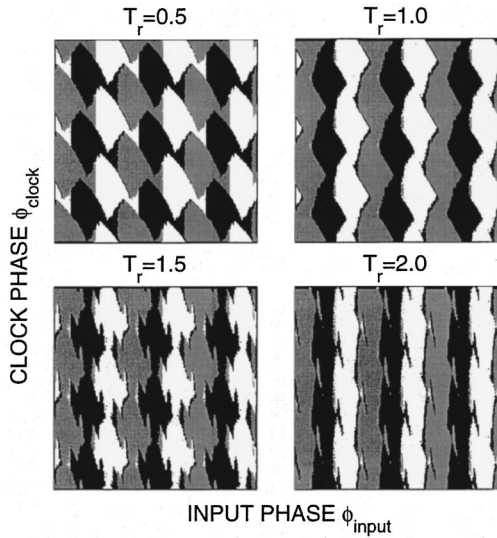


FIG. 5. Phase map for $T_r=0.5, 1.0, 1.5,$ and 2.0 .

T_r , defined as the time in which the clock reaches half of its final value. The results in Fig. 5 show that for sufficiently long rise times, the clock loses its influence on the output state, which becomes solely dependent on the input phase, a necessary condition for reachability of all three phase states from the output of a previous stage. In separate simulations, we have also investigated the effect of the ratio between coupling-to-tunneling capacitance and found that a coupling ratio of 1 works well. We have also found that the output state is not dependent on the turn-off time of the input signal. All these results indicate that this ternary gate, which is analogous to a binary inverter, functions reasonably well for sufficiently long clock rise times. A logic table simplification of the phase-state map shows that our inverter-equivalent gate performs a rotation operation ($Y=X\ominus 1$).

In conclusion, we have extended the study of tunneling phase logic by examining the case of a tristable TPL element. Our Monte Carlo simulations show that tristable operation produces the one-third subharmonic step in the current-voltage characteristic of a single tunneling junction with an applied ac signal. Our simulations also show stable locking into three equally separated phase states. We have extended the analytical results for the stable operating regime to include optimization of an operating range for ternary logic, which puts constraints on the ac amplitude and frequency, yielding a maximum operating range of 19%. In addition, we have found linear relationships between optimal parameters and the ac frequency, thereby suggesting a simpler optimization scheme might be possible for other multi-level logic families. Finally, we have shown that operation of an inverter-equivalent gate displays large, simply shaped

output regimes in a phase-state map, thereby demonstrating that all phase states are reachable in this simpler gate. This suggests that they may also be reachable for more highly functional gates under suitable clock conditions, namely, a slow rise time in the clock transition. We hope to extend this work by adding more functionality in the types of basic logic gates available in the ternary tunneling logic family. While further study is needed to investigate interactions and signal transfer between coupled ternary gates in a circuit, the results presented here indicate that ternary tunneling phase logic is a promising approach.

The authors would like to thank A. Krishnaswamy, H. Fahmy, C. Y. Hung, and A. Loke for fruitful discussions. This work was supported by the DARPA Advanced Microelectronics Program under Contract No. N66001-97-8905. Support from Fujitsu Laboratories, Ltd., is also gratefully acknowledged.

APPENDIX: EQUATION FOR AC DRIVEN JOSEPHSON JUNCTION

From Ref. 2, the differential equation for the time evolution of the potential ϕ across the tunneling junction can be written as

$$a + b \cos(\Omega_r \tau) = \phi - 2\nu + \pi \frac{\partial \phi}{\partial \tau},$$

for $2\nu - 1 \leq \phi \leq 2\nu + 1$, where a and $b \cos(\Omega_r \tau + \alpha)$ are the dc bias and ac signal, τ is the normalized time, and Ω_r is the normalized frequency. For each Ω_r and b , there is a corresponding range in a , between a_{up} and a_{low} , for which locking occurs. The method in obtaining these solutions consists of finding the roots for the following equation:⁵

$$\begin{aligned} \phi_n(\tau) = & 2\nu_n + \phi_{n0} e^{-(\tau - \tau_n)/\pi} + a[1 - e^{-(\tau - \tau_n)/\pi}] \\ & + j[\sin(\Omega_r \tau + \chi) - e^{-(\tau - \tau_n)/\pi} \sin(\Omega_r \tau_n + \chi)], \end{aligned} \quad (\text{A1})$$

for $2\nu_n - 1 \leq \phi_n \leq 2\nu_n + 1$, $\tau_n \leq \tau \leq \tau_{n+1}$, $\chi = \alpha + \arctan(\pi \Omega_r)^{-1}$ and $j = b/[1 + (\pi \Omega_r)^2]^{1/2}$. The values τ_n correspond to successive times when the value ϕ_{n-1} reaches an odd integer. Taking the initial value $\phi_{00} = -1$ at $\tau = 0$, the condition for locking to the 1/3 subharmonic is satisfied when $\phi_0(3\tau_r) = 1$, where $\tau_r = 2\pi/\Omega_r$ (the normalized pump period), and when the condition $-1 < \phi_0(\tau) < 1$ is met for $0 < \tau < 3\tau_r$.

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