OCIN Workshop Wrapup

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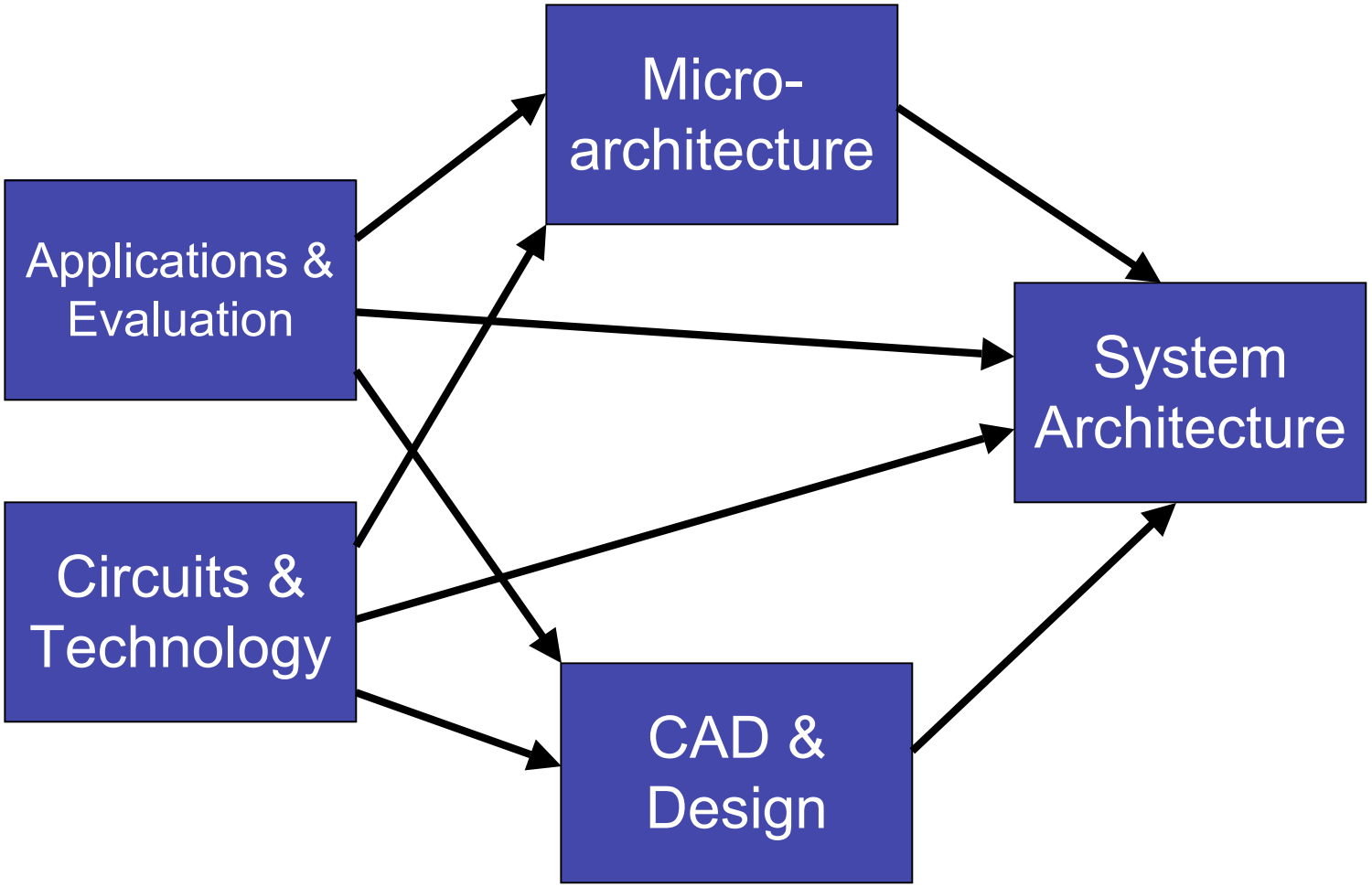
Thanks To

- Funding
  - NSF - Timothy Pinkston, Federica Darema, Mike Foster
  - UC Discovery Program
- Organization
  - Jane Klickman, John Owens, Li-Shiuan Peh
- Attendees
  - Speakers and poster presenters
  - Working groups did a great job!

OCINs are a Critical Technology

- Key component of
  - emerging multi-core systems
  - MPSoCs
- Straightforward scaling will not satisfy need
  - 15x over power budget for channels
  - Off-chip organizations give excessive latency
  - Support needed for monitoring/debugging
- Research is needed to close the gap
  - Will enable future systems
    - enterprise to handheld

Overview


Micro-
architecture
Applications &
Evaluation
System
Architecture
Circuits &
Technology
CAD &
Design

Enabling Circuits and Technology

- General areas to be addressed
  - Lower power communication
  - Lower power, fast memory
- Areas for future research (for year 2015 systems)
  - Low swing wires
  - Role of 3D integration for on-die interconnects
  - Role of photonics for on-die interconnects
  - Optimized metallization
    - Tradeoff high C lower layers for upper level layers

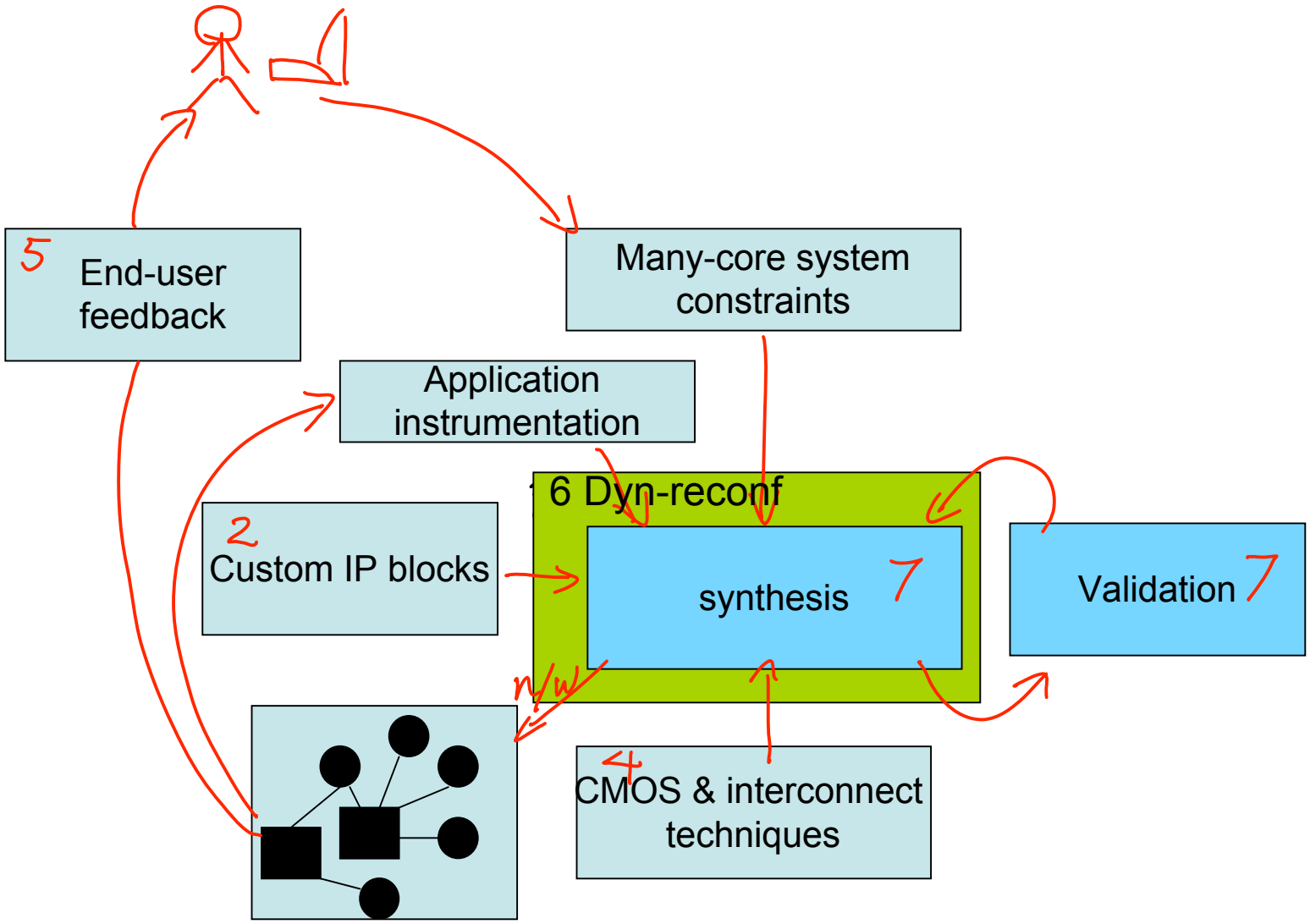
Application & Evaluation Research Issues

- Applications/Services
  - New programming models
    - performance aware constructs and annotations
  - Limits to scalability of coherence protocols (enhanced support for barriers, multicast)
  - Network support for classes of traffic
  - Models for RT guarantees (for SoC)
  - New types of network services
    - isolation, security, partitioning, error recovery, power-aware decisions, reconfiguration, ...
- Architectural benchmark suites & characterization
- Simulation tools and techniques

CAD Research Challenges

1. Network synthesis' interface with system-level constraints and design
2. Hybrid custom and synthesized tool flow
3. Design validation
4. Impact of CMOS scaling and new interconnect technologies (e.g. 3D integration, optical)
5. End-user feedback design toolchain
6. Dynamic reconfigurable network tools
7. Beyond simulation

CAD Overview



System Architecture Research Agenda

- Flow Control
  - Congestion control with bounded or limited buffering
  - Adaptive flow control/ switching for multi-modal traffic and time varying application requirements
- Network interface
  - Light weight, generic: low latency, tightly coupled, general programming, flexible and general purpose
  - Virtualized network interface
- Technology-aware topologies : higher dimensions
- Fault Tolerance, Reconfiguration
  - Self tuning links and switches to process variation, soft errors
  - Network reconfiguration to adapt to application requirements
  - Support for partitioning and virtualization: isolation, performance across domains, accelerators, traffic heterogeneity
- Support for monitoring, debugging

Enabling Microarchitecture

- Minimizing latency & power are key
  - Fundamental research needed in routers, interfaces, electrical design
  - Reliability and variability are emerging challenges
- Programming interface is key
  - Must expose low latency to software
  - Programmability drives network constraints & features
- Broader impact: making multicore systems viable, usable, and effective

Potential for Tremendous Impact

- Continued scaling of computing
- Reduced design complexity, improved design reuse
- Reliability in the presence of errors/variation
- Simplified programming

Next Steps

- Report
  - Summarize findings of workshop
  - I'll be asking for your help
- Special Issue of IEEE Micro
- Funding?