The revolution of the new millennium...
The Road to Multicore
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2002: POWER4+ is released
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2004: Sun Microsystems Releases the **Sun UltraSPARC IV** Dual Core CPU
More Multicores
More Multicores

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2005: Sun Microsystems Releases the Sun UltraSPARC T1 (codename Niagara) 8-Core CPU
Multicore Becomes Mainstream
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2005: Intel Pentium D (Smithfield, Presler)
2006: Intel Core Duo (Yonah), Core 2 Duo (Conroe, Merom, Woodcrest)
2006: Intel fabs 80-core teraflop processor
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2005: AMD Opteron (Egypt, Italy, Denmark), Athlon 64 X2 (Manchester, Toledo)
2006: AMD Athlon 64 X2 (Windsor), Athlon Turion 64 X2 (Taylor)
Even More Cores in the Pipeline
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2007: Intel Kentsfield, Clovertown **Quad-Core CPUs**

2009: Intel Yorkfield **8-Core CPU** (45 nm)
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Multi-Core Chips are the Way of the Future!!!

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Even More Cores in the Pipeline

2007: Intel Kentsfield, Clovortown Quad-Core CPUs

2009: Intel Yorkfield 8-Core

BUT...could the INTERCONNECT stand in their way???

Greyhound, Zamora Quad-Core CPUs

2007: Sun Rock, Niagara 2 8-Core CPUs
2006 Workshop on On- and Off-Chip Interconnection Networks for Multicore Systems

Dec 6, 2006

Exploring NoC Architecture Design Space for Multicore Systems

Chita R. Das

The Pennsylvania State University
Department of Computer Science & Engineering
Talk Outline

- Motivation
- A Typical NoC Router Architecture
- The Row-Column (RoCo) Router
- Unified Buffer Organization: ViChaR
- 3D NoC Architectures
- CNT-based Interconnects
- Conclusions
The Billion Transistor Era
The Billion Transistor Era

Intel Itanium 2
(Codename Montecito)

1.7 BILLION transistors per die!
The Billion Transistor Era

- Feature sizes **diminishing RAPIDLY** into the nanometer regime

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- Transistor densities skyrocketing

![Image of Intel Itanium 2 (Codename Montecito)](Photo by Intel)

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- What about Global Wiring delays?

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- Transistor densities skyrocketing
- Gate delays are scaling down
- What about Global Wiring delays?
  - As wire cross-sections decrease, resistance INCREASES!
- Interconnects are also an issue in terms of AREA, POWER, and RELIABILITY

Photo by Intel

Intel Itanium 2
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1.7 BILLION transistors per die!
The Billion Transistor Era

- Feature sizes decreasing RAPIDLY into the nanometer regime
- Transistor density increasing
- Gate delays are decreasing
- What about Global Interconnects?
  - As wire cross-sections shrink, the resistance increases

The INTERCONNECT can no longer be ignored!

Intel Itanium 2
(Codename Montecito)
1.7 BILLION transistors per die!
Old Wine in a New Bottle…

Network Research is Old…
Old Wine in a New Bottle...

Network Research is Old...

But, Comes With Different Flavors...
Old Wine in a New Bottle...

Network Research is Old...

But, Comes With Different Flavors...

Submicron Design:

- Going Thinner... Less Reliable...
- Power Consumption Going Higher...
- Higher Integration... Getting Hotter...
Enter the Network-on-Chip (NoC)!
Enter the Network-on-Chip (NoC)!

- Replace Global Wires with a Resource-Constrained Network
Enter the Network-on-Chip (NoC)!

- Replace Global Wires with a Resource-Constrained Network
- Structured Interconnect Layout
Enter the Network-on-Chip (NoC)!

- Replace Global Wires with a Resource-Constrained Network
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- Electrical Properties OPTIMIZED and WELL CONTROLLED
Enter the Network-on-Chip (NoC)!

- Replace Global Wires with a Resource-Constrained Network
- Structured Interconnect Layout
- Electrical Properties OPTIMIZED and WELL CONTROLLED
- NoCs are like IP Blocks for Wiring!
Enter the Network-on-Chip (NoC)!
Enter the Network-on-Chip (NoC)!
What are Networks-on-Chip (NoC)?
What are Networks-on-Chip (NoC)?

Processing Elements (PEs) interconnected via a packet-based network
**What** are Networks-on-Chip (NoC)?

Processing Elements (PEs) interconnected via a **packet-based** network.

- Audio
- Video
- 802.11
- DSP
- CPU
- UART
- MPEG
- RAM
- RAM
What are Networks-on-Chip (NoC)?

Processing Elements (PEs) interconnected via a packet-based network.

Diagram depicting various elements such as Audio, Video, 802.11, DSP, CPU, UART, MPEG, RAM, and RAM, connected by a network. Each box has a NIC (Network Interface Controller) label.
What are Networks-on-Chip (NoC)?

Processing Elements (PEs) interconnected via a *packet-based* network

- Audio
- Video
- 802.11
- DSP
- CPU
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**What** are Networks-on-Chip (NoC)?

Processing Elements (PEs) interconnected via a *packet-based* network.
What are Networks-on-Chip (NoC)?

Processing Elements (PEs) interconnected via a packet-based network
What are Networks-on-Chip (NoC)?

Processing Elements (PEs) interconnected via a *packet-based* network.

Diagram showing various processing elements such as Audio, Video, 802.11, DSP, CPU, UART, MPEG, RAM, and a Processing Element (PE) with NIC.
What are Networks-on-Chip (NoC)?

Processing Elements (PEs) interconnected via a packet-based network.
Average Power Consumption in NoC Architectures

Note the contributions of: (1) Crossbar, (2) Buffers, (3) Links

RAW
- Link: 39%
- Crossbar: 30%
- Arbiter: ~0%
- Input Buffer: 31%

TRIPS
- Link: 31%
- Arbiter: 1%
- Crossbar: 33%
- Input Buffer: 35%

H.S. Wang & L.S. Peh, MICRO 2003
A Conventional NoC Router
A Conventional NoC Router

From East

VC Identifier

From West

VC 0
VC 1
VC 2

From North

VC 0
VC 1
VC 2

From South

VC 0
VC 1
VC 2

From PE

VC 0
VC 1
VC 2
A Conventional NoC Router

From East

VC Identifier

VC 0
VC 1
VC 2

From West

VC 0
VC 1
VC 2

From North

VC 0
VC 1
VC 2

From South

VC 0
VC 1
VC 2

From PE

VC 0
VC 1
VC 2

Input Port with Buffers
A Conventional NoC Router

Input Port with Buffers

From East
- VC Identifier
  - VC 0
  - VC 1
  - VC 2

From West
- VC Identifier
  - VC 0
  - VC 1
  - VC 2

From North
- VC Identifier
  - VC 0
  - VC 1
  - VC 2

From South
- VC Identifier
  - VC 0
  - VC 1
  - VC 2

From PE
- VC Identifier
  - VC 0
  - VC 1
  - VC 2

Routing Unit (RC)
VC Allocator (VA)
Switch Allocator (SA)
A Conventional NoC Router

Input Port with Buffers

Control Logic

Routing Unit (RC)
VC Allocator (VA)
Switch Allocator (SA)

From East
VC 0 → VC 1 → VC 2

From West
VC 0 → VC 1 → VC 2

From North
VC 0 → VC 1 → VC 2

From South
VC 0 → VC 1 → VC 2

From PE
VC 0 → VC 1 → VC 2
A Conventional NoC Router

VC Identifier

Input Port with Buffers

From East

VC 0
VC 1
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From South

VC 0
VC 1
VC 2

From PE

VC 0
VC 1
VC 2

Routing Unit (RC)
VC Allocator (VA)
Switch Allocator (SA)

Control Logic

Crossbar (5 x 5)

To East
To West
To North
To South
To PE
A Conventional NoC Router

Input Port with Buffers

Control Logic

Routing Unit (RC)
VC Allocator (VA)
Switch Allocator (SA)

Crossbar (5 x 5)

Crossbar

To East
To West
To North
To South
To PE
The First Design Challenge: Reduce Crossbar Complexity: **Path-Sensitive Router [DAC-05]**

- Direction vector indicates destination quadrant (SW, SE, NW, NE) including required direction (S, N, E, W).

- *Previous node* sets which of the two quadrants (NE, SE) or PE it will go to.

- Pre-Selection Mechanism in *current node* determines output port (N or E, S or E)
The Path-Sensitive Router [DAC-05]
The Row-Column (RoCo) Router [ISCA-06]
The Row-Column (RoCo) Router [ISCA-06]

- Two **Smaller, Distinct** and **Independent** modules
- Smaller Crossbars (2 2x2 instead of 1 5x5)
- Partitioned Virtual Channels
- Guided Flit Queuing
- Early Ejection Mechanism
- Maximal Matching through Mirroring-Effect
- Inherent Fault-Tolerance
- Hardware Recycling Mechanism
The RoCo Router Architecture
The RoCo Router Architecture
The RoCo Router Architecture

Guided Flit Queuing
**The RoCo Router Architecture**

**Partitioned VCs**

\[ \begin{align*}
    d_x &= \text{Continue on X} \\
    d_y &= \text{Continue on Y} \\
    t_{yx} &= \text{Turn from Y to X} \\
    t_{xy} &= \text{Turn from X to Y} \\
    \text{Inj}_{xy} &= \text{Injection into X} \\
    \text{Inj}_{yx} &= \text{Injection into Y}
\end{align*} \]
The RoCo Router Architecture
The RoCo Router Architecture
Maximal Matching with the Mirroring Effect
Maximal Matching with the Mirroring Effect

Path Sets

2x2 Crossbar

Row Module

West

East
Maximal Matching with the Mirroring Effect

Row Module

Path Sets

2x2 Crossbar

West

East

Column Module

South

North
Maximal Matching with the Mirroring Effect

Row Module
- Path Sets
- 2x2 Crossbar
  - West
  - East

Column Module
- Path Sets
- 2x2 Crossbar
  - South
  - North
Maximal Matching with the Mirroring Effect

Path Sets

2x2 Crossbar

Row Module

Conflict!

West

East

South

North

Column Module
Maximal Matching with the Mirroring Effect

Row Module

Path Sets

2x2 Crossbar

West

East

Column Module

Perfect Matching!

South

North
Maximal Matching with the Mirroring Effect

Path Sets

2x2 Crossbar

Row Module

West

East

Column Module

South

North

Perfect Matching!
Maximal Matching with the Mirroring Effect

Path Sets

2x2 Crossbar

Row Module

West

East

Column Module

South

North

Perfect Matching!
Maximal Matching with the Mirroring Effect

Path Sets

Row Module

2x2 Crossbar

West

Mirror Effect

East

Perfect Matching!

Column Module

South

Mirror Effect

North
What about Fault-Tolerance?
What about Fault-Tolerance?

- The RoCo Router has **inherent fault-tolerant** attributes due to its **DECOPLED** operation
What about Fault-Tolerance?

- The RoCo Router has inherent fault-tolerant attributes due to its DECOUPLED operation
- Two SEPARATE and INDEPENDENT modules
What about Fault-Tolerance?

- The RoCo Router has inherent fault-tolerant attributes due to its DECOUPLED operation.
- Two SEPARATE and INDEPENDENT modules.
- Only faulty module is isolated.
What about Fault-Tolerance?

- The RoCo Router has inherent fault-tolerant attributes due to its DECOUPLED operation
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- Afflicted router can still handle limited network traffic
What about Fault-Tolerance?

- The RoCo Router has inherent fault-tolerant attributes due to its DECOUPLED operation.
- Two SEPARATE and INDEPENDENT modules.
- Only faulty module is isolated.
- Afflicted router can still handle limited network traffic.
- Supports hardware recycling.
Performance Analysis:
Average Latency under Uniform Random Traffic
Performance Analysis:
Average Latency under Uniform Random Traffic

Deterministic Routing
Performance Analysis:
Average Latency under Uniform Random Traffic

![Graph showing average latency vs. injection rate for different routing methods: Generic VC Router, Path-Sensitive, and RoCo.](image)

**Deterministic Routing**

**RoCo**
Performance Analysis:
Average Latency under Uniform Random Traffic

- Generic VC Router
- Path-Sensitive
- RoCo

**Deterministic Routing**  **RoCo**  **Adaptive Routing**
Performance Analysis:
Average Latency under Uniform Random Traffic

- **Generic VC Router**
- **Path-Sensitive**
- **RoCo**

Injection Rate (flts/node/cycle)

Average Latency (cycles)

Deterministic Routing

RoCo

Adaptive Routing
Performance Analysis:
Average Latency under Uniform Random Traffic

35% (Det.) and 40% (Ad.) improvement over Generic
7% (Det.) and 4% (Ad.) improvement over Path-Sensitive

Deterministic Routing
RoCo
Adaptive Routing
Performance Analysis:
Packet Completion Probabilities in the Presence of Faults
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Packet Completion Probabilities in the Presence of Faults

- Faults injected randomly
  - Generic and Path-Sensitive: Entire node blocked
  - RoCo: Only one module blocked
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Packet Completion Probabilities in the Presence of Faults

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Deterministic Routing
Performance Analysis:
Packet Completion Probabilities in the Presence of Faults
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Higher is better!

Injection Rate in faulty network = 30%

Deterministic Routing
Performance Analysis:
Packet Completion Probabilities in the Presence of Faults

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Deterministic Routing

Adaptive Routing
Performance Analysis:
Packet Completion Probabilities in the Presence of Faults

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  - Generic and Path-Sensitive: Entire node blocked
  - RoCo: Only one module blocked

Higher is better! Injection Rate in faulty network = 30%

70% improvement with Det. Routing
7% improvement with Adapt. Routing
Performance Analysis:
Energy and PEF Metric Results
Performance Analysis:
Energy and PEF Metric Results

Lower is better!

Injection Rate in network = 30%

Energy Per Packet
Performance Analysis:
Energy and PEF Metric Results

Lower is better!

Injection Rate in network = 30%

Energy Per Packet
Performance Analysis:
Energy and PEF Metric Results

Lower is better!

Injection Rate in network = 30%

20% improvement over generic
6% improvement over Path-Sensitive

Energy Per Packet
Performance Analysis: Energy and PEF Metric Results

Injection Rate in network = 30%

RoCo

20% improvement over generic
6% improvement over Path-Sensitive

Energy Per Packet

Performance-Energy-Fault (PEF) Metric
Performance Analysis: Energy and PEF Metric Results

Lower is better!

Injection Rate in network = 30%

RoCo

20% improvement over generic
6% improvement over Path-Sensitive

Energy Per Packet

Performance-Energy-Fault (PEF) Metric
Performance Analysis: Energy and PEF Metric Results

Injection Rate in network = 30%

20% improvement over generic
6% improvement over Path-Sensitive

RoCo

50% improvement over generic
35% improvement over Path-Sensitive

Energy Per Packet

Performance-Energy-Fault (PEF) Metric
The Second Design Challenge: The NoC buffers

- The NoC Buffers **DOMINATE** the **Area** and **Power** budgets of the router!
- Any improvements in the on-chip buffers will yield significant benefits in the overall interconnect system.
- Existing on-chip buffer solutions suffer from a number of crippling limitations (such as Head-of-Line Blocking and Underutilization)
The Second Design Challenge: The NoC buffers

Solution:

ViChaR: A Dynamic Virtual Channel Regulator for Network-on-Chip Routers

To appear at the 39th Annual International Symposium on Microarchitecture (MICRO)
December 2006
ViChaR: A Dynamic Virtual Channel Regulator for NoC Routers

- ViChaR’s operation revolves around two fundamental concepts:
  - ViChaR uses a Unified Buffer Structure (UBS)
  - ViChaR provides each individual router port with a variable number of VCs
ViChaR: A Dynamic Virtual Channel Regulator for NoC Routers

ViChaR’s operation revolves around two fundamental concepts:

- ViChaR uses a Unified Buffer Structure (UBS)
- ViChaR provides each individual router port with a variable number of VCs
ViChar – Average Latency
ViChaR – Average Latency

GEN = Generic Router
ViC = ViChaR Router
NR = Normal Random (Source-Destination Selection)
TN = Tornado (Source-Destination Selection)
UR = Uniform Random Traffic

Average Latency (Deterministic Routing)
ViChaR – Average Latency

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Average Latency (Deterministic Routing)
ViChaR – Average Latency

GEN = Generic Router
ViC = ViChaR Router
NR = Normal Random (Source-Destination Selection)
TN = Tornado (Source-Destination Selection)
UR = Uniform Random Traffic

~30% Improvement (Deterministic Routing)
~25% Improvement (Minimal Adaptive Routing)
over a Conventional Router
ViChaR – Average Latency
ViChaR – Average Latency

Average Latency (Deterministic Routing)
ViChaR – Average Latency

Average Latency (Deterministic Routing)
ViChaR – Average Latency

Average Latency (Deterministic Routing)

- ViChaR's efficiency allows us to *halve the buffer resources with no discernible effect on performance.*
ViChaR – Power Improvements
ViChaR – Power Improvements
For equally sized configurations, ViChaR consumes slightly more power than a conventional buffer structure (GEN-16 vs. ViC-16).
For equally sized configurations, ViChaR consumes slightly more power than a conventional buffer structure (GEN-16 vs. ViC-16).

However, since ViChaR's efficiency allows us to halve the buffer resources with no discernible effect on performance, the overall power drops by about 34% (GEN-16 vs. ViC-8) for equivalent performance.
The Third Design Challenge: Reducing Wire Length
The Third Design Challenge: Reducing Wire Length

- Three-dimensional integration (3D IC) is an attractive option for interconnect scaling.
The Third Design Challenge: Reducing Wire Length

- **Three-dimensional integration** (3D IC) is an attractive option for interconnect scaling.
- **Direct vertical tunnel** reduces global interconnects.
The Third Design Challenge: Reducing Wire Length

- **Three-dimensional integration (3D IC)** is an attractive option for interconnect scaling.
- **Direct vertical tunnel** reduces global interconnects.
- A combination of the 3D technology and **NoC** design can be used to provide scalable and efficient on-chip networks.
A 3D Symmetric NoC Architecture

Simplest Extension to the Baseline NoC Router to facilitate a 3D layout:

- 3D Symmetric NoC Architecture
- **Hop-by-Hop traversal**: implemented by 2D Crossbar.
3D NoC-Bus Hybrid Architecture

Hybridized with a bus link in the vertical dimension: Given the very small inter-strata distance, single hop communication is feasible.
A Full 3D NoC Router

Vertical Links are embedded in 3D crossbar switch:

- **Seamless integration** of the vertical links in a single router operation.
- **Multiple internal paths** and no intermediate buffers – go through a couple of crossbar switching points and directly connect to the output port of the destination layer.
Inter-Layer Via Structure in a 3D Crossbar Technology

3D connection box can facilitate linkage between vertical and horizontal channels, and vertical pillars are segmented for flexible flit traversal.
DimDe: A Dimensionally-Decomposed 3D NoC Router Architecture

Full 3D crossbar requires complex arbitration and enormous number of vertical links and control signals.
DimDe Router (Contd.)

Partially-connected 3D crossbar structure (two pillars)

* Top View
Performance Evaluation with Workload Traces

Average Latency with various Commercial and Scientific Workloads

Energy-Delay Product (EDP) with various Commercial and Scientific Workloads
Performance Evaluation with Workload Traces

Average 27% Latency Gain over all designs except Full 3D Crossbar (and within 4% of Full 3D Crossbar)

Average Latency with various Commercial and Scientific Workloads

Energy-Delay Product (EDP) with various Commercial and Scientific Workloads
Performance Evaluation with Workload Traces

**Average 27% Latency Gain** over all designs except Full 3D Crossbar (and within 4% of Full 3D Crossbar)

Average Latency with various Commercial and Scientific Workloads

**Average 26% Improvement** *(Energy-Delay Product (EDP))* over all other 3D Routers

Energy-Delay Product (EDP) with various Commercial and Scientific Workloads
Looking into Future: CNT-based Interconnects?

*IBM has announced that its researchers have built the first complete electronic integrated circuit around a single “carbon nanotube” molecule, a new material that shows promise for providing enhanced performance over today’s standard silicon semiconductors.*

“Carbon nanotube transistors have the potential to outperform state-of-the-art silicon devices,” said Dr. T.C. Chen, vice president, Science & Technology, IBM Research.

“Intel is eyeing carbon nanotubes as a possible replacement for copper wires inside semiconductors, a switch that one day could eliminate some big problems for chipmakers.” CNET News
CNT - An Interconnect Medium?

- High current carrying capacity: Reported Current densities of $10^5$ A/cm$^2$, 1000 times more than copper

- Higher reliability against electromagnetic failures

- Higher signal integrity, less cross-talk issues

- Higher thermal conductivity can help mitigate thermal issues

- High contact resistance – can be solved by using parallel bundles of SWCNTs
CNT - An Interconnect Medium?

- **High current carrying capacity**: Reported Current Density 10^7 A/cm²

  How will these affect NoC Design Decisions?
  Will Hybrid Cu-CNT interconnects be attractive?
  Can CNT-3D technologies combine to offer new benefits?

- **High contact resistance** – can be solved by using parallel bundles of SWCNTs

  thermal issues
Summarizing Our NoC Research
Research Group

Faculty:
Chita R. Das
Vijaykrishnan Narayanan
Yuan Xie

Graduate Students:
Jongman Kim      Chrysostomos Nicopoulos
Dongkook Park    Reetuparna Das

Collaborators:
Intel, IBM, Xilinx, AMD
Univ. of Bologna
Rice University
Conclusions

- On-chip interconnects will play a significant role in designing next generation multicore architectures.
- A holistic approach considering performance, energy, reliability and thermal issues is essential in designing NoC architectures.
- Development of accurate performance, energy, reliability, thermal models/tools for NoC is necessary.
- The proposed RoCo and 3D routers seem quite promising.
- 3D and CNT-based designs are under progress.
Thank You!