

Contact Information

ACSEL Laboratory
Electrical and Computer Engineering Department
University of California, Davis
One Shields Avenue, Davis, CA 95616

Cell Phone: (914)584-0709
Work Phone: (530)752-6800
Home Phone: (530)759-8757
Fax: (530)752-6800

Email: milena@acsel-lab.com
URL: <http://www.ece.ucdavis.edu/~milena/>

Education

Ph.D. candidate in Electrical Engineering and Computer Sciences
University of California, Davis

September 2003 - present
Expected graduation: 2009.

Research:

- Power-performance modeling methodology for high-performance microprocessors
- Framework for the circuit and micro-architectural level power-performance optimization
- Architecture-Circuit space exploration for balanced co-design in the power-performance tradeoff analysis

Research advisor: Prof. Vojin G. Oklobdzija

Research Scholar
University of California, Davis
ACSEL Laboratory

March – September 2003.

I have joined ACSEL Laboratory at UC-Davis initially as a Research Scholar. During this period, I have performed early analysis and optimization of arithmetic units for low-power. Afterwards, I have continued as a PhD student.

B. S. in Electrical Engineering
University of Belgrade, Yugoslavia, School of Electrical Engineering

October 1997 – March 2003.

Graduated with honors

Professional Experience

Research Assistant
University of California, Davis

September 2003 - present

PhD research topic: Power-Aware Microprocessor Design

The main research objective of my thesis is development of new strategies and design guidelines for efficient power-management control in microprocessor design. Using power-performance modeling methodology, impact of different architectural modifications can be analyzed early in the design stage. However, micro-architectural optimization and analysis cannot be performed solely and in isolation, i.e. without taking into the account the impact of the architectural decisions on the underlying circuit-level counterparts. Exploration in the architecture-circuit space, co-design and balancing at both micro-architectural and circuit levels simultaneously is necessary for efficient microprocessor design.

Summer Internship
IBM, T. J. Watson Research Center, Yorktown Heights, NY

April – November 2006.

Reliability and Power-Aware Microarchitectures Group
Manager: Dr. Pradip Bose, Mentor: Dr. Victor Zyuban

During my internship, I worked on power modeling for new generation high-performance low-power microprocessors.

Research Staff Member
Siemens, Vienna, Austria

March – September 2002.

For my undergraduate thesis project, I have developed an architectural organization for next-generation Voice over IP (VoIP) processor. The processor was aimed to enable a new compelling class of multimedia applications and supports real-time performance. Now it is being used as part of VoIP products in Siemens Company.

The project was called:

RTP GAME: Real Time Protocol – Generator And Modifier of Environment

Publications

- **“Circuit Sizing and Supply-Voltage Selection for Low-Power Digital Circuit Design”**
M. Vratonjic, B. R. Zeydel, V. G. Oklobdzija
16th Int. Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)
Montpellier, France, Sept. 13-15, 2006.
 - **“Low- and Ultra Low-Power Arithmetic Units: Design and Comparison”**
M. Vratonjic, B. R. Zeydel, V. G. Oklobdzija
Int. Conference on Computer Design (ICCD)
San Jose, California, Oct. 2-5, 2005.
 - **“Exploratory Designs for Low- and Ultra Low-Power Applications”**
M. Vratonjic, B. R. Zeydel, V. G. Oklobdzija
TECHCON, Semiconductor Research Corp.
Portland, Oregon, Oct. 24-26, 2005.
 - **“Low-Power Aspects of Different Adder Topologies”**
M. Vratonjic, B. R. Zeydel, V. G. Oklobdzija
37th Annual Asilomar Conference on Signals, Systems and Computers
Pacific Grove, California, Nov. 9-12, 2003.
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Awards

- Summer Research Assistantship Award, University of California 2005, 2004
 - Award for Excellent Academic Performance and Accomplishments,
from Royal Norwegian Embassy 2002
 - Award for Exceptional Undergraduate Accomplishments,
University of Belgrade, Yugoslavia 2002
 - Fellowship from Serbian Ministry of Education,
Foundation for Young Artists and Scientists 2001
 - Scholarship from Engineering Society Pavle Savic,
Serbian Academy of Sciences and Arts 1998
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Skills

- **Software:** SimpleScalar Simulator, Cadence Composer, HSPICE, MATLAB
 - **Programming:** Perl/Shell scripting, Verilog, C/C++
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References

Prof. Vojin G. Oklobdzija, ACSEL Laboratory Director (vojin@acsel-lab.com)
Prof. Vladimir M. Stojanovic, MIT (vlada@mit.edu)