

## Marko Aleksić

Department of Electrical and Computer Engineering  
University of California,  
One Shields Ave., Davis, CA 95616, USA  
Tel.: (530) 752-6347  
E-mail: [maleksic@ece.ucdavis.edu](mailto:maleksic@ece.ucdavis.edu)  
URL: <http://www.ece.ucdavis.edu/~maleksic>

### RESEARCH INTERESTS

- Design of integrated circuits for high-performance and low-power systems
- Noise analysis of integrated circuits

### EDUCATION

**Ph.D. in Electrical Engineering (in progress)**, University of California, Davis. Advanced to candidacy Mar '04. Expected graduation time: Dec '06. Dissertation title: *Jitter Analysis of Non-Autonomous MOS Current-Mode Logic Circuits*. Advisors: Prof. K. Wayne Current and Prof. Vojin G. Oklobdžija.

**M.S. in Electrical Engineering**, University of California, Davis, Mar '04. Project: *Jitter Analysis of Current-Mode Logic Frequency Dividers*. Advisors: K. W. Current and V. G. Oklobdžija.

**Dipl.Ing. in Electrical Engineering**, University of Belgrade, Serbia, Sep 2000. Thesis title: *Serial CORDIC Computer*. Advisor: Prof. Slavoljub Marjanović.

### EXPERIENCE

**Graduate Student Researcher** at the ECE Dept., UC Davis (Fall '01–present) on projects:

- Analysis of jitter in MOS current-mode logic circuits (Fall '02–present), under Prof. K. Wayne Current and Prof. Vojin G. Oklobdžija
- Behavioral modeling and high-level optimization of mixed-signal ICs, under Prof. K. W. Current (Winter '03–Spring '04)
- Design and analysis of flip-flops and latches for high-performance microprocessors, under Prof. V. G. Oklobdžija (Fall '01–Fall '02)

**Summer Intern** at Fujitsu Labs of America, under the supervision of William W. Walker (summers of '02, '03, '04 and '05). The work involved:

- Jitter analysis of RF circuits
- Device modeling
- Design of ICs for RF frequency synthesizers
- High-level modeling of communication systems
- Noise analysis of RF ICs
- RF measurements

**Assistant Instructor** at the ECE Dept., UC Davis. Taught three upper division courses: Electronic Circuits and Systems, Electronic Circuits I, and Electronic Circuits II, in Summer '06, Winter '05, and Fall '03, respectively.

**Teaching Assistant** (Fall '01–present) for lower and upper division courses at the ECE Dept., UC Davis: Electronic Circuits and Systems (Spring '06), Circuits I (for 3 quarters '05–'06), Digital Systems I (for 5 quarters '01–'04), Assembly Language Programming (Fall '04), and Microcomputer-Based System Design (Fall '02).

**Post Graduate Researcher** (visiting scholar) at the ECE Dept., UC Davis, under Prof. Vojin G. Oklobdžija (Fall 2000–Fall '01). The work involved design and analysis of flip-flops and latches, and analysis of different clocking schemes for high-performance, low-power microprocessors.

## PUBLICATIONS

- M. Aleksić, N. Nedovic, K. W. Current and V. G. Oklobdzija, “*A New Model for Timing Jitter Caused by Device Noise in Current-Mode Logic Frequency Dividers*”, Proceedings of the 15th International Workshop on Power And Timing Modeling, Optimization and Simulation, PATMOS, Leuven, Belgium, September 21-23, 2005.
- N. Nedovic, W. W. Walker, V. G. Oklobdzija and M. Aleksić, “*A Low Power Symmetrically Pulsed Dual Edge-Triggered Flip-Flop*”, Proceedings of the 28th European Solid-State Circuits Conference, Florence, Italy, September 24-26, 2002.
- N. Nedovic, M. Aleksić and V. G. Oklobdzija, “*Conditional Pre-Charge Techniques for Power-Efficient Dual-Edge Clocking*”, Proceedings of the International Symposium on Low-Power Electronics and Design, Monterey, California, August 12-14, 2002.
- N. Nedovic, M. Aleksić and V. G. Oklobdzija, “*Comparative Analysis of Double-Edge versus Single-Edge Triggered Clocked Storage Elements*”, 2002 IEEE International Symposium on Circuits and Systems, Scottsdale, Arizona, May 26-29, 2002.
- N. Nedovic, M. Aleksić and V. G. Oklobdzija, “*Timing Characterization of Dual-Edge Triggered Flip-Flops*”, Proceedings of the International Conference on Computer Design, ICCD 2001, Austin, Texas, September 23-26, 2001.
- N. Nedovic, M. Aleksić and V. G. Oklobdzija, “*Conditional Techniques for Small Power Consumption Flip-Flops*”, Proceedings of the 8th IEEE International Conference on Electronics and Systems, Malta, September 2-5, 2001.

## SKILLS

**Computer Skills:** HSPICE, Cadence, MATLAB, C/C++, Perl

**Languages:** English, Serbian, Russian, basic Spanish

## MEMBERSHIPS

IEEE and Solid-State Circuits Society Student Member since 2001

## REFERENCES

Available upon request