

A New Model for Timing Jitter Caused by Device Noise in Current-Mode Logic Frequency Dividers

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Abstract. A new method for predicting timing jitter caused by device noise in current-mode logic (CML) frequency dividers is presented. Device noise transformation into jitter is modeled as a linear time-varying (LTV) process, as opposed to a previously published method, which models jitter generation as a linear time-invariant (LTI) process. Predictions obtained using the LTV method match jitter values obtained through exhaustive simulation with an error of up to 7.7 %, whereas errors of the jitter predicted by the LTI method exceed 57 %.

1 Introduction

Timing jitter (or phase noise, if observed in the frequency domain) is a major constraint in modern high-speed communication systems. Jitter imposes limitations to the maximum signaling rate for which the bit error rate (BER) does not exceed its maximum acceptable level, the minimum spacing between channels in order to avoid inter-channel interference, etc. Unfortunately, jitter does not scale down with the signal period. As the signaling rates increase and are now in the range of tens of Gbps, even small amounts of jitter can severely impair the performance of these systems.

It would be very desirable to know the amount of jitter that will be caused by device noise of circuits in a system before the system is actually fabricated. This way, it would be possible to determine whether the system meets the requirements in the pre-fabrication phase of the design process, and hence, reduce the cost of the design. For that reason, a lot of research has been done on jitter and phase noise analysis of different circuits constituting precise frequency synthesizers, namely phase-locked loops (PLLs). Most of this research targeted voltage-controlled oscillators (VCOs) and several different theories emerged for predicting VCO jitter and phase noise, [1], [2], [3]. However, oscillators are not the only source of jitter in a PLL. As shown in [4], phase noise caused by the frequency divider, which is an integral part of every high-frequency PLL, can be amplified by the loop and occur at the PLL output, degrading performance of the subsequent circuitry. Beside PLLs, frequency dividers can also be found in multi-phase clock generators, multiplexers and demultiplexers of high-speed front-ends, etc. Therefore, there is an evident need for studying the jitter of frequency dividers.

Before we start analyzing jitter, it needs to be defined: jitter is a variation of the signal period from its nominal value. It is caused by various factors such as power

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supply noise, substrate noise, cross-talk etc. In the analysis presented here, only jitter caused by the circuit device noise will be studied. The effects of other sources of jitter can be minimized through the circuit design (e.g. differential circuits are resistant to power supply noise) or technological process (e.g. circuits fabricated in a triple-well process are resistant to substrate noise). Since it is caused by random processes, jitter itself is a random process and is described by its variance or root-mean-square (RMS) value, rather than its instantaneous value.

Until recently, the only reliable way to predict jitter of frequency dividers was through exhaustive simulation. Several models for frequency divider jitter and phase noise were proposed, [5], [6], but these were based on experimental results and could not be applied to circuits other than those described in the studies. Even though empirical, model described in [5] revealed some properties of frequency divider jitter that can be used to simplify the analysis. Since multi-stage frequency dividers are often implemented as asynchronous counters, total jitter at the output of a multi-stage divider is the sum of jitters of each stage. Therefore, stages can be analyzed only one at a time. The first analytical model was proposed in [7]. This model was an application of a VCO jitter model described in [1] to a current-mode logic (CML) frequency divider, and it models generation of jitter as a linear time-invariant (LTI) process.

The work presented in this paper proposes a new way of modeling the process of device noise transformation into jitter in CML frequency dividers. The focus is on CML circuits since that is the usual design technique of choice in high-speed systems. Jitter generation is modeled as a linear time-varying (LTV) process and the model achieves more accurate predictions than the LTI model.

2 CML Frequency Divider Circuit Design

As will be shown shortly, jitter generation of a circuit is closely related to the circuit topology and output waveforms. For that reason, Fig. 1 shows a block-diagram of a CML frequency divider-by-two. It consists of a master-slave latch connected as a T-flip-flop and a level-shifter. Transistor-level schematics of the latch and the level-shifter are given in Fig. 2. The circuit was implemented in a triple-well process by Fujitsu, with the minimum channel length of 110 nm and a power supply voltage $V_{DD} = 1.2$ V. Maximum frequency of the input signal for which the circuit still operates properly is 10 GHz. CML design technique employs low-swing differential-voltage signaling and in this case, circuits were designed for a nominal output swing of 300 mV. Waveforms of the master-slave latch and the level-shifter output voltages around the switching time are given in Fig. 3. Active (rising) edge of the input signal (v_{in} in Fig. 1) arrives at $t = 0$ in Fig. 3. For all the following considerations, it will be assumed that the input signal is perfect and does not contain any jitter.

3 The LTI Frequency Divider Jitter Model [7]

According to the model proposed in [7], noise can affect the output crossing time only around the nominal crossing time. Then, variance of the output jitter is equal to the variance of the output-referred voltage device noise, multiplied by the inverse of the squared derivative of the differential output voltage at the nominal crossing time:

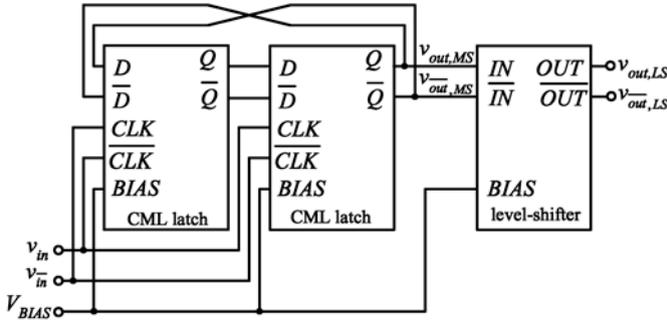


Fig. 1. Block diagram of a CML frequency divider-by-two

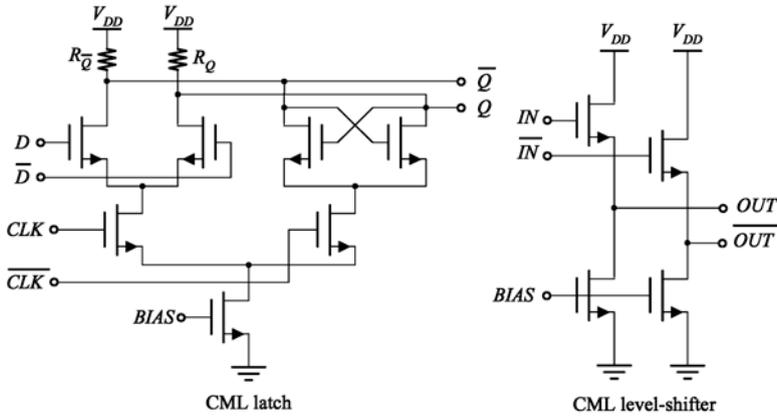


Fig. 2. Transistor-level schematics of the CML latch and the level-shifter

$$\sigma_T^2 = \left[\frac{\partial(v_{out} - v_{out}^-)}{\partial t} \right]_{@t_x}^{-2} \times \sigma_{v_n}^2 \tag{1}$$

In case of a CML frequency divider, variance of jitter at the output will be equal to the sum of variances of the master-slave latch jitter and the level-shifter jitter, assuming that noise sources in the latch and the level-shifter are uncorrelated:

$$\sigma_{T,tot}^2 = \left[\frac{\partial(v_{out,MS} - v_{out,MS}^-)}{\partial t} \right]_{@t_x,MS}^{-2} \times \sigma_{v_n,MS}^2 + \left[\frac{\partial(v_{out,LS} - v_{out,LS}^-)}{\partial t} \right]_{@t_x,LS}^{-2} \times \sigma_{v_n,LS}^2 \tag{2}$$

Since the circuits are differential, there are noise sources at both outputs. Assuming that these noise sources are mutually uncorrelated, total jitter variance will be double the value given in (2):

$$\sigma_{T,tot}^2 = 2 \times \left\{ \left[\frac{\partial(v_{out,MS} - v_{out,MS}^-)}{\partial t} \right]_{@t_x,MS}^{-2} \times \sigma_{v_n,MS}^2 + \left[\frac{\partial(v_{out,LS} - v_{out,LS}^-)}{\partial t} \right]_{@t_x,LS}^{-2} \times \sigma_{v_n,LS}^2 \right\} \tag{3}$$

Jitter RMS value is found as the square-root of the variance given in (3), i.e. $\sigma_{T,tot}$.

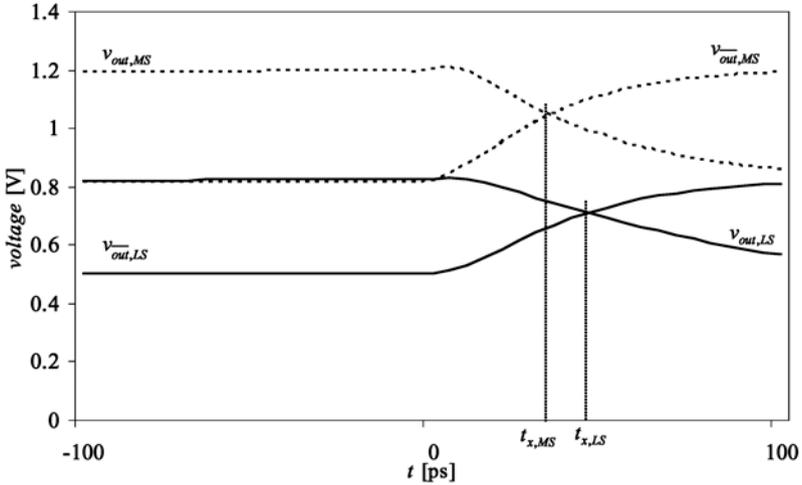


Fig. 3. Output voltages of the master-slave latch and the level-shifter

According to (1), impulse response function of an abstract system that converts device noise into jitter can be defined as:

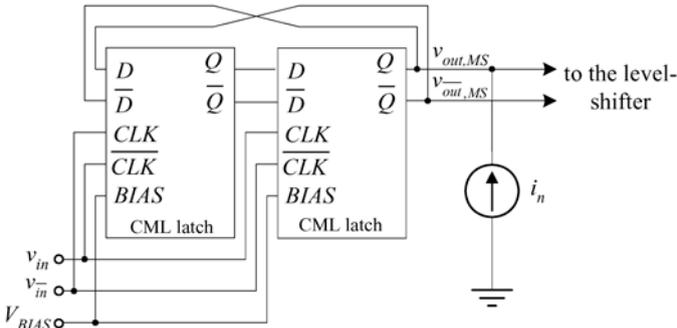


Fig. 4. Setup for determining the impulse sensitivity function (ISF) of the master-slave latch

$$h(t) = \left[\frac{\partial(v_{out} - v_{out}^-)}{\partial t} \right]_{@t_x}^{-1} \times \delta(t) , \tag{4}$$

where $\delta(t)$ is the Dirac impulse. The system defined by (4) is a linear time-invariant (LTI) system, since its response does not depend on the occurrence time of the input (i.e. noise, in this case).

4 The Proposed LTV Jitter Model

Frequency divider jitter model proposed here was inspired by the oscillator phase noise model presented recently in [2], even though representation of electric oscillators as linear time-varying systems for noise was known even in the late 1960s [8].

One important difference between the model from [2] and the model proposed here is that the model in [2] is linear periodically time-varying, whereas the model presented here is aperiodic. Unlike oscillators which are autonomous circuits, frequency dividers are driven circuits and their jitter does not accumulate with time, since the timing is reset with each occurrence of the input. Therefore, variation of the output crossing time in one cycle is caused by device noise during that cycle only, and jitter generation can be represented as an aperiodic process.

To start with the analysis, observe the waveform of the master-slave latch output, $v_{out,MS}$ in Fig. 3. Assume that the output-referred device noise of the master-slave latch can be represented by a current source connected to the latch output node, i_n in Fig. 4. (To be more precise, this noise source needs to include only device noise originating from the slave latch, since the master latch outputs are stable at the time when the slave latch outputs are switching. Therefore, master latch noise cannot affect jitter of the slave latch output and this was also recognized in [7].) Now, assume that source i_n is a unit impulse that occurs at time $t = \tau$, $i_n = \delta(t - \tau)$. The current impulse injects 1 C of electric charge at the latch output node, which causes an abrupt increase of voltage $v_{out,MS}$ at time $t = \tau$. The effects of charge injection will diminish with time, but will also affect the crossing time of the master-slave latch outputs. Naturally, if the impulse occurs after the nominal crossing time (i.e. $\tau > t_{x,MS}$) charge injection will not cause any crossing time variation. It is possible to define a function that shows the dependence of the crossing time variation on the impulse arrival time, τ . This function is called the impulse sensitivity function (ISF), $\Gamma(\tau)$, and is shown in Fig. 5 for both master-slave latch and the level shifter ($\Gamma_{MS}(\tau)$ and $\Gamma_{LS}(\tau)$ respectively). The ISFs in Fig. 5 show that, the closer the impulse arrival time to the nominal crossing time, the larger the effects of charge injection on the crossing time variation.

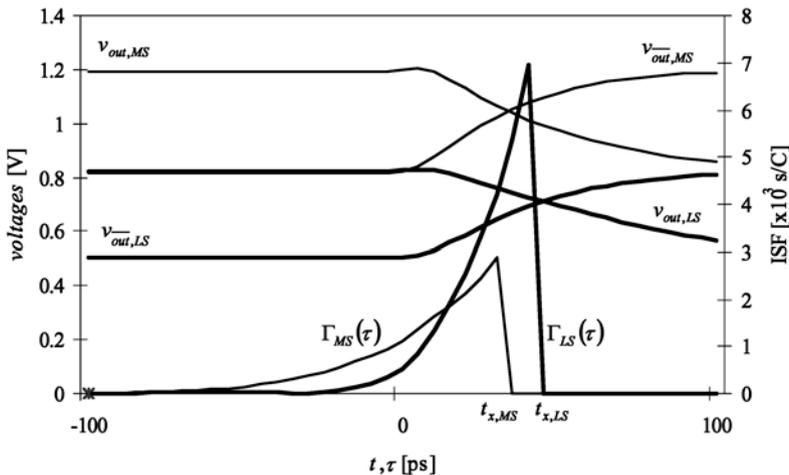


Fig. 5. ISFs of the master-slave latch and the level-shifter ($\Gamma_{MS}(\tau)$ and $\Gamma_{LS}(\tau)$, respectively)

Once $\Gamma(\tau)$ is known, we can define the impulse response function of the noise-to-jitter conversion system, $h(t, \tau)$:

$$h(t, \tau) = \Gamma(\tau) \times u(t - \tau) , \quad (5)$$

where $u(t)$ is the unit step function. Now it is obvious that this system is an LTV system, since its response depends on the impulse arrival time.

The response of an LTV system to an input signal $x(t)$ is given by the convolution integral:

$$y(t) = \int_{-\infty}^{+\infty} h(t, \tau) x(\tau) d\tau . \quad (6)$$

If the input to the system is a random process whose autocorrelation function is given by $R_X(t, \xi)$, autocorrelation of the resulting random process, at the output of the LTV system, $R_Y(t, \xi)$, will be [9]:

$$R_Y(t, \xi) = \int_{-\infty}^{+\infty} \int_{-\infty}^{+\infty} h(t, r) h(\xi, s) R_X(r, s) dr ds . \quad (7)$$

To demonstrate the proposed LTV model for the noise-to-jitter conversion, we will assume that the output-referred noise of the slave latch (i_n in Fig. 4) is white and has a RMS value $\sigma_{n,MS}$. Then, the autocorrelation function, $R_{n,MS}(t, \xi)$, of that noise source is:

$$R_{n,MS}(t, \xi) = \sigma_{n,MS}^2 \times \delta(t - \xi) . \quad (8)$$

Combining (5), (7) and (8), with $\Gamma(\tau) = \Gamma_{MS}(\tau)$ and $R_X(t, \xi) = R_{n,MS}(t, \xi)$, it can be shown that the autocorrelation of the output random process (i.e. master-slave latch jitter), $R_{T,MS}(t, \xi)$, is given by the following expression:

$$R_{T,MS}(t, \xi) = \sigma_{n,MS}^2 \times \int_{-\infty}^{\min\{t, \xi\}} \Gamma_{MS}^2(s) ds . \quad (9)$$

Since the output random process is jitter (i.e. crossing time variation), it would be natural to evaluate (9) at the nominal crossing time, $t = t_{x,MS}$. In addition, variance of a random process is given as the autocorrelation function $R_X(t, \xi)$ for $t = \xi$. Hence, variance of the master-slave latch jitter will be equal to $R_{T,MS}(t_{x,MS}, t_{x,MS})$:

$$\sigma_{T,MS}^2 = R_{T,MS}(t_{x,MS}, t_{x,MS}) = \sigma_{n,MS}^2 \times \int_{-\infty}^{t_{x,MS}} \Gamma_{MS}^2(s) ds . \quad (10)$$

Note that evaluating (10) at a time instant $t > t_{x,MS}$ will not change the result, since $\Gamma_{MS}(s) = 0$ for $s > t_{x,MS}$, which is shown in Fig. 5.

Equation (10) does not give the total variance of the master-slave latch jitter. Remember that another noise source exists at the other output of the master-slave latch, which will also affect the output crossing time. We will assume that the RMS value of this noise source is also $\sigma_{n,MS}$ and that the cross-correlation between the noise sources at the two outputs is zero. In addition we will assume that the rising and falling edges of the master-slave output signal are symmetrical, hence, ISFs of both outputs of the master-slave latch are the same. Under these assumptions, total variance of the master-slave output jitter is double the value given in (10).

Similar analysis can be conducted for jitter caused by the level-shifter device noise. In this case, a relationship similar to (10) can be derived, but using the level-shifter

ISF, $\Gamma_{LS}(\tau)$, and the RMS value of the level-shifter output-referred device noise, $\sigma_{n,MS}$. (Again, it will be assumed that the noise is white.) Also, in this case, jitter is evaluated at the nominal crossing time of the level-shifter outputs, $t_{x,LS}$.

Finally, if noise sources in the master-slave latch and the level-shifter are not correlated, the total jitter variance of the CML frequency divider-by-two is given by the following expression:

$$\sigma_{T,tot}^2 = 2 \times \left[\left(\sigma_{n,MS}^2 \times \int_{-\infty}^{t_{x,MS}} \Gamma_{MS}^2(s) ds \right) + \left(\sigma_{n,LS}^2 \times \int_{-\infty}^{t_{x,LS}} \Gamma_{LS}^2(s) ds \right) \right] \quad (11)$$

Total jitter RMS value is given as the square-root of the variance in (11).

5 Comparison of the Two Jitter Models

The LTI and the LTV jitter models were used to predict jitter of the one-stage CML frequency divider from Fig. 1 and 2. The predictions were compared against jitter results obtained through exhaustive simulation in HSPICE. In all three cases, output-referred noise was white, and the RMS values of noise at each output of the master-slave latch and the level-shifter were $\sigma_{n,MS} = 1.61 \times 10^{-12}$ A and $\sigma_{n,LS} = 1.73 \times 10^{-12}$ A, respectively. These values were determined using the NOISE analysis in HSPICE, with DC conditions that are equal to the instantaneous voltages and currents at the moments when the master-slave latch and the level-shifter outputs are crossing, $t_{x,MS}$ and $t_{x,LS}$.

For the LTI model, derivatives of the output voltages were obtained through simulation in HSPICE, using the DERIVATIVE function in the MEASURE statement. Variances of the output-referred voltage noise sources were calculated using the following relationships:

$$\begin{aligned} \sigma_{Vn,MS}^2 &= \int \sigma_{n,MS}^2 |Z_{MS}(f)|^2 df \\ \sigma_{Vn,LS}^2 &= \int \sigma_{n,LS}^2 |Z_{LS}(f)|^2 df \end{aligned} \quad (12)$$

where $Z_{MS}(f)$ and $Z_{LS}(f)$ are output impedances of the master-slave latch and the level-shifter, which were obtained in HSPICE. Finally, jitter was found using (3).

For the LTV model, ISFs of the master-slave latch and the level-shifter were found in HSPICE in the following manner: a charge was injected via a short current impulse, while changes of the output crossing times were measured for different impulse arrival times. (The ISFs shown in Fig. 5 were obtained this way.) Nominal crossing times $t_{x,MS}$ and $t_{x,LS}$ were also found in HSPICE. Finally, jitter was calculated using (11).

To compare the accuracy of the LTI and the LTV jitter models, jitter values obtained through exhaustive transient simulation in HSPICE were used. However, in the HSPICE transient analysis, it is not possible to specify noise sources. Therefore, device noise from the master-slave latch and the level-shifter was simulated by four piecewise linear (PWL) current sources connected to the outputs of the circuits. Instantaneous values of these sources were determined using a random number generator in MATLAB, while keeping their RMS values equal to $\sigma_{n,MS}$ for the sources at the master-slave latch outputs, and $\sigma_{n,LS}$ for the sources at the level-shifter outputs. Time

step of the PWL sources was small enough so that the power spectral density of the sources was white over the bandwidth of interest. The four PWL sources were mutually uncorrelated, which was verified in MATLAB. Finally, the transient analysis was run for 100 periods of the frequency divider output signal, and variations of the crossing times of the outputs were recorded. Simulation time was over 24 hours. In contrast, time needed to obtain data for the LTI and the LTV model from HSPICE was in the range from a few minutes for NOISE analyses to an hour for determining the ISFs for the LTV model.

The results are summarized in Table 1. Jitter values are given for three cases of the biasing current: case 1 is the nominal value, case 2 is a value 20 % less than nominal, and case 3 is a value 20 % greater than nominal. Last two columns in Table 1 show relative errors of the jitter values predicted by the LTV and the LTI models, with respect to the values obtained through the exhaustive HSPICE simulation.

It can be seen from Table 1 that the new LTV model gives jitter predictions which are much closer to the values obtained through exhaustive simulation. The reason for this is that the LTV model integrates effects of noise prior and at the crossing time, while the LTI model evaluates effects of noise only at the nominal crossing time and hence predicts jitter values which are smaller than the actual ones.

6 Conclusions

A new method for predicting jitter caused by device noise in current-mode logic (CML) frequency dividers is presented. As opposed to a previously published method, the new method models device noise transformation into jitter as a linear-time-varying (LTV) process. Predictions of the LTV model match jitter values obtained through exhaustive simulation with an error of up to 7.7 %. In contrast, error of the predictions obtained by the previously published method exceeds 57 %.

In this work, the new jitter model was demonstrated for CML frequency dividers and white noise only. However, the method is not limited to this case. As long as the impulse sensitivity function (ISF) of a circuit and the autocorrelation function of the output-referred noise are known, the LTV jitter model formulated in (11) can be used to estimate jitter.

Table 1. Comparison of the LTI and the LTV jitter models with exhaustive simulation

	Exhaustive simulation $\sigma_{T,tot}$ [fs]	LTV model (this work) $\sigma_{T,tot}$ [fs]	LTI model [7] $\sigma_{T,tot}$ [fs]	Error LTV [%]	Error LTI [%]
case 1	62.2	65.9	26.6	5.9	57.3
case 2	82.8	89.2	36.0	7.7	56.5
case 3	48.8	52.5	21.6	7.7	55.7

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