Early Monolithic Pipelined ADCs

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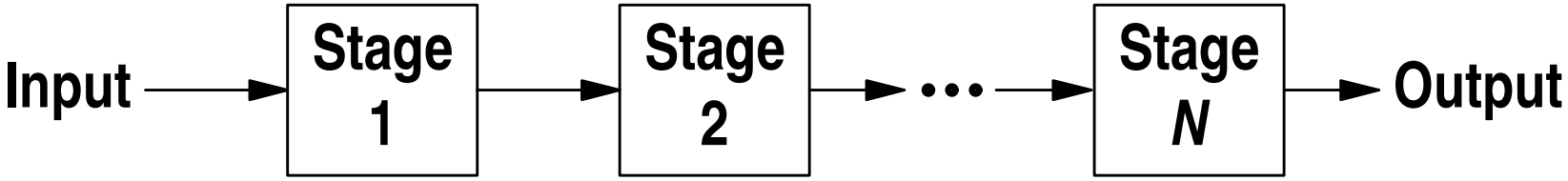
Pipelining



- Break a repetitive job into sequential stages
- When full, pipelines are fast
- Each stage can be optimized for the job it does
- All outputs come through the same path
- The same concept as in assembly lines

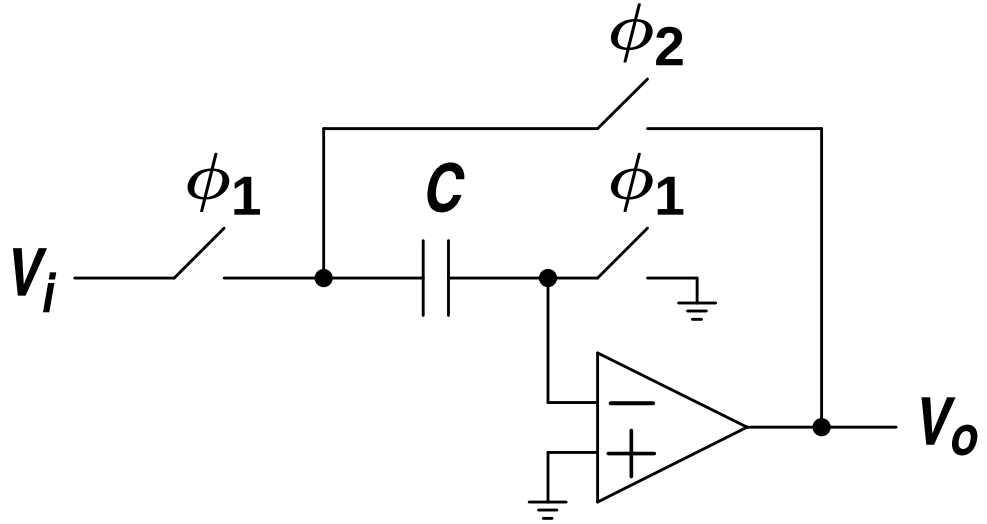
Pipelined ADC Concept

- Gordon, TCAS, 7/78

  Jepperson, US Patent #3,119,105, 1/64

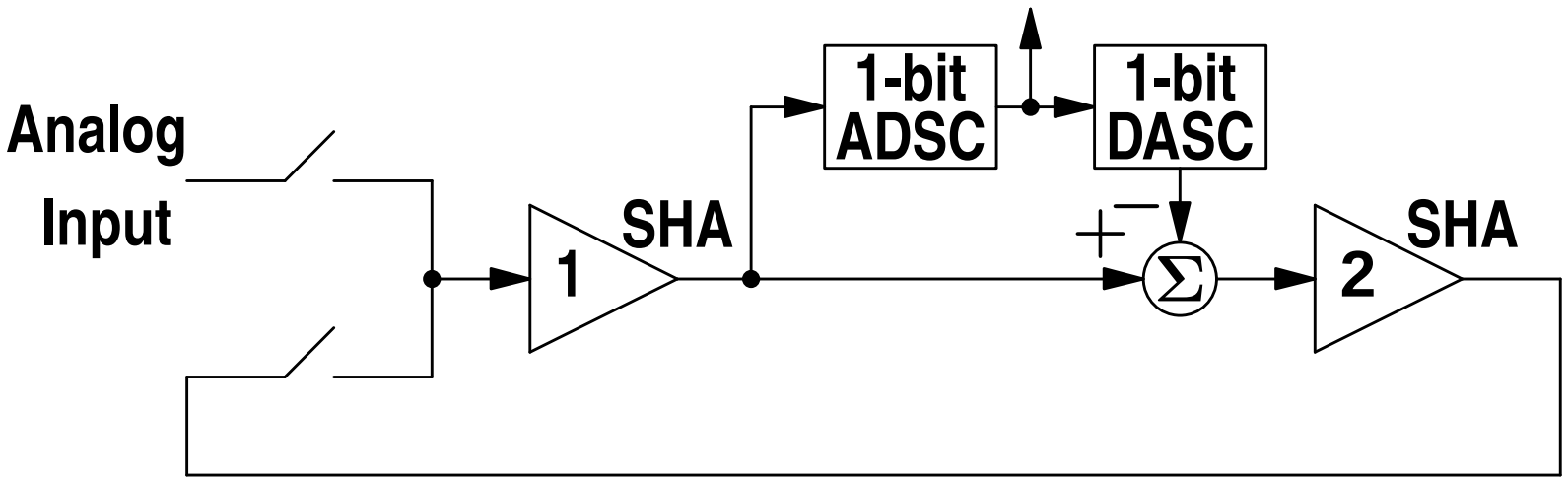
  Waldhauer, US Patent #3,187,325, 6/65
- Black, PhD Thesis, UC Berkeley, 11/80
- McCharles, PhD Thesis, UC Berkeley, 6/81
- Martin, Asilomar, 9/81

Pipelined ADCs Need SHAs



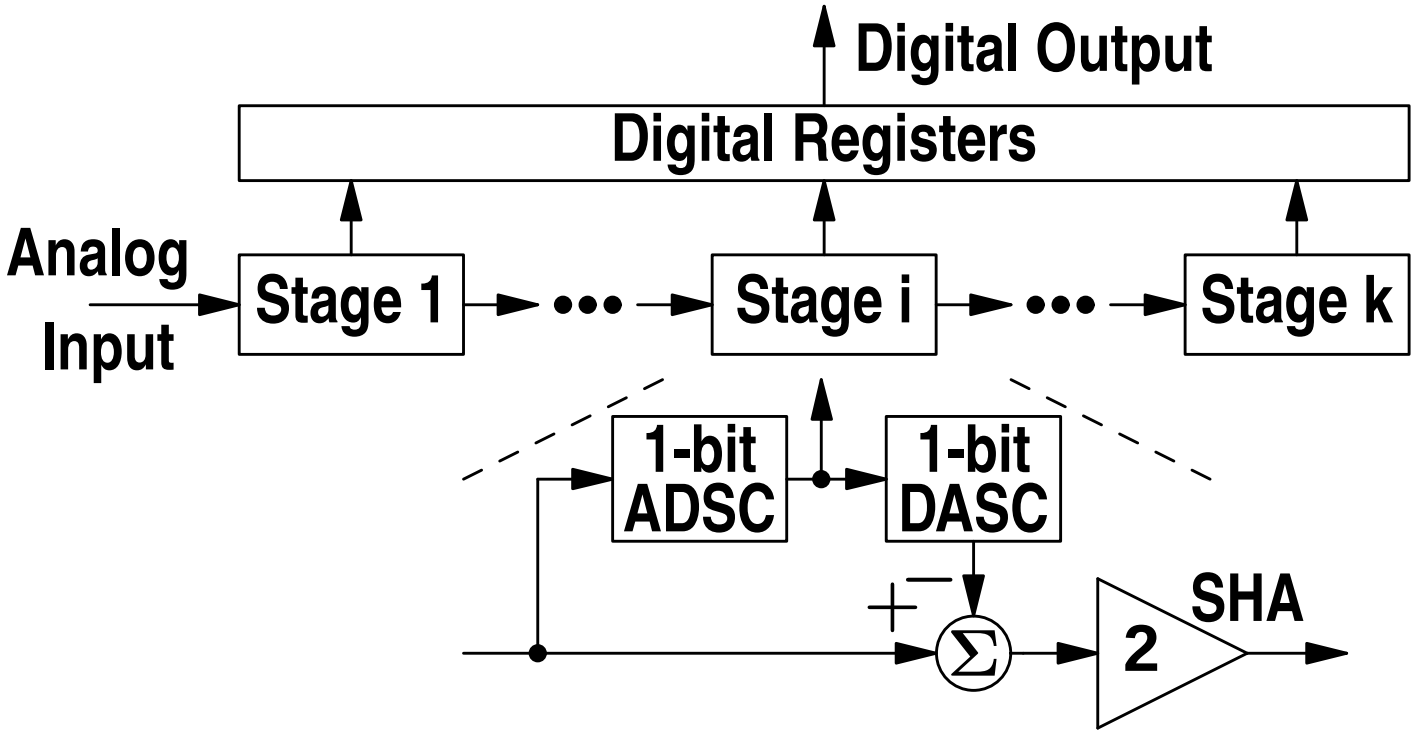
- CMOS provides simple SHAs
- MOS transistor switches have $V_{DS} = 0$ when $I_D = 0$
- Little leakage

Algorithmic ADCs



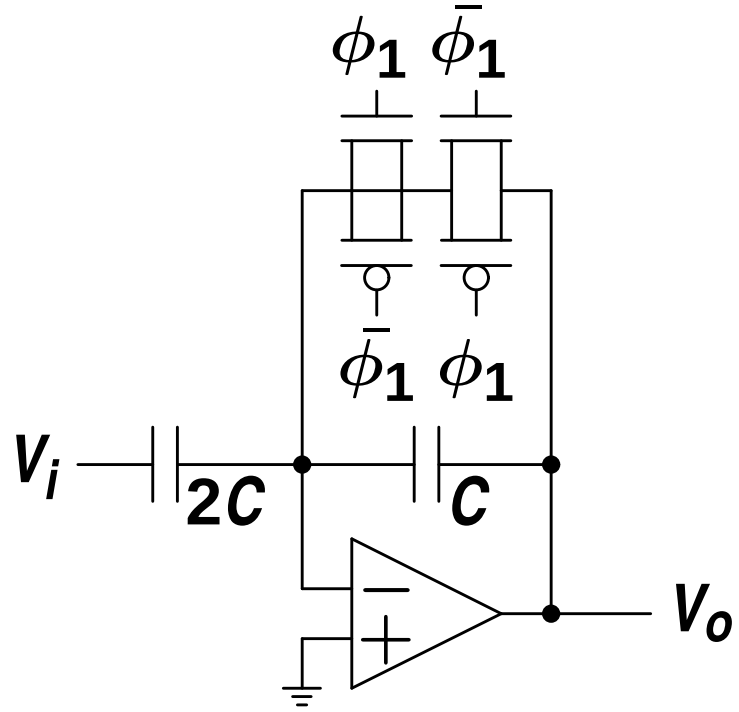
- Reusing stages saves area
- McCharles, Saletore, Black, and Hodges, ISSCC, 1977
- Li, Chin, Gray, and Castello, JSSC 12/84
- Shih and Gray, JSSC, 8/86

The First Monolithic Pipelined ADCs



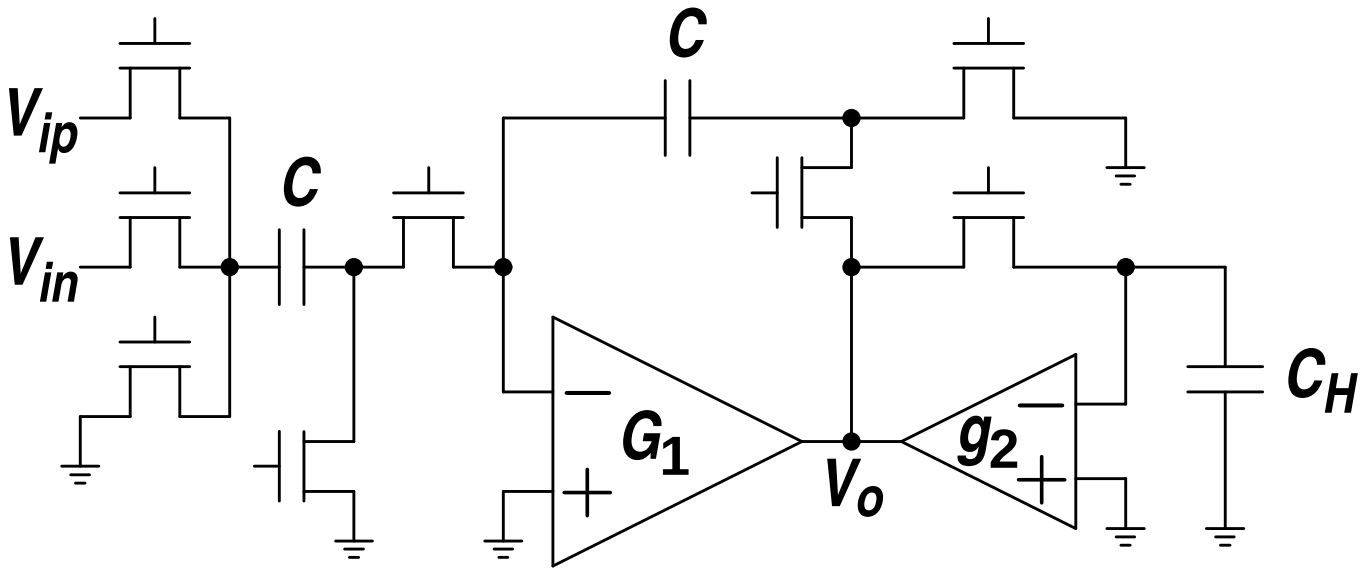
- Masuda, Kitamura, Ohya, and Kikuchi, CICC 1984
  7-b res. and linearity at 3 Msamples/s
- Yiu and Gray
  12-b res. and 10-b linearity at 278 ksamples/s
- No redundancy

Masuda's SHA



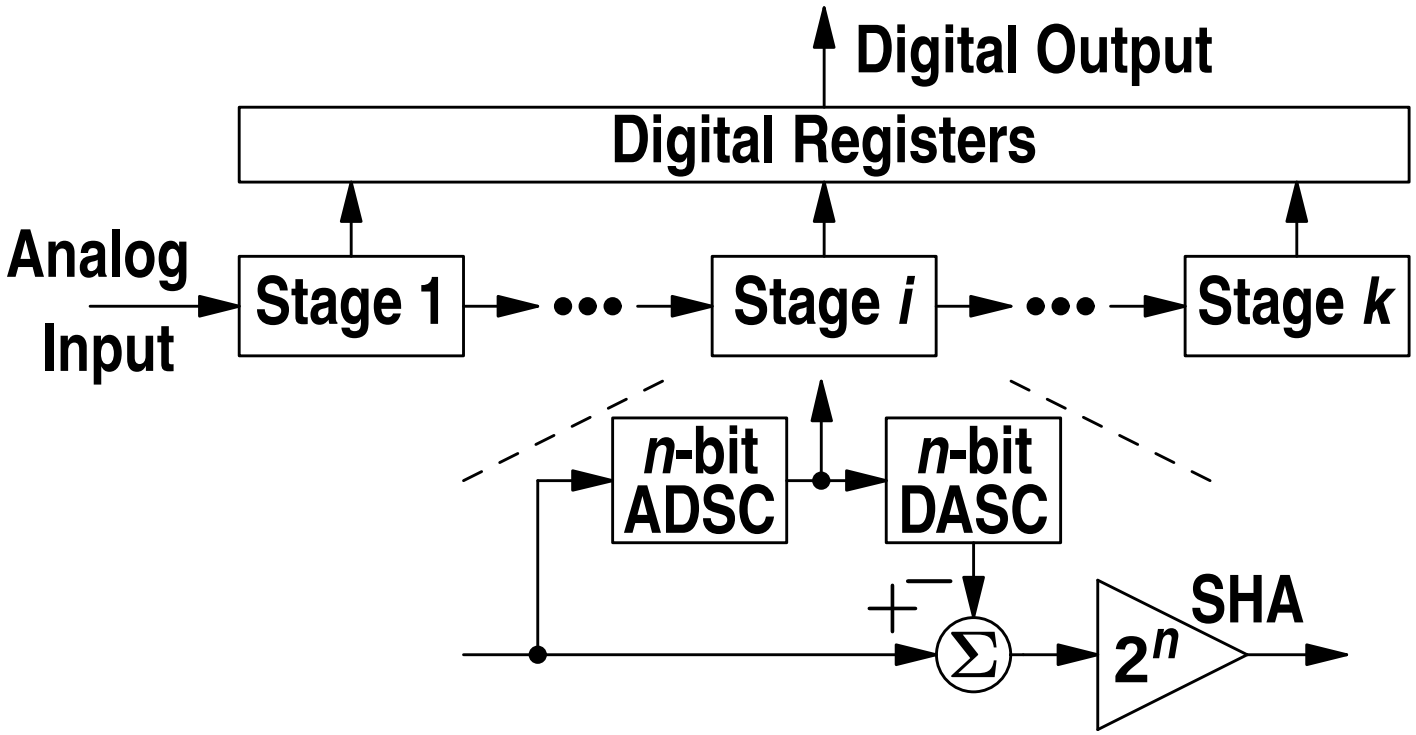
- Single ended in 1.5-μm CMOS
- Uses partial offset cancellation at the input
- Uses dummy switch to reduce charge-injection error

Yiu's SHA



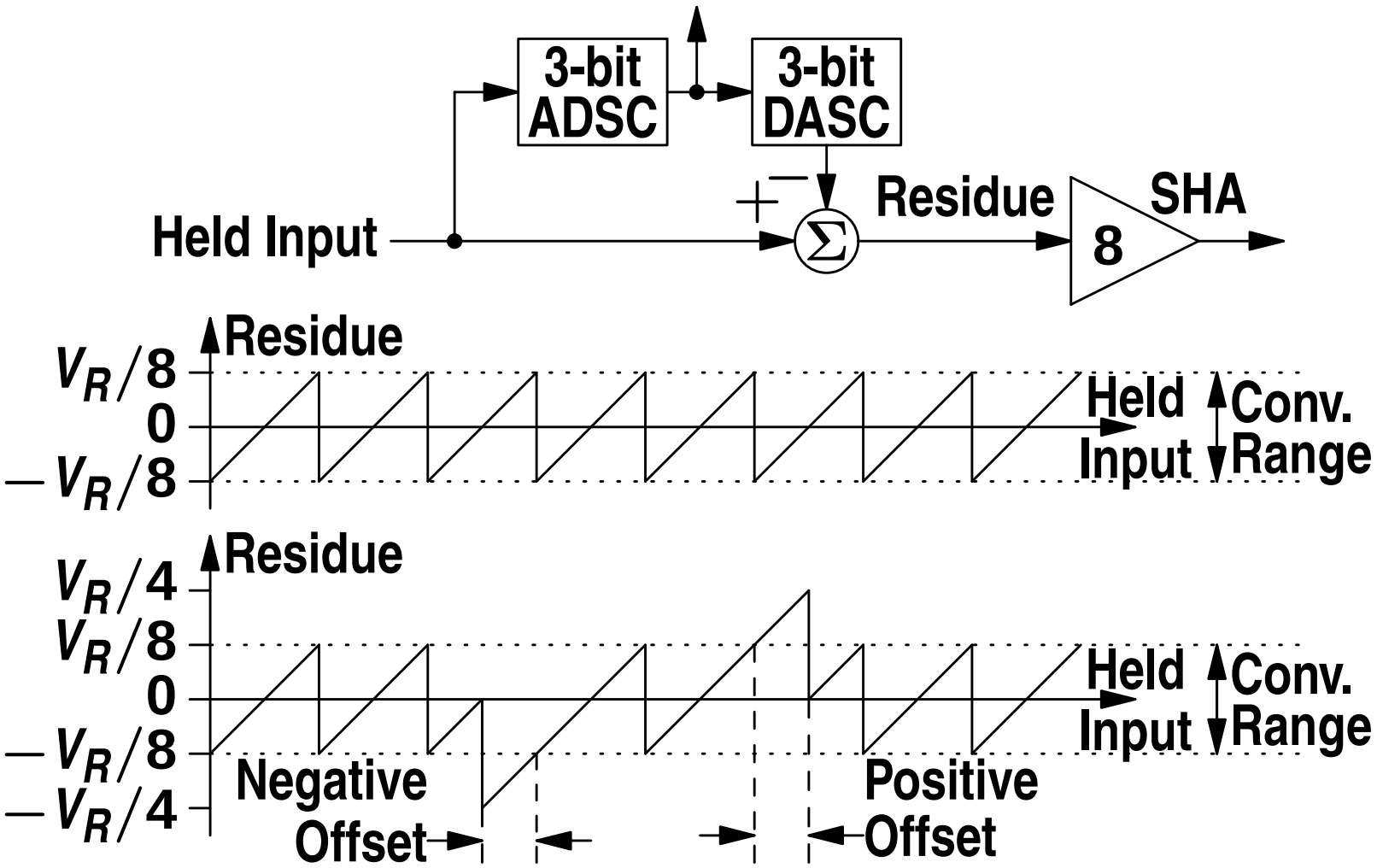
- Fully differential in 3-μm CMOS
- Cancels offset at aux. input (Degrauwe, JSSC 8/85)
- Uses reference refreshing (Shih and Gray, JSSC 8/86)
- 9 clock phases per conversion
- Fabricated in 1984, PhD Thesis, UC Berkeley, 1992

Increased Stage Resolution and Interstage Gain



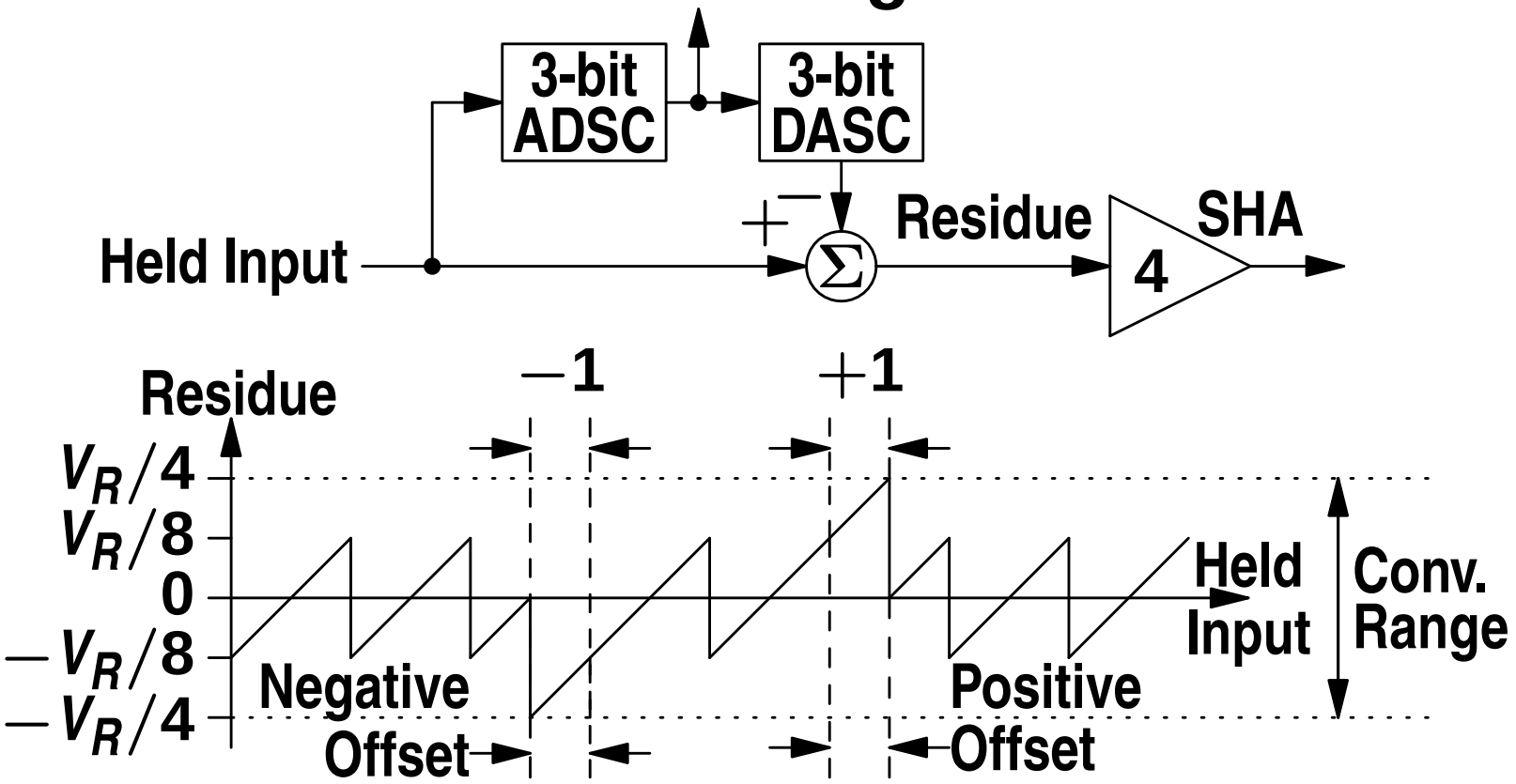
- Increasing *n* reduces significance of errors after first stage
- Still sensitive to first-stage comparator offsets

Residue Plots



- If DASC is ideal, digital output and residue together are still accurate
- However, increasing max. |Residue| saturates next stage

Reduced Interstage Gain



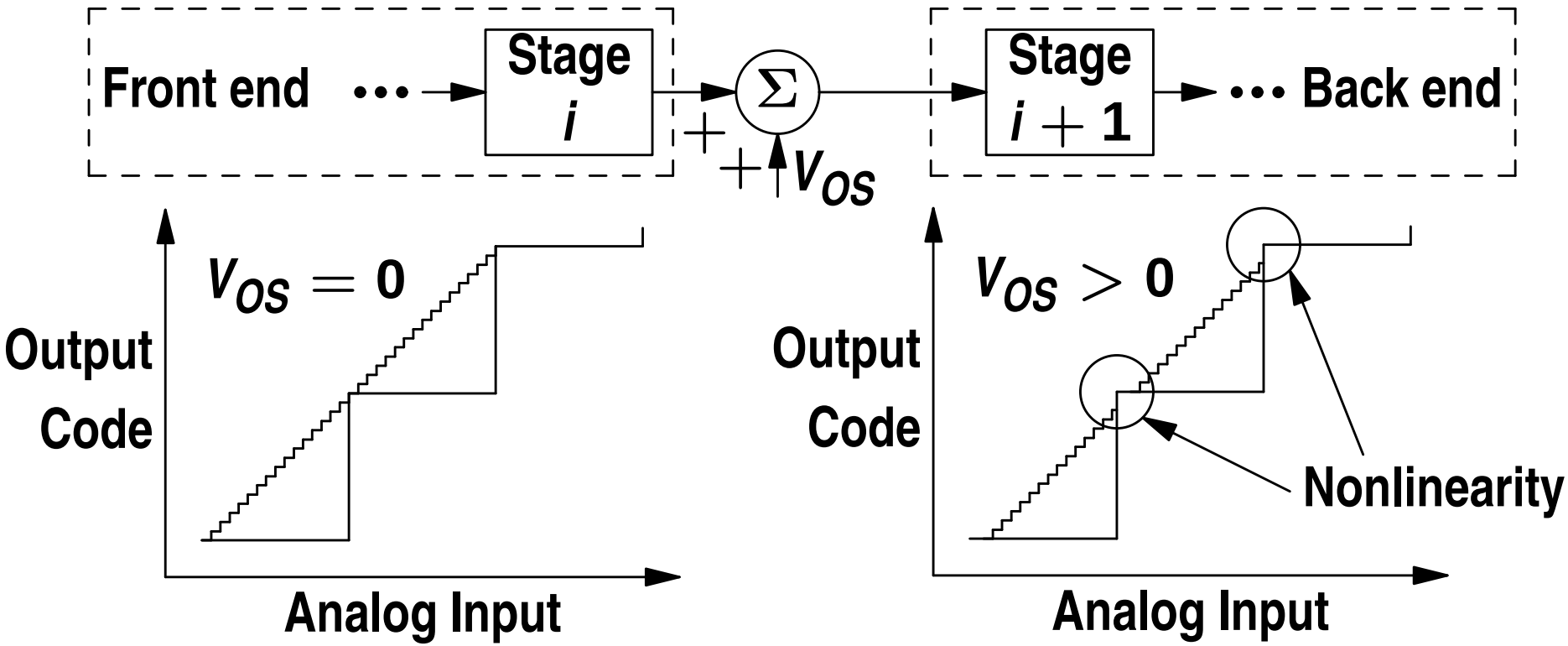
- Halving the gain doubles the next-stage range
- Now the errors shown can be measured and corrected
- Correction requires ± 1
- Correction range is ± 0.5 LSB @ 3-b level

Previous Work on Redundancy and Dig. Correction

- Verster, IEEE Trans. on Electronic Computers, 12/64
- Gorbatenko, IEEE National Convention Record, 3/66
- Kinniment, Aspinall, and Edwards, IEE Proc., 12/66
- Horna, Comsat Technical Review, 1972
- Taylor, PhD Thesis, UC Berkeley, 1978

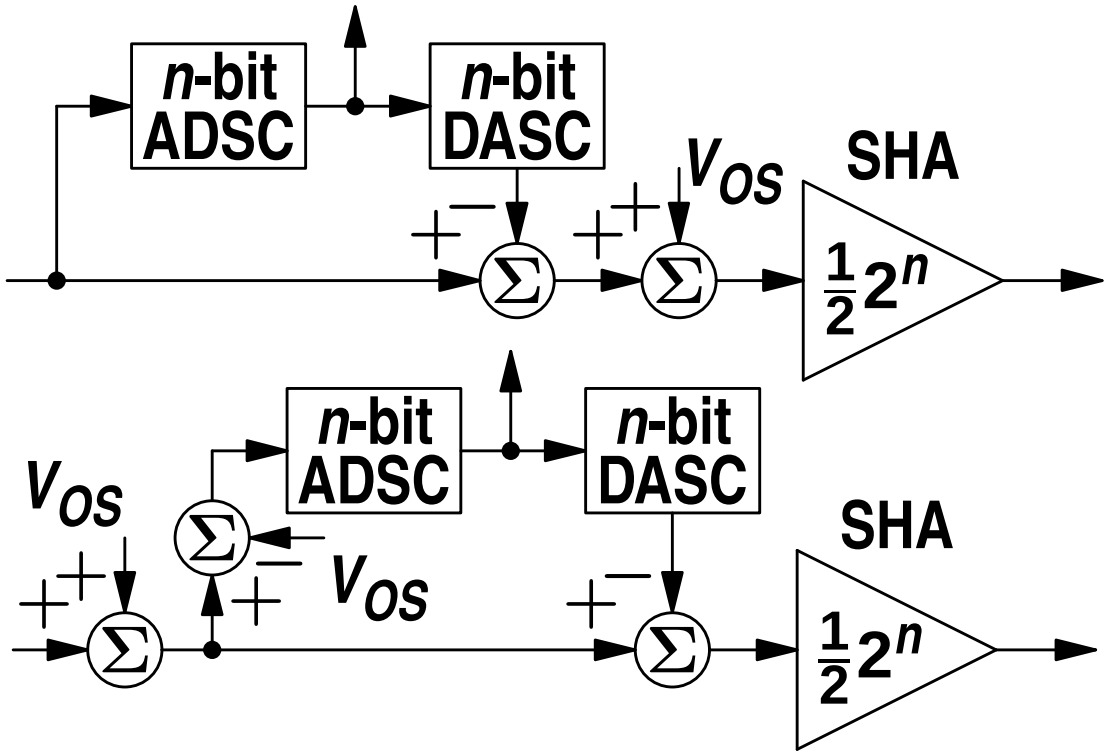
- Enabled by CMOS technologies

Interstage Offset without Redundancy



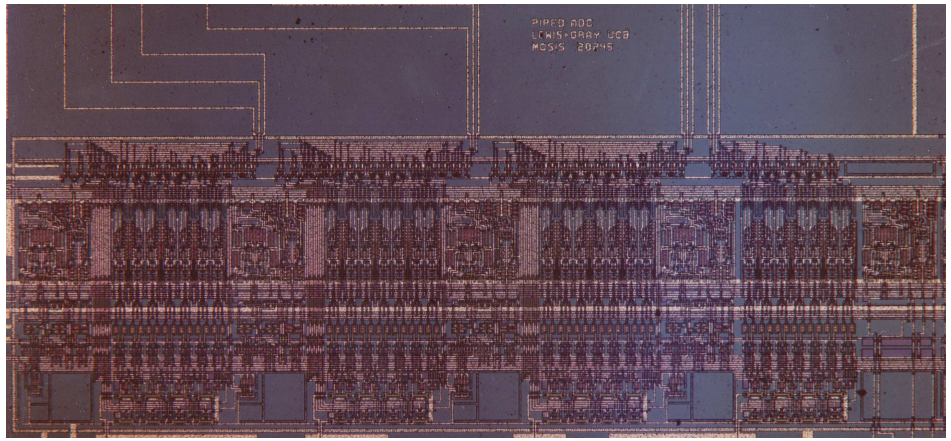
- If $V_{OS} \neq 0$, fine and coarse thresholds are not aligned
- Nonlinearity appears
- Offset cancellation is usually needed without redundancy

Interstage Offset with Redundancy



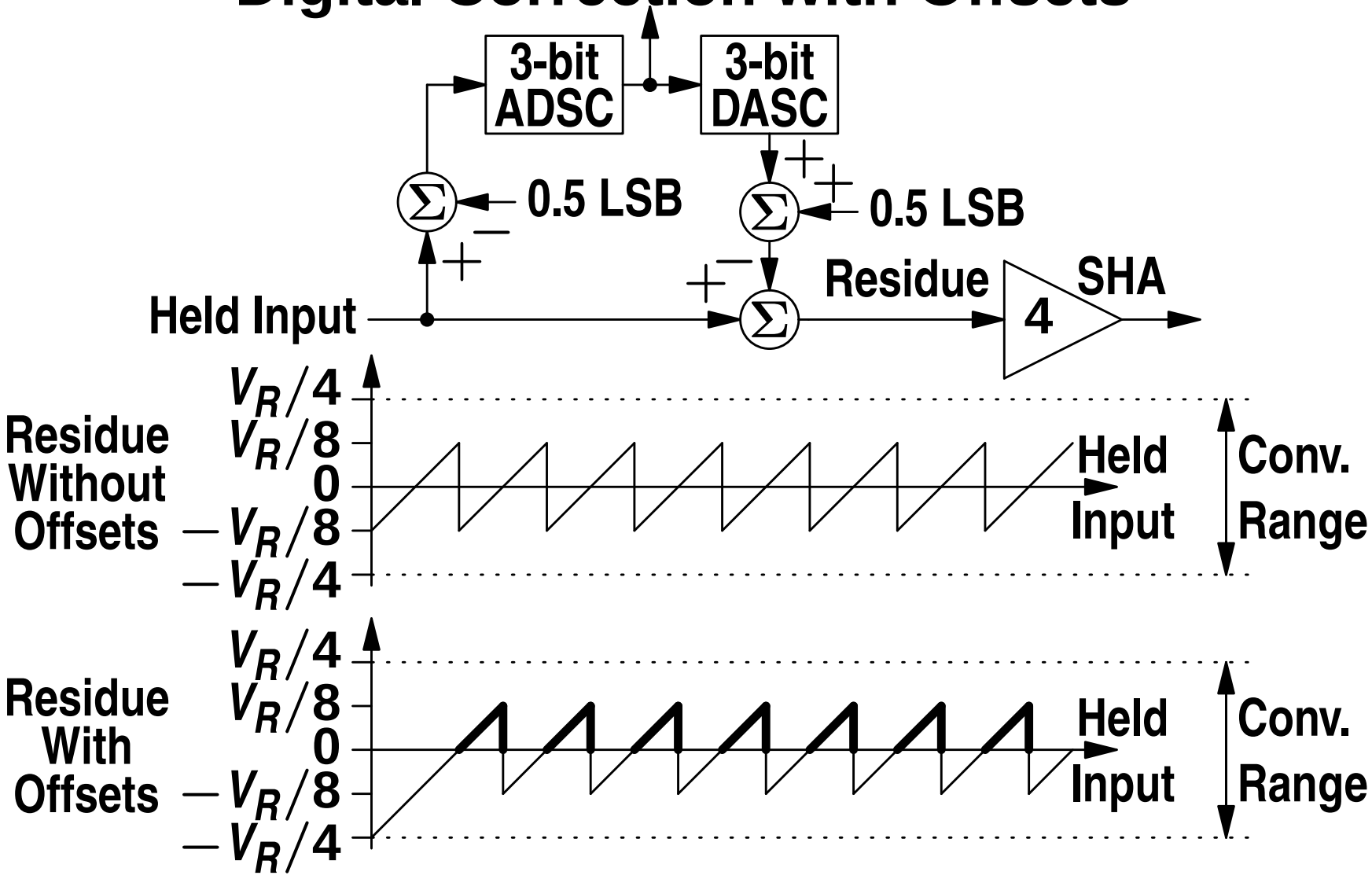
- If V_{OS} < correction range,
  Nonlinearity does not appear
  $V_{OS} \neq 0$ causes only input-referred offset
- Offset cancellation is not required
  Reduces power dissipation

Berkeley Pipeline



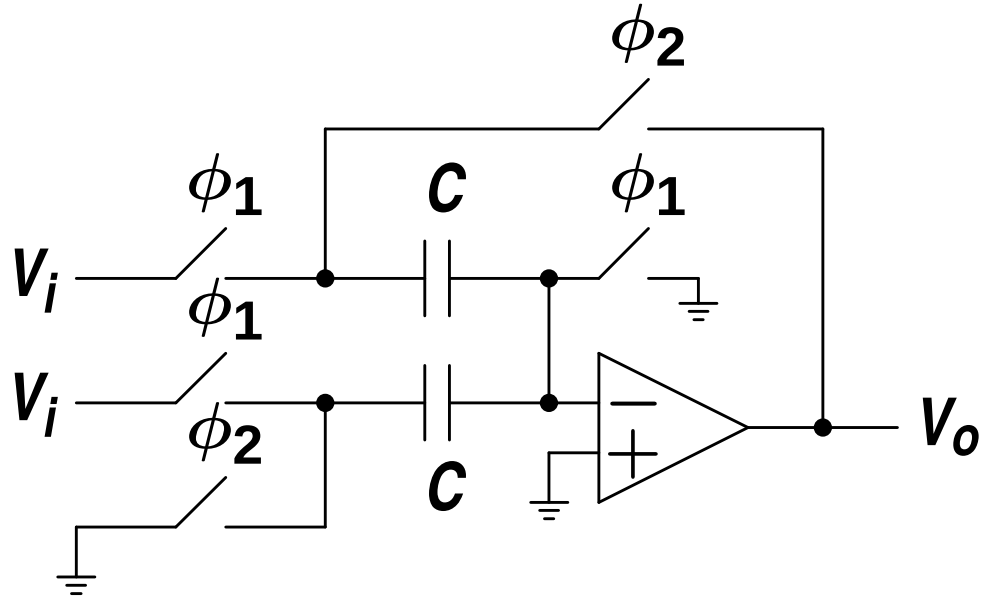
- 3-μm double-poly CMOS
- Area $=$ 5.5 mm^2
- Power Diss. $=$ 180 mW
- Speed $=$ 5 Msamples/s
- Resolution $=$ 9 bits

Digital Correction with Offsets



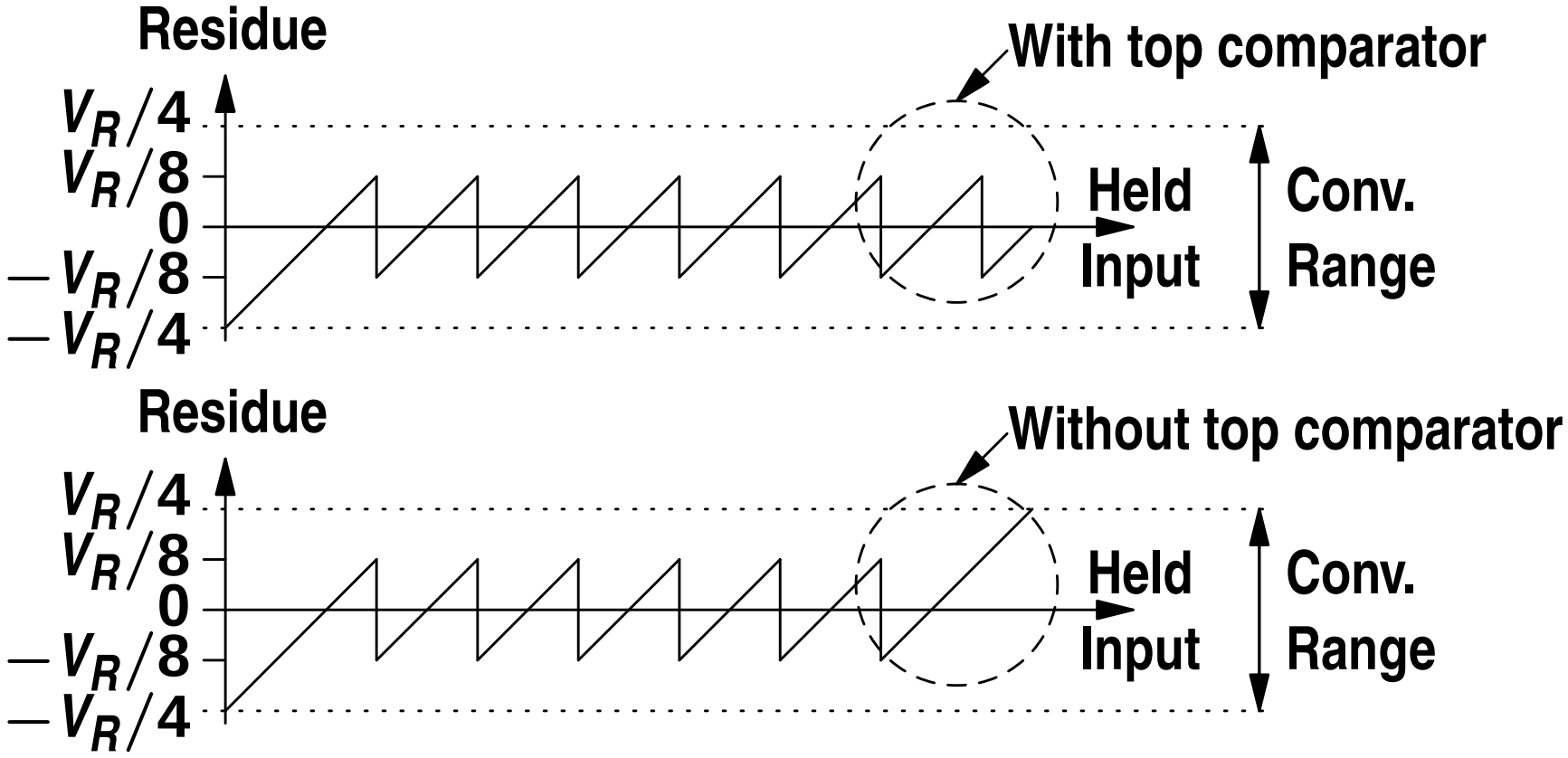
- Correction requires $+1$ when Residue > 0
- Correction range is still ± 0.5 LSB @ 3-b level

Sutardja's SHA



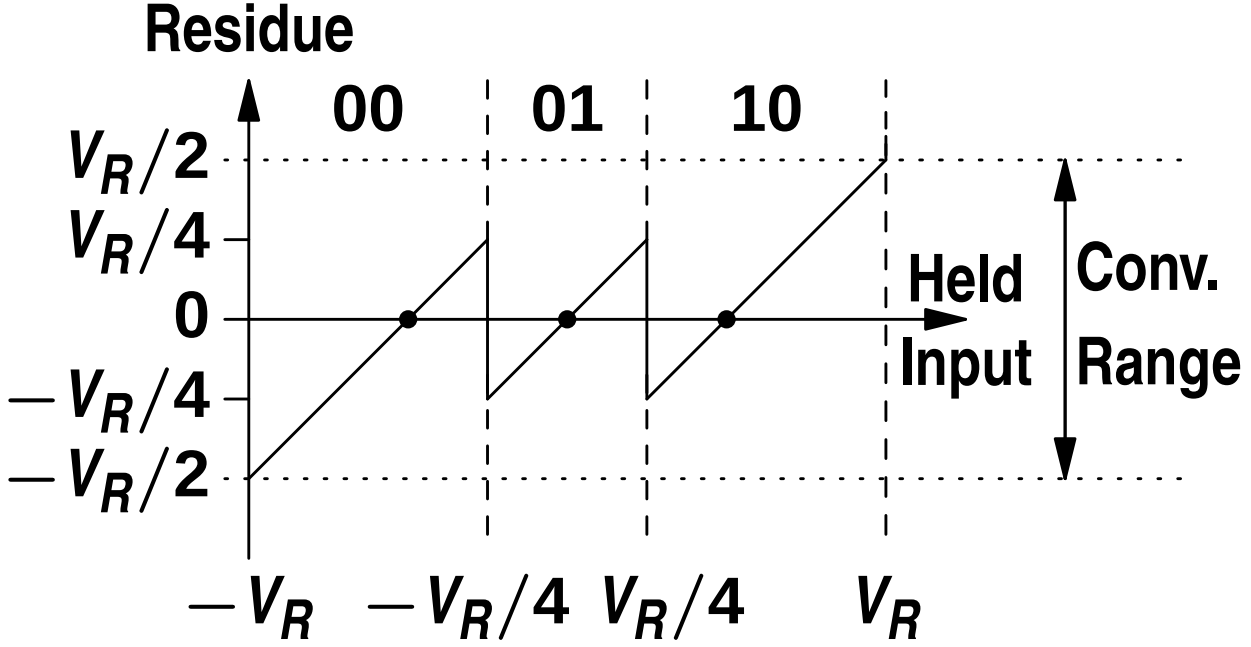
- Uses feedforward to increase the gain
- Gives ideal gain $= 2$ with equal capacitors
- Increases FB factor and speed & improves accuracy
- PhD Thesis, UC Berkeley, 1988

Drop the Top Comparator



- Forces error that can be corrected (simplifies testing)
- Does not change the correction range
- Requires $2^n - 2$ comps (Res $= log_2(7) \simeq 2.8$ b/stg)
- Not fast enough for video in 0.9-μm CMOS

1.5-bit Stage Resolution

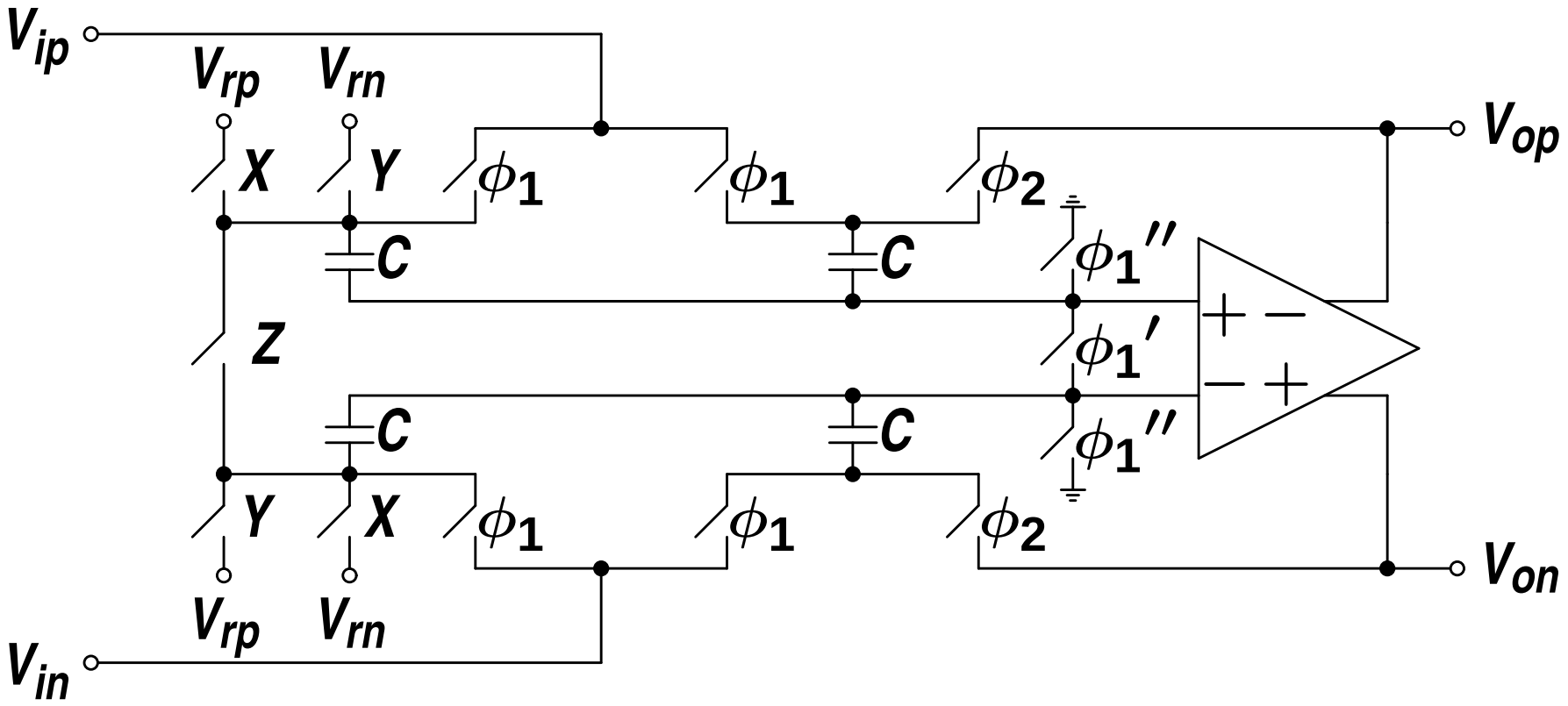


- Requires 2 comps and 3 DAC levels (Res $= log_2(3) \simeq 1.5$ b/stg)
- Same as in

  Jusuf, Memo No. UCB/ERL M90/69, UC Berkeley, 8/90

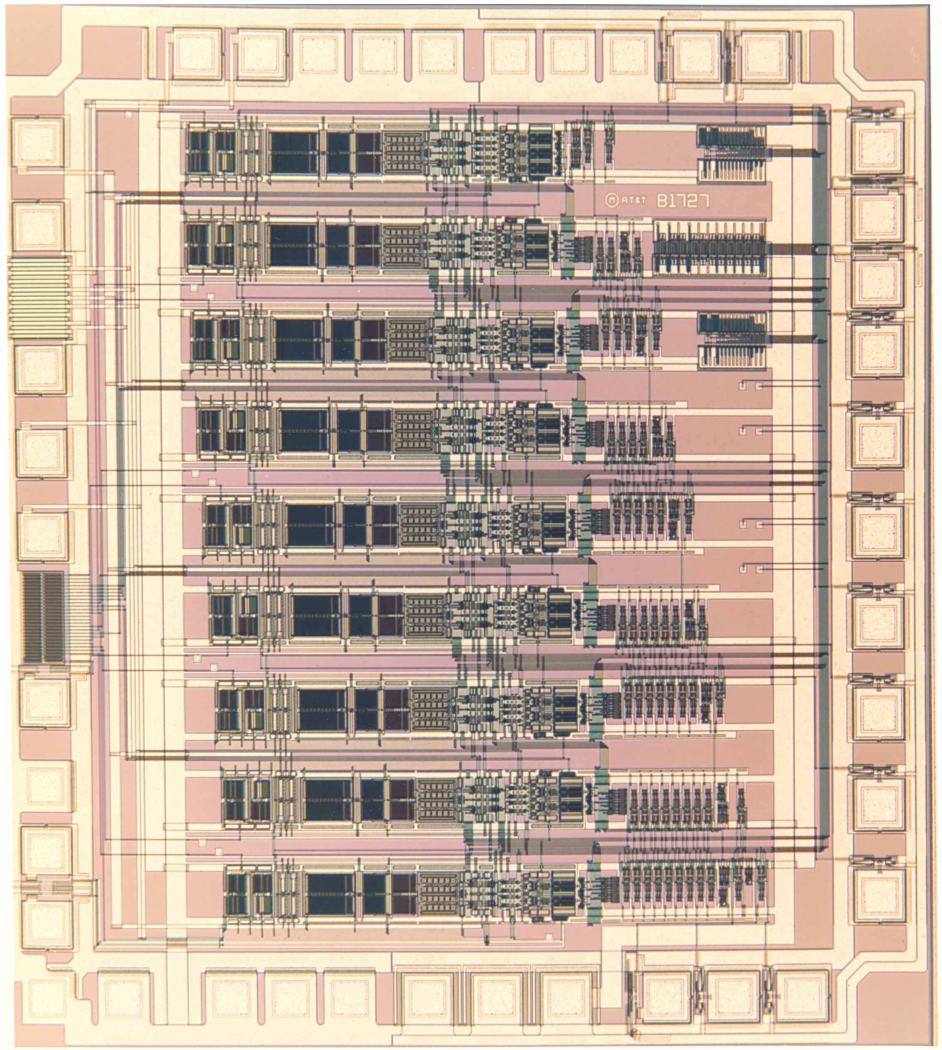
  Ginetti, Jespers, and Vandemeulebroecke, JSSC 7/92

Multiplying-Digital-to-Analog Converter



- Feed forward improves accuracy and speed
- Generates 3 DAC levels
- Fast enough for video in 0.9-μm CMOS

AT&T Pipeline



- 0.9-μm double-poly CMOS
- Area $=$ 8.7 mm^2
- Power Diss. $=$ 240 mW
- Speed $=$ 20 Msamples/s
- Resolution $=$ 10 bits

Other Work

- Karanicolas, Lee, and Bacrania, JSSC, 12/93
- Cho and Gray, JSSC, 3/95
- Cline and Gray, JSSC, 3/96

Acknowledgments

- Professor Paul R. Gray
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