Digitally Corrected Data Converters

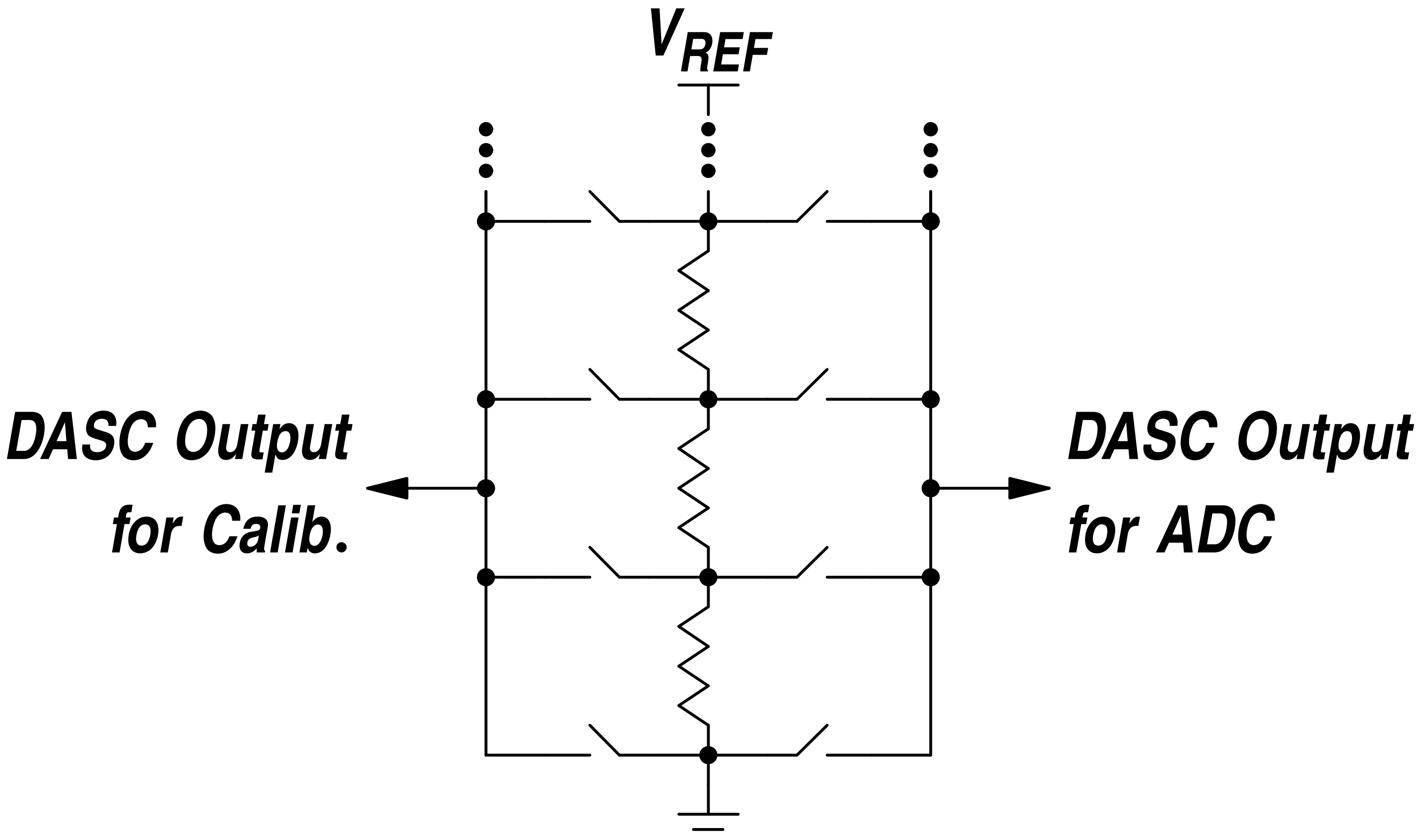
Stephen H. Lewis

Solid-State Circuits Research Laboratory
Department of Electrical and Computer Engineering
University of California, Davis CA USA

Background-Calibration Techniques

- Parallelism (Shu et al. JSSC 4/95)
- Skip and fill (Moon et al. TCASII 2/97 & Kwak et al. JSSC 12/97)
- Queueing (Erdoğan et al. JSSC 12/99)
- Embedded dither (Jewett et al. ISSCC 2/97)

Parallelism (Resistor-String DASC)

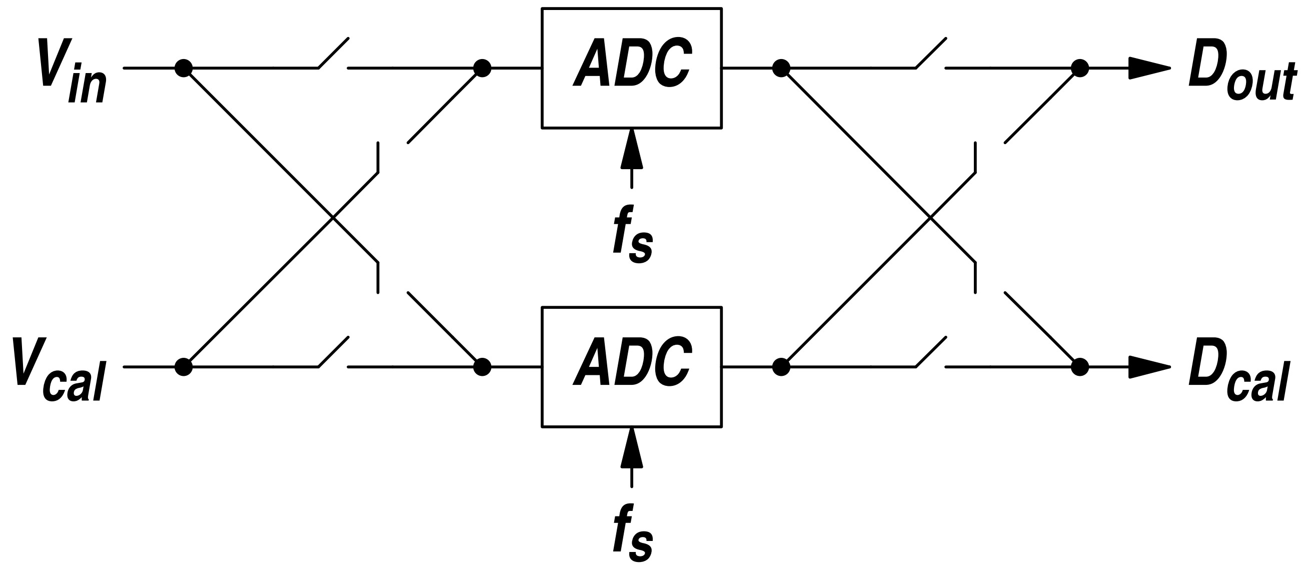


- Shu et al., JSSC 4/95
- All DASC outputs available all the time
- Only works for resistor strings

Figure of Merit (FOM)

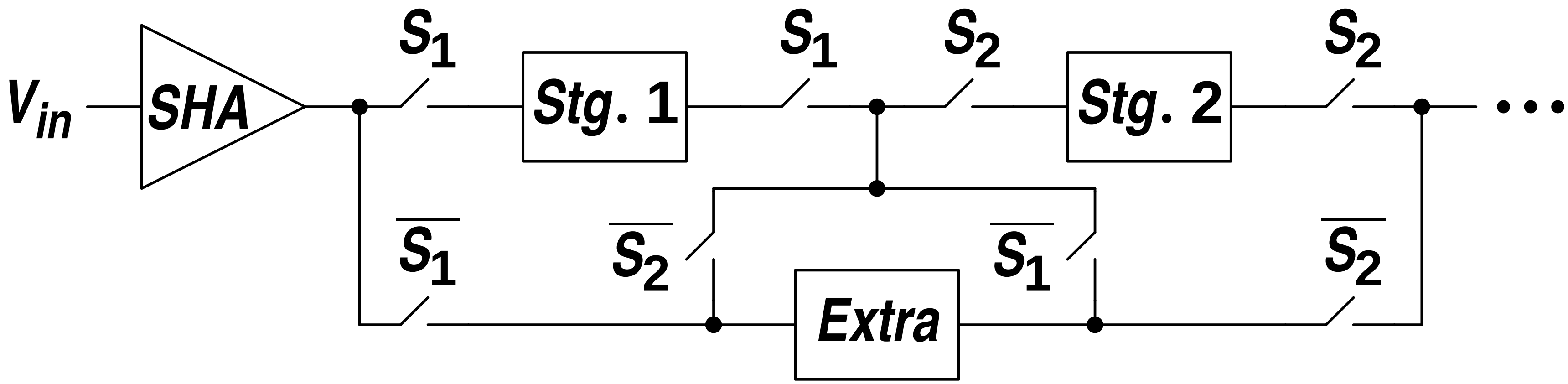
- $FOM = \frac{P}{f_S 2^{ENOB}}$
- Example: $FOM = \dfrac{500\ \text{mW}}{100\ \dfrac{\text{Msample}}{\text{s}} \cdot 2^{11}\ \dfrac{\text{steps}}{\text{sample}}} = 2.5\ \dfrac{\text{pJ}}{\text{step}}$
- Assume digital calibration circuits are free

Parallelism



- $FOM = \frac{2P}{f_s 2^{ENOB}}$
- Reduce overhead by increasing number of channels
- Dyer et al., JSSC 12/98, $FOM = \frac{1.5P}{f_s 2^{ENOB}}$

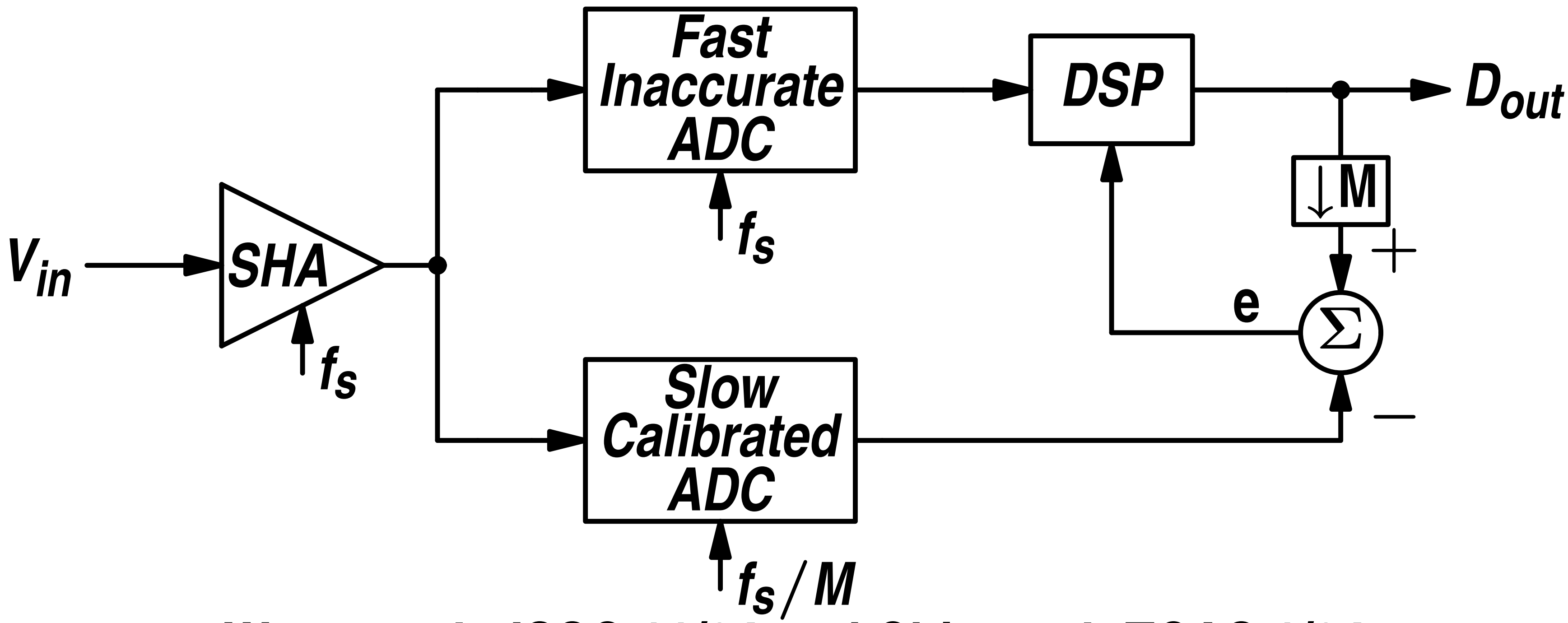
Extra Stage



- Ingino et al., JSSC 12/98
- Extra stg. must have same noise performance as stg. 1
- With scaled stages (Cline et al., JSSC 3/96)

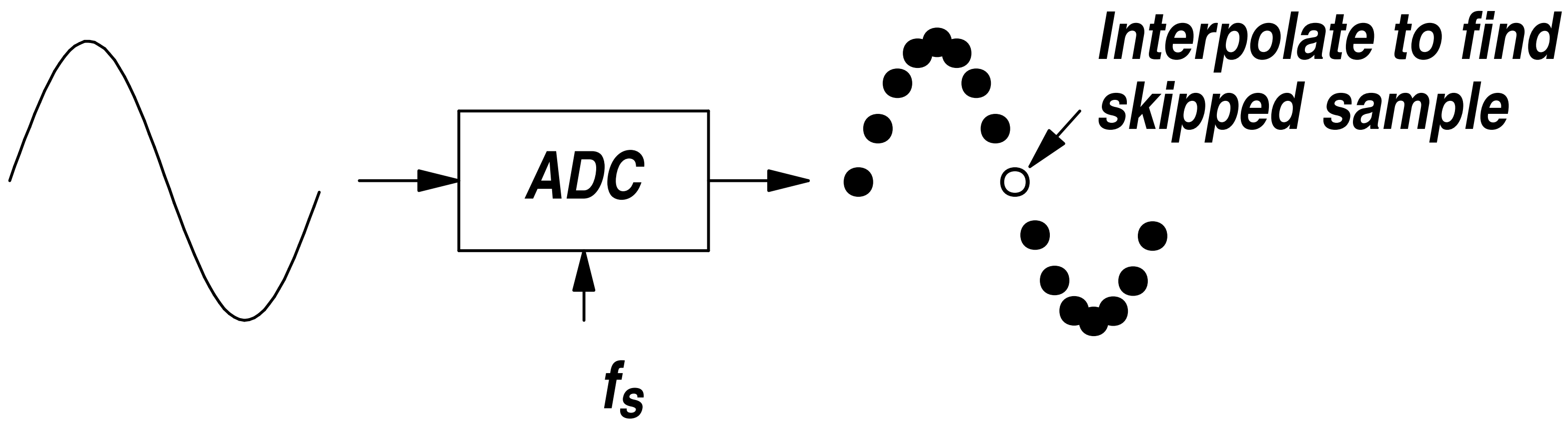
$$FOM \approx \frac{1.25P}{f_s 2^{ENOB}}$$

Parallelism with Nesting



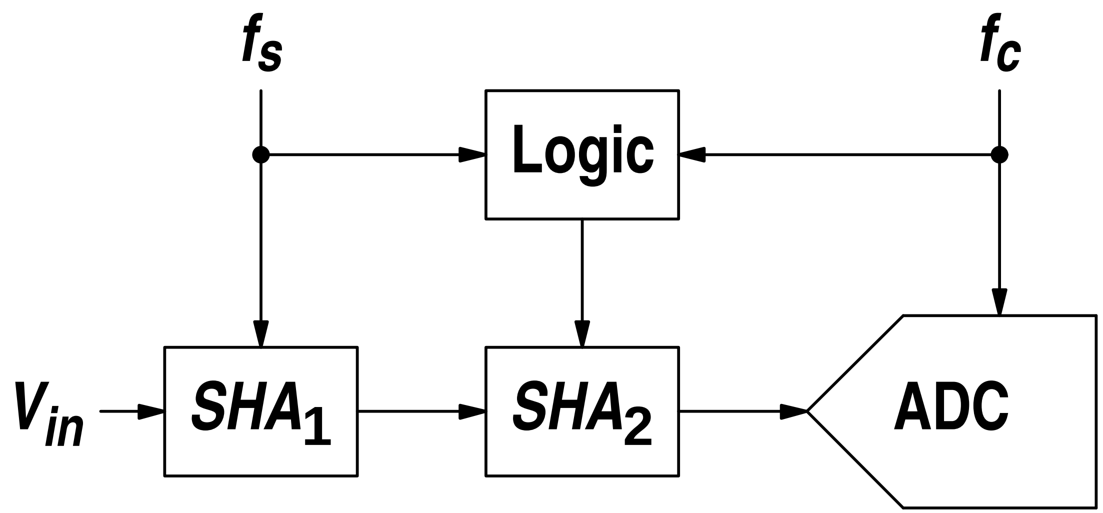
- Wang et al. JSSC 11/04 and Chiu et al. TCAS 1/04
- Uses V_{in} to calibrate
- Slow ADC can have high noise & low power dissipation
- $FOM \approx \frac{1.2P}{f_s 2^{ENOB}}$

Skip and Fill



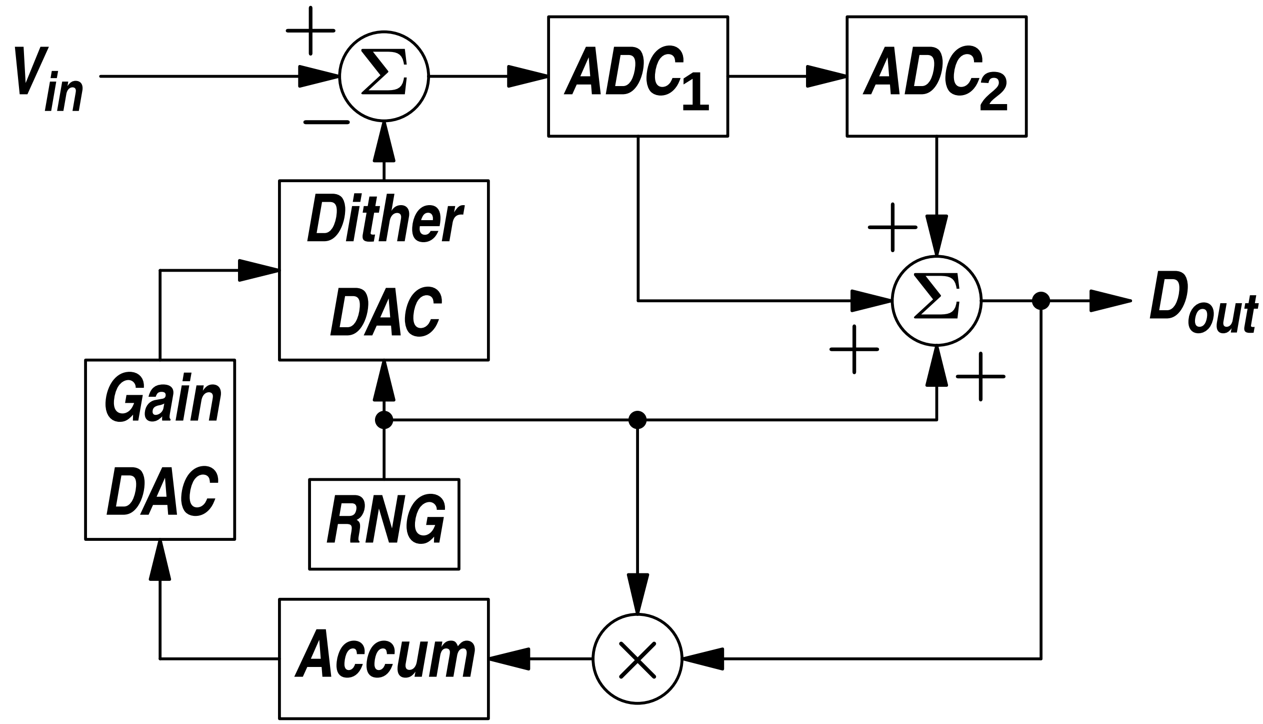
- Moon et al. TCASII 2/97 & Kwak et al. JSSC 12/97
- Interpolation limits bandwidth to $f_s/3$
- $FOM \approx \frac{1.5P}{f_s 2^{ENOB}}$

Queueing



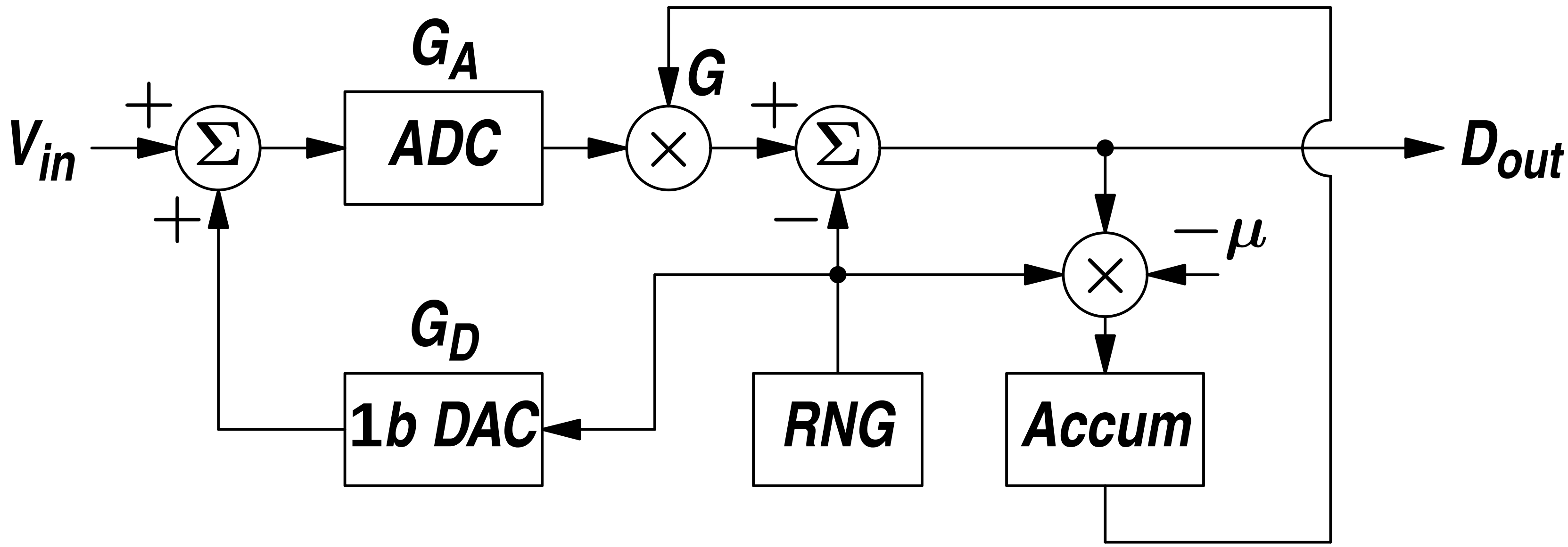
- Erdoğan et al., JSSC 12/99
- $f_c > f_s$
- Extra SHA increases noise $\longrightarrow$ $FOM \approx \frac{1.5P}{f_s 2^{ENOB}}$
- With only 1 SHA (JSSC: Blecker 6/03, Grace 5/05), same *FOM*

Add Dither to Input (1)



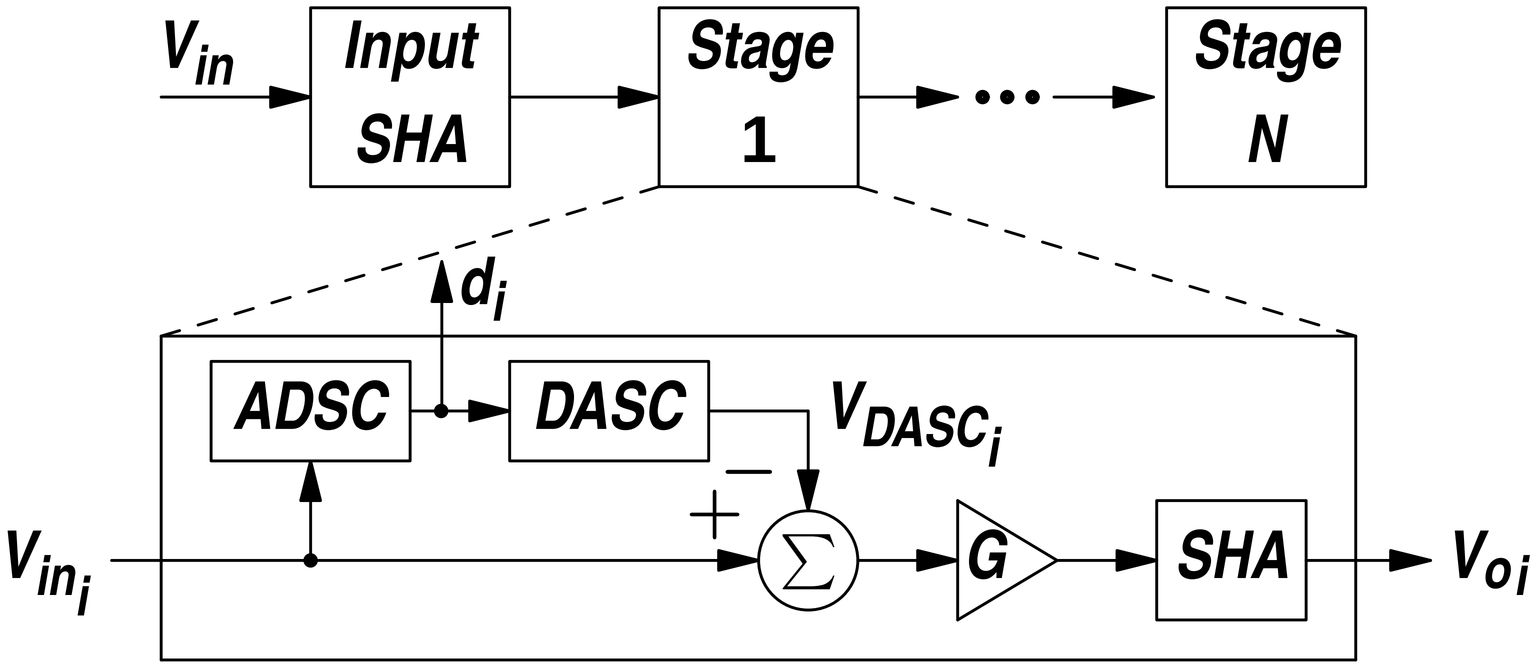
- Jewett et al., ISSCC 2/97
- Power diss. penalty depends on dither amplitude
- If dither amplitude is 10% of FS, $FOM \approx \frac{1.2P}{f_s 2^{ENOB}}$

Add Dither to Input (2)



- Fu et al., JSSC 12/98
- $G_A \cdot G = 1/G_D$
- Calibrates gain mismatch with interleaved channels
- If dither amplitude is 10% of FS, $FOM \approx \frac{1.2P}{f_s 2^{ENOB}}$

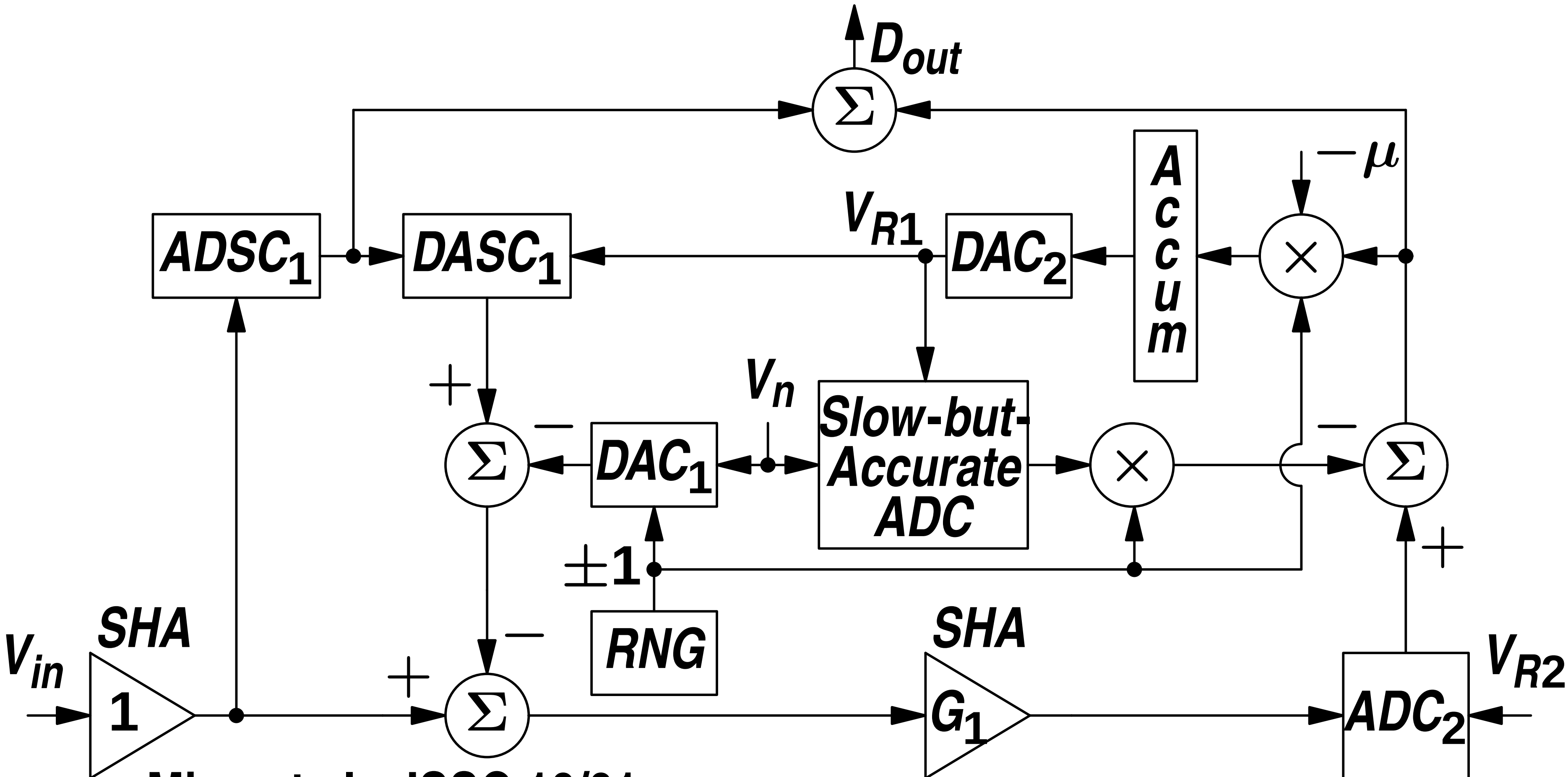
Pipelined ADC



- Insensitive to offset errors
- Main performance limitations:

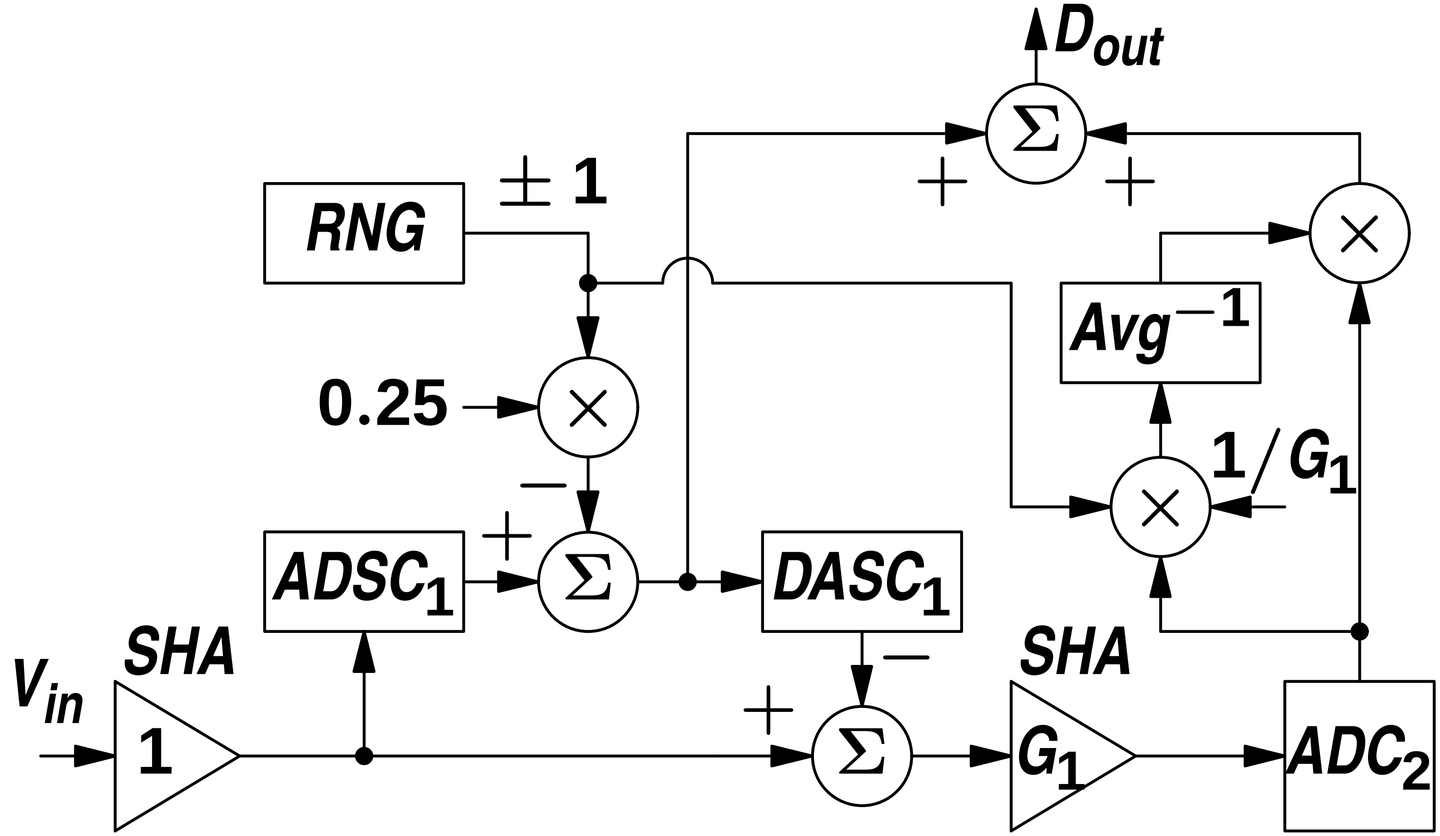
  DASC nonlinearity ⟶ Galton, TCASII 3/00
  Interstage gain errors

Add Dither to DASC Output



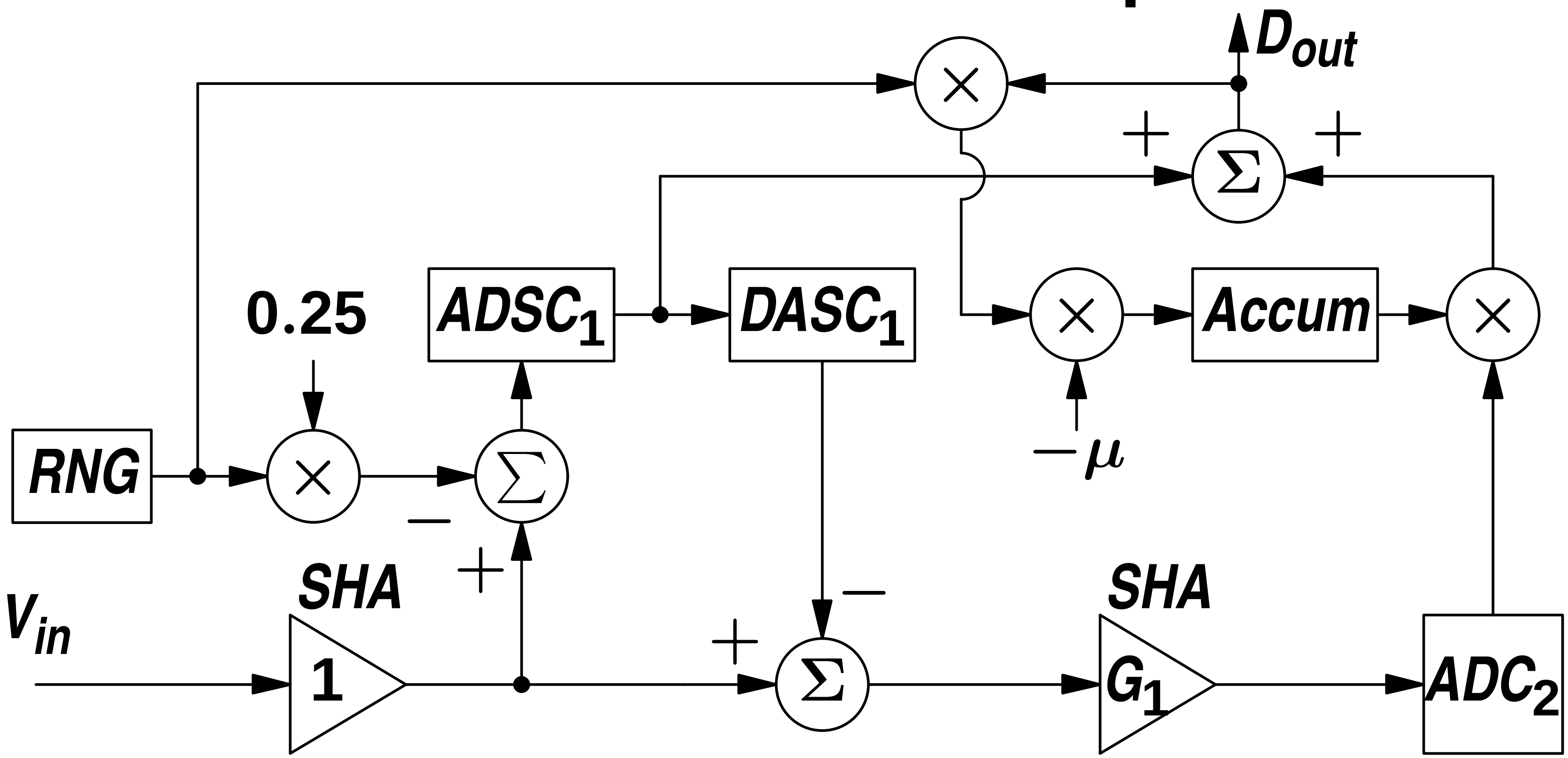
- Ming et al., JSSC 10/01
- Dither is inside correction range: $FOM \approx \frac{P}{f_s 2^{ENOB}}$
- Slow-but-accurate ADC needed to measure dither amplitude

Add Dither to ADSC Output



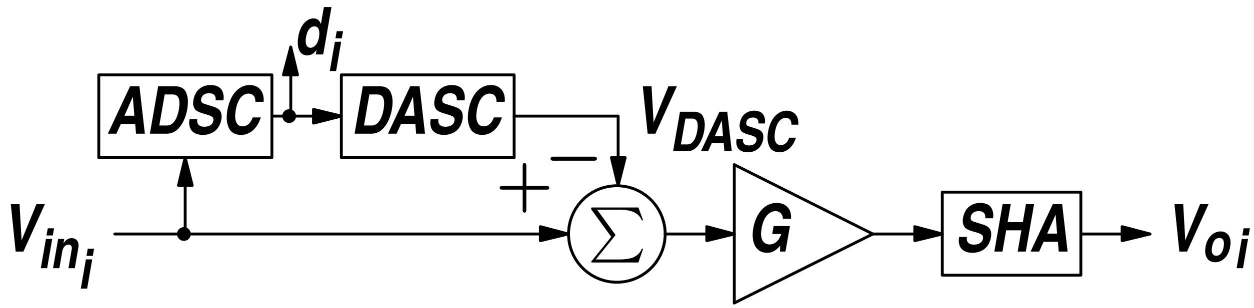
- Siragusa et al., Electronics Letters 3/00 & JSSC 12/04
- No slow-but-accurate ADC but increases DASC resolution
- $FOM \approx \frac{P}{f_s 2^{ENOB}}$

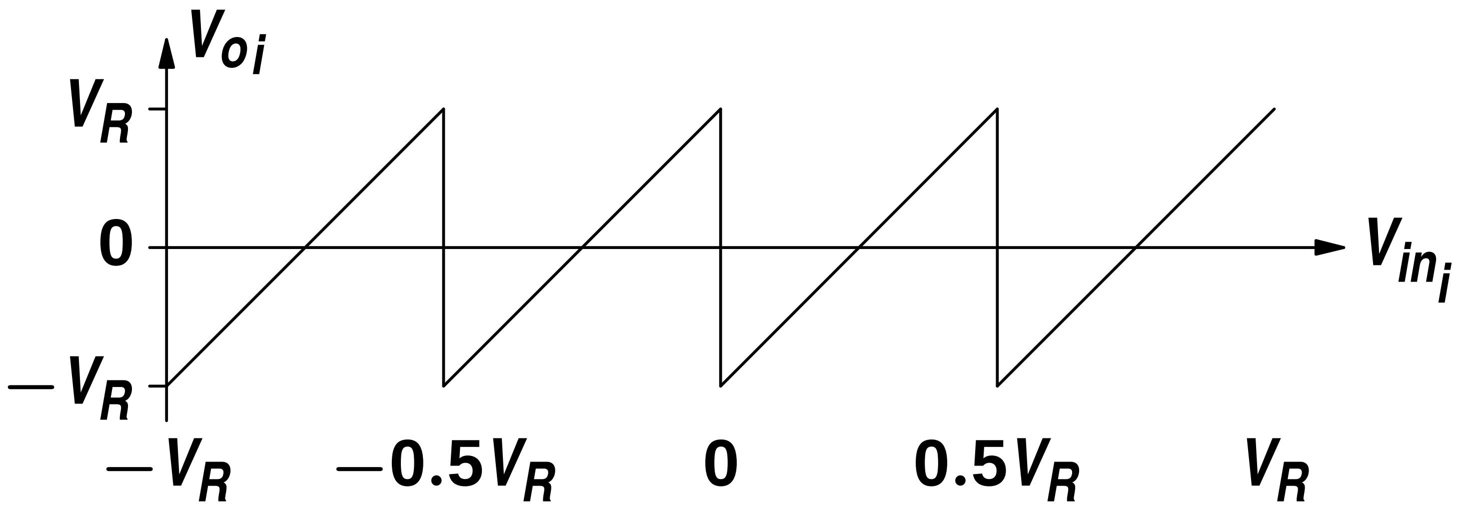
Add Dither to ADSC Input



- Li et al. TCASII 9/03
- Low complexity but only calibrates for V_{in} near $ADSC_1$ thresholds
- $FOM \approx \frac{P}{f_s 2^{ENOB}}$
- Fetterman et al., CICC 5/99 (dither without calibration)

Without Calibration

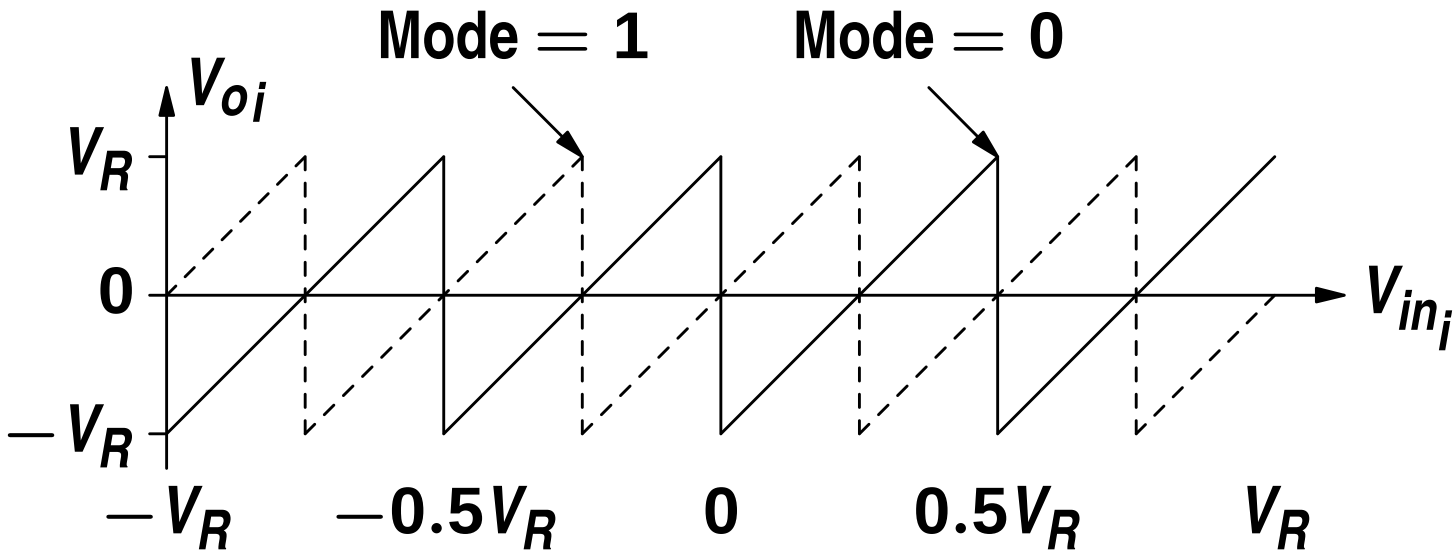




- Ideal jump $= 2V_R$
- Measure jump to calibrate gain error digitally

  Karanicolas et al., JSSC 12/93 (foreground cal.)

Redundant Residue Mode



- Murmann et al., JSSC 12/03
- Requires about 1 extra bit of resolution
- Equivalent to adding dither to ADSC and DASC inputs
- Ideally both modes give identical results
- Calibrates by measuring ΔV_{o_i} statistically

Key Points (Murmann)

- Overhead:

1.

	Prototype	Post proc.	Net
Area	Same	$+1.4$ mm^2	$+18\%$
Power	-33 mW	$+10$ mW	$-\ 7\%$

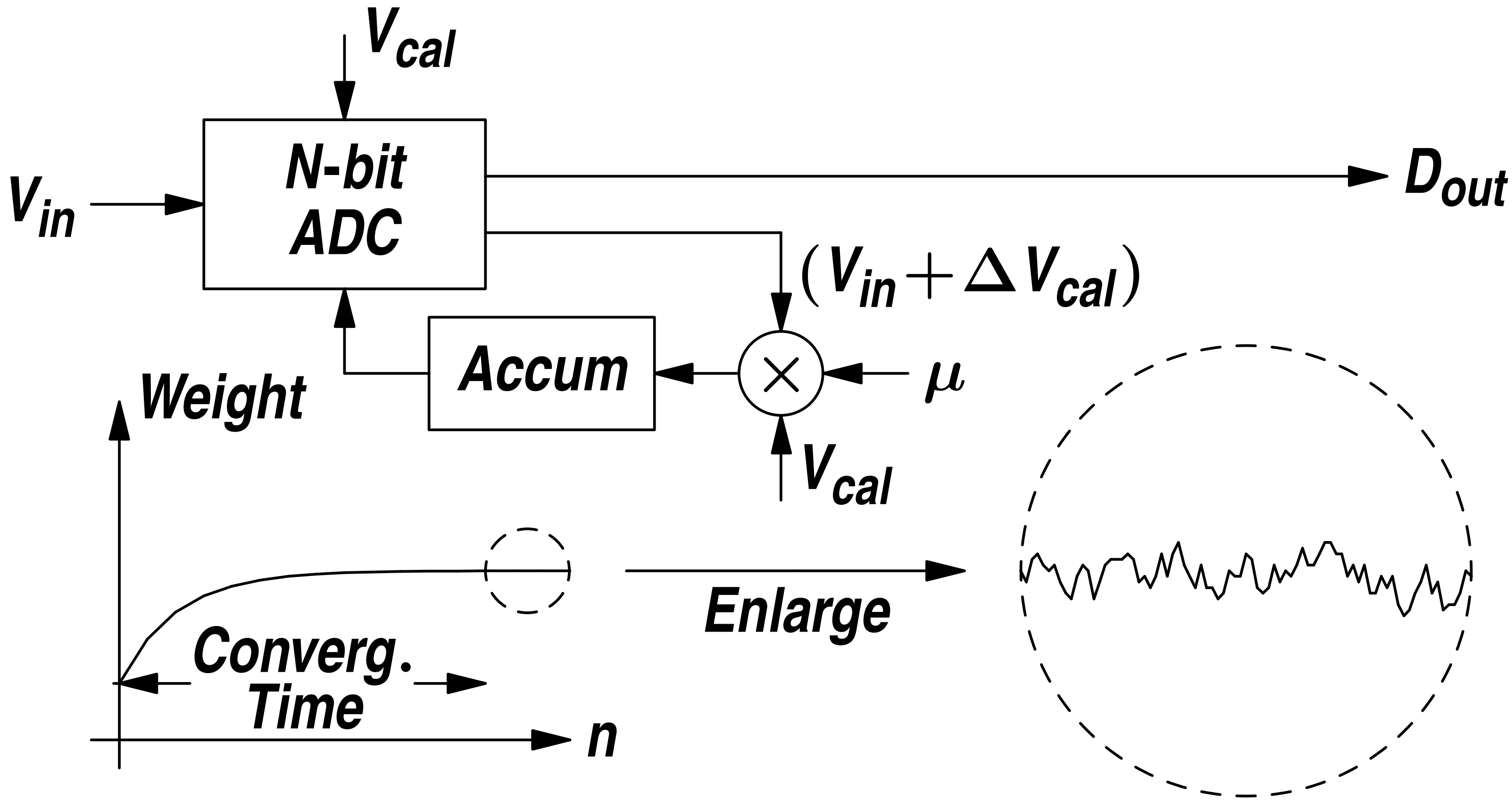
Therefore, $FOM \approx \frac{(0.93)P}{f_s 2^{ENOB}}$

2. Test time increases

- Convergence time:

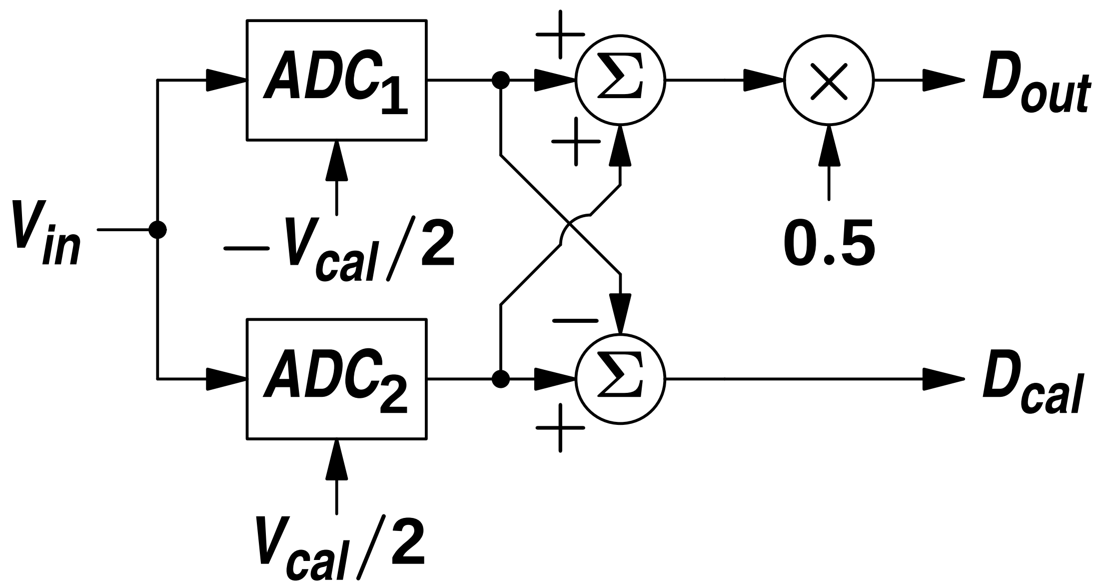
1. Code dependent (see Keane et al., TCASI 1/05)
2. Slow (input varies during calibration)

Convergence Time



- $Weight[n+1] = Weight[n] + \mu(V_{in} + \Delta V_{cal}) \cdot V_{cal}$
- Steady state SNR $\propto 1/\mu$: Need small μ (Wang et al., ISCAS 5/05)
- Convergence time $\propto N \cdot 2^{2N}$

Two-Channel or Split ADC Architecture



- Li et al., TCASII 9/03 and JSSC 4/05
  McNeill et al., JSSC 12/05
- Reduces V_{in} in D_{cal}
- Reduces convergence time dramatically
- Requires little extra power dissipation

Other Work

- Any systematic error can be calibrated in principle
- Examples

  Offset (random chopping):

  van der Ploeg et al. JSSC 12/01 & Jamal JSSC 12/02

  Summing node error: Ali et al., TCASII 9/03

  Slew rate: Grace et al., JSSC 5/05

  Nonlinear gain (piecewise lin.): Yuan et al., CICC 9/05

  Memory errors: Keane et al., TCASI 3/06

  Incomplete settling (glitch suppression):

  Iroaga et al., VLSI Symp. 6/06

  OFDM-based UWB receivers: Oh et al., TCASI 8/06
- Commercially important when *FOM* is reduced