Digital Background Calibration of an Algorithmic Analog-to-Digital Converter Using a Simplified Queue

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Abstract

An analog queue-based architecture and an adaptive digital-calibration algorithm calibrate an 8-bit two-stage pipelined algorithmic analog-to-digital converter (ADC). To minimize power dissipation and noise, the queue consists of only one sample-and-hold amplifier. At a sampling rate of 20 Msamples/s, the peak signal-to-noise-and-distortion ratio (SNDR) is 45 dB, and the spurious-free dynamic range (SFDR) is 62 dB. The total power dissipation is 25.4 mW from 3.0 V. The active analog area is 0.11 mm^2.

Index Terms – Adaptive systems, analog-digital conversion, calibration, CMOS analog integrated circuits.

I. Introduction

Traditional designs of high-performance ADCs have required high-performance operational amplifiers (op amps). In many cases, single-stage op amps have been chosen to provide both high gain and high speed. As CMOS process geometries continue to shrink, however, the open-loop gain of single-stage op amps is decreasing. To overcome this problem, digital background calibration can be used to adjust for the effects of reduced open-loop gain. Background calibration is transparent to the ADC user and can track variations caused by changes in temperature, unlike foreground calibration done at power up. Also, the cost of digital calibration is decreasing due to the scaling of CMOS technologies. As a result, digital-background calibration can potentially allow the cost-effective design of high-performance analog-to-digital converters with low-performance op amps.

In this paper, the application of queue-based digital-background calibration to an 8-bit algorithmic ADC is described [1]. To reduce power dissipation, the length of the calibration queue is reduced from two sample-and-hold amplifiers (SHAs) in [2] to one here. A resolution of 8 bits is selected to demonstrate that calibration is potentially useful at a level where it has not traditionally been required or used.

II. Queue-Based Background Calibration

Fig. 1(a) shows a block diagram of an ADC with a calibration queue. The input to the queue, $x(t)$, is sampled at a rate f_S, which is slightly less than the ADC conversion rate, f_C. The difference between these two rates allows the ADC to occasionally process a calibration signal, while the queue stores one or more samples of the input signal. When the queue consists of two SHAs [2], the time allowed for the ADC to complete a calibration must be less than two input sampling periods or $2/f_S$. An advantage of this method is that this calibration interval is long enough to do a highly accurate calibration. However, a disadvantage of this method is that although one SHA is necessary to achieve excellent dynamic performance, the second SHA is extra and adds extra noise to the input signal. To overcome this problem, the calibration queue in this paper uses only one SHA.

Fig. 1b shows a simplified timing diagram. Impulses in "Sample" show times when the SHA begins sampling the input. Impulses in "Convert" show times when the ADC begins a conversion. "Full" is high when the queue holds an input sample. Once a sample is completely transferred to the ADC, Full is reset. Because $f_C > f_S$, the interval during which samples are held in the queue decreases over time at first. When the ADC is available to begin a conversion while the queue is empty, "Calibrate" rises, and the ADC instead converts a calibration signal, which is introduced directly at the ADC input, bypassing the SHA. The information obtained by these calibration operations is used to overcome limitations that would otherwise occur because of finite op-amp gain and capacitor ratio errors. The use of a queue with two SHAs allows nearly identical conversion and sample rates. However, when the queue consists of only one SHA, the ratio of these rates must be increased.

The queue has three distinct modes of operation: acquisition, hold, and transfer to the ADC. During the acquisition time t_A, a new input sample is acquired and a valid SHA output is not available. Any conversion begun by the ADC during t_A cannot be used to quantize an input sample. During the transfer time t_T, the SHA output must be held constant and another input

sampling operation is not allowed to begin. Fig. 1*c* shows a detailed worst-case timing diagram of Sample and Convert in the synchronous case, where T_S is $n+1$ periods and T_C is n periods of one master clock. In general, n is an integer, and $n = 3$ in this example. When Sample rises, the SHA starts to acquire the input signal. When Sample falls, the acquisition of the SHA input is complete. When Convert rises, the ADC starts to acquire its input, which comes from either the SHA output or the calibration input. When Convert falls, the acquisition of the ADC input is complete. The first rising edges of Sample and Convert are assumed to occur at the same time. Also, $T_{CAL} = T_C$ is assumed, where T_{CAL} is the time required by the ADC to convert a calibration signal and T_C is the conversion time for input samples stored by the queue.

During the first T_C period, a calibration is done because the acquisition of the input is not complete when the ADC is ready to begin a new conversion. During the calibration, the input acquisition is completed, and the resulting sample must be transferred to the ADC before another acquisition can begin. Therefore, the first T_S interval in Fig. 1*c* must be at least $T_{CAL} + t_T$. Since $T_{CAL} = T_C$ is assumed,

$$\frac{f_C}{f_S} = \frac{T_S}{T_C} > 1 + \frac{t_T}{T_C} \tag{1}$$

During the next nT_C intervals, input signals stored by the SHA are quantized by the ADC, and the delay between the end of the acquisition time and the beginning of the conversion time decreases because $T_C < T_S$ by design. In the last T_C period before the process repeats, the delay between the rising edges of the sample clock and convert clocks is minimum. To guarantee that a conversion begins in this interval instead of a calibration, this delay must be at least as long as t_A so that the acquisition is complete when the ADC is ready to start conversion. After this last T_C period, the rising edges of the sample and convert clocks again occur at the same time. Therefore, the last T_S interval in Fig. 1*c* must be at least as long as $T_C + t_A$. In other words,

$$\frac{f_C}{f_S} = \frac{T_S}{T_C} > 1 + \frac{t_A}{T_C} \tag{2}$$

As a result, both conditions (1) and (2) must be satisfied in the synchronous case.

III. Pipelined Algorithmic Architecture with Calibration

In the prototype algorithmic ADC, the residue gain g is less than 2 so that charge injection, comparator offset, and op-amp offset do not cause stage outputs to exceed the full-scale input range of the next stage [3]. The digital calibration adaptively determines g by measuring the major-carry jump and uses this information to appropriately weight the output bits, thus eliminating the effect of the reduced gain g on ADC linearity [2].

In a traditional algorithmic ADC, one comparator determines a single decision each time the residue goes around the loop. In practice, two SHAs are used in the loop because each SHA by itself does not sample its input while producing an output. Since two SHAs are used, the maximum sample rate of an algorithmic ADC can be doubled by using one comparator at the output of each SHA instead of only one comparator for both SHAs [4]. With two comparators, however, the loop has two residue gains. These gains are nominally set equal, but they may mismatch in practice. Although these two gains can be measured separately in principle, the calibration here calculates a single gain, which is a weighted average of the two possibly different gains. This approach is effective in overcoming linearity errors to the extent that the two gains match each other. Since about 8-bit gain matching is expected in practice, and since the prototype is expected to have 8-bit resolution, this approach should be satisfactory here.

Another consequence of the use of only one SHA is that when the ADC enters the calibration mode, the calibration must be complete in less than one sample period instead of two sample periods with two SHAs in the queue. Therefore, the result of each individual calibration interval is not as accurate as in [2]. However, if the calibration is intended to track variations in the residue gain that only occur slowly (from changes in temperature for example), each individual calibration measurement need not be highly accurate by itself. Instead, the individual calibration measurements must only converge to an accurate value after averaging the results from many calibration cycles. To allow this averaging to occur without a limitation arising from quantization noise, dither is added to the calibration signal V_{cal} [5].

For a white Gaussian dither signal, at least 0.5 LSB rms is required [6]. This dither causes the major-carry jump to take on a variety of values that when averaged determine the residue gain to a greater accuracy than would otherwise be possible. However, adding noise to the calibration input adds noise to the value of g that is determined by the calibration. To overcome this problem, the step size in the adaptive calibration loop can be reduced so that the noise power at the ADC output is not significantly increased by the presence of the dither. The disadvantages of this approach are that it increases the number of cycles required for the calibration to converge, and it reduces the rate at which the calibration can track changes in the residue gain.

IV. Prototype Implementation

The prototype uses three op amps (one for the queue and two for the ADC) and two comparators. Control logic for the ADC and queue is implemented on the prototype as well as output latches and buffers. The digital calibration is performed off chip.

Fig. 2*a* shows a simplified schematic of a residue amplifier. A differential circuit with two inputs (V_{ip} and V_{in}) and two outputs (V_{op} and V_{on}) is used in practice. In the differential circuit, the left side of C_s is connected to the left side of its differential counterpart and otherwise floated during ϕ_2, providing some common-mode rejection [7]. Here, d represents the binary decision of the corresponding comparator. A standard two-phase nonoverlapping clock is used. Clock phase ϕ_1' falls slightly before ϕ_1 to reduce signal-dependent charge-injection errors [8]. These clocks run at the master clock frequency of 120 MHz. With an ideal op amp, the stage gain would be approximately $97.5/50 = 1.95$. The SHA used in the queue is the same as this residue amplifier with the exceptions that C_r and its switches are removed, C_s and C_f are equal, and no connection to a comparator is made.

Fig. 2*b* shows a schematic of the op amp. It consists of a pair of cascoded common-source amplifiers. Cascodes are used to reduce the Miller effect and the input capacitance, increasing the feedback factor and the speed for a given power dissipation. Since a tail current source is not used, the common-mode gain of the differential pair is not suppressed, and feedback to the

V_{i+} and V_{i-} inputs controls not only the differential output voltage but also the common-mode output voltage. This op amp was chosen for its simplicity and speed in keeping with the goal of relaxing the required gain through digital calibration. With an op-amp gain of a and a parasitic capacitance from each op-amp input to ground of C_p, the differential residue amplifier output $V_{od} = V_{op} - V_{on}$ is

$$V_{od} = \left(\frac{C_s}{C_f + \dfrac{C_f + C_s + C_r + C_p}{a}} \right) V_{id} \pm \left(\frac{C_r}{C_f + \dfrac{C_f + C_s + C_r + C_p}{a}} \right) V_{rd} \qquad (3)$$

where $V_{id} = V_{ip} - V_{in}$ is the differential input and $V_{rd} = V_{rp} - V_{rn}$ is the differential reference. Calculation shows that C_p is about 170 fF, and simulation shows that a is about 160. Therefore, the gain applied to the input in (3) is about 1.86. This gain is about 4.4% less than the gain with an ideal op amp and would limit the uncalibrated ADC linearity to less than 5 bits.

For testing, the sampling clock frequency is the master clock frequency divided by six, which is 20 Msamples/s. The conversion clock frequency is the master clock frequency divided by five or 24 Msamples/s, but one out of every six conversions operates on a calibration signal instead of the input. Each algorithmic stage produces one output bit each master clock cycle; therefore, five cycles are required to produce a raw output of 10 decisions. The digital output is truncated to 8 bits after the calibration calculations.

Two comparator decisions are produced on each cycle of the master clock, which is divided into two nonoverlapping phases of equal duration. As a result, each clock phase produces one comparator decision. The duration of each phase must be long enough to allow an op amp to settle. Since each ADC output consists of 10 comparator decisions, the op-amp settling time must be less than $T_C/10$, where T_C is the ADC conversion time. The transfer time t_T in (1) is limited by the settling time of the op amp in the queue. Since all the settling times are assumed equal, one phase of the master clock is allocated for t_T. Therefore, $t_T = T_C/10$. For the prototype, $t_A = 4.9$ ns and the maximum ADC conversion rate is 24 Msamples/s. Therefore, $T_C \geq 41.7$ ns and $t_T \geq 4.17$ ns. For $f_C = 24$ Msamples/s, (1) gives $f_C/f_S > 1.10$, and (2) gives $f_C/f_S > 1.12$ for synchronous operation. As a result, the conditions described in the previous

paragraph with $f_C/f_S = 1.2$ satisfy (1) and (2). In contrast, with a queue of two SHAs, f_C/f_S as low as 1.0006 was demonstrated [2]. The difference between these two cases is that the time required for acquisition and transfer can be accommodated within the second sampling interval when two SHAs are used in the queue but increases the required f_C/f_S ratio with only one SHA.

V. Experimental Results

Fig. 3 shows the integral nonlinearity (INL) without calibration as well as the INL and the differential nonlinearity (DNL) with calibration. The sample rate is 20 Msamples/s; the conversion rate is 24 Msamples/s, and the frequency of the analog input is 540 kHz. In Fig. 3(a), g is set equal to 1.95, which is C_s/C_f, the closed-loop gain with perfect matching and infinite op-amp gain. The peak INL is 8.0 LSB at an 8-bit level. In Fig. 3(b) and (c), the calibration loop is allowed to converge using a Gaussian dither signal with a standard deviation of approximately 3.9 mV or 1 LSB. With calibration, the peak INL and DNL are 0.72 LSB and 0.71 LSB, respectively. The corresponding steady-state value of g is found to be 1.7887, which is about 8.3% less than the residue gain with an ideal op amp and about 3.8% less than the residue gain when the simulated finite op-amp gain is taken into account. Furthermore, the measured value of g increases to 1.8486 when the input sample rate and conversion rate are reduced to 13.3 Msamples/s and 16 Msamples/s, respectively. The decrease in g from 1.8486 to 1.7887 is attributed to incomplete op-amp settling, which causes a constant gain error if slew rate errors are negligible. The ability of the calibration loop to track closed-loop gain errors caused not only by capacitor mismatch and finite op-amp gain, but also by incomplete linear settling is an advantage of the proposed background calibration method.

Finally Fig. 4 shows the die photograph, and Table 1 summarizes the performance.

Acknowledgment

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References

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Figure and Table Captions

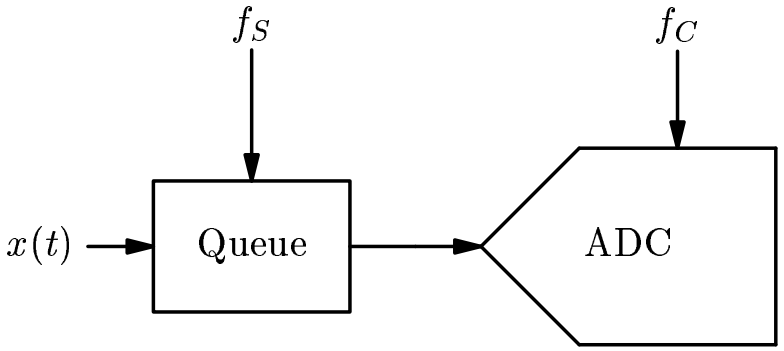
Fig. 1: (*a*) Block diagram of an ADC with a calibration queue, (*b*) simplified queue timing diagram, and (*c*) worst-case queue timing diagram in the synchronous case.

Fig. 2: (*a*) Simplified residue-amplifier schematic and (*b*) op-amp schematic.

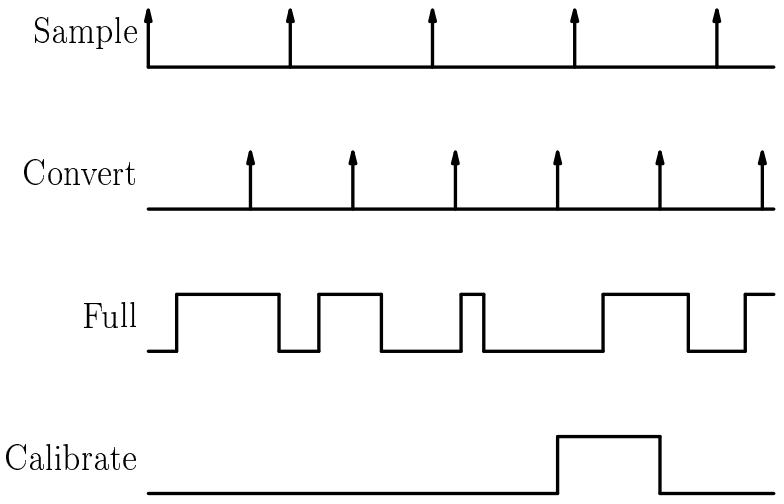
Fig. 3: (*a*) Integral nonlinearity (INL) versus code without calibration, (*b*) INL versus code with calibration, and (*c*) Differential nonlinearity (DNL) versus code with calibration. The sample rate is 20 Msamples/s, and the input frequency is 540 kHz.

Fig. 4: Die photograph.

Table I: Measured Performance (3 V and 25°C)



(a)



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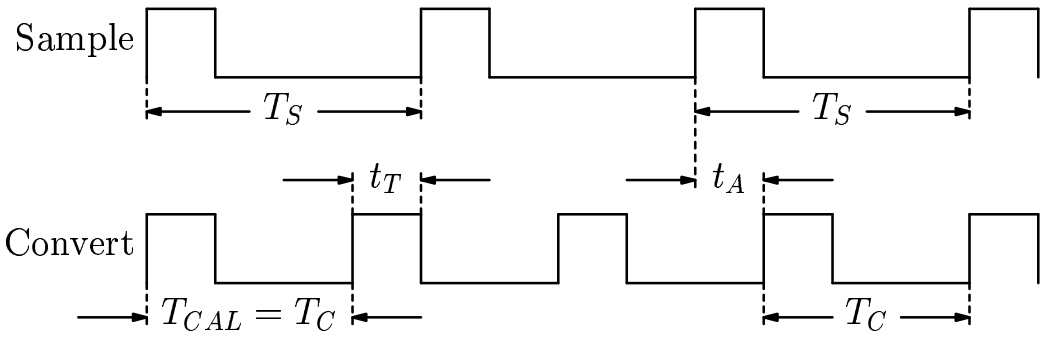
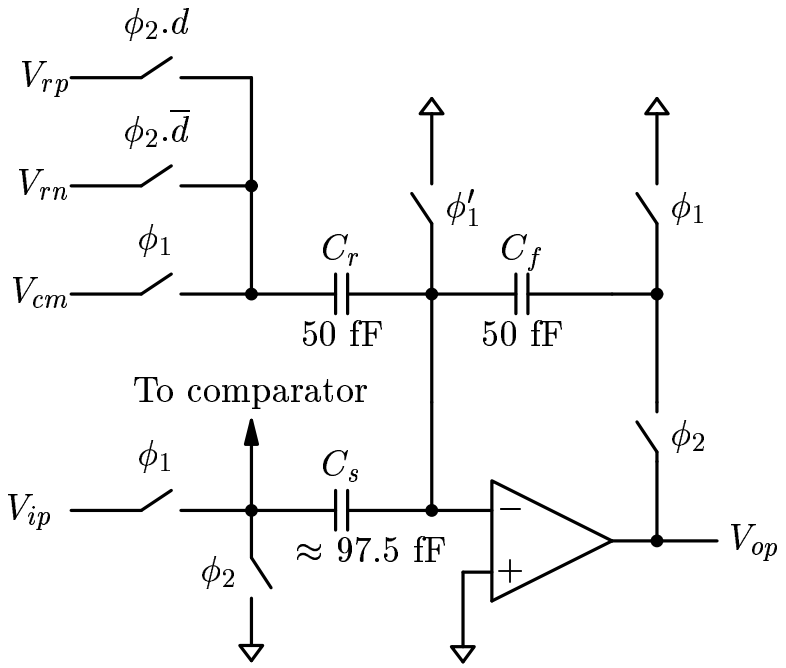
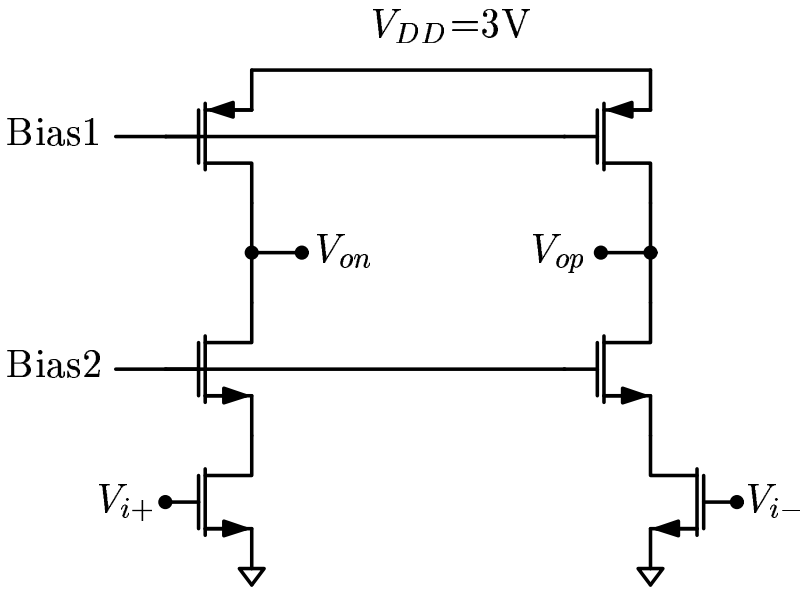


(c)

Fig. 1. (a) Block diagram of an ADC with a calibration queue, (b) simplified queue timing diagram, and (c) worst-case queue timing diagram in the synchronous case.

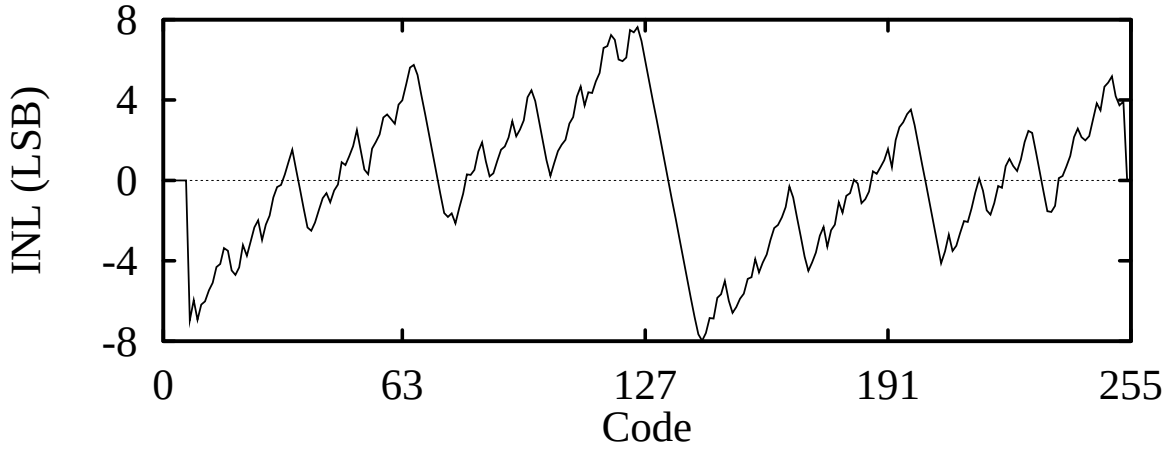


(a)

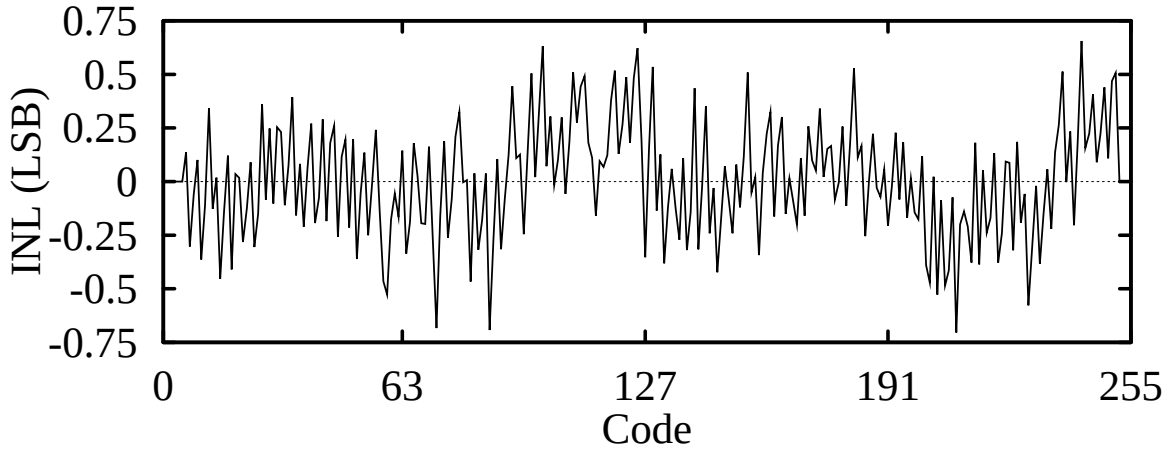


(b)

Fig. 2. (a) Simplified residue-amplifier schematic and (b) op-amp schematic.



(*a*)



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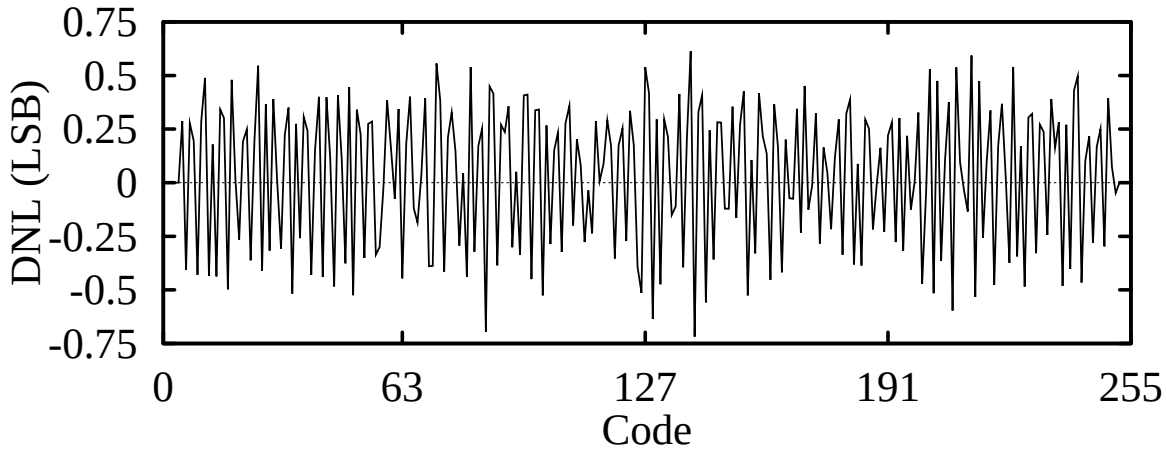

(*c*)

Fig. 3. (*a*) Integral nonlinearity (INL) versus code without calibration, (*b*) INL versus code with calibration, and (*c*) Differential nonlinearity (DNL) versus code with calibration. The sample rate is 20 Msamples/s, and the input frequency is 540 kHz.

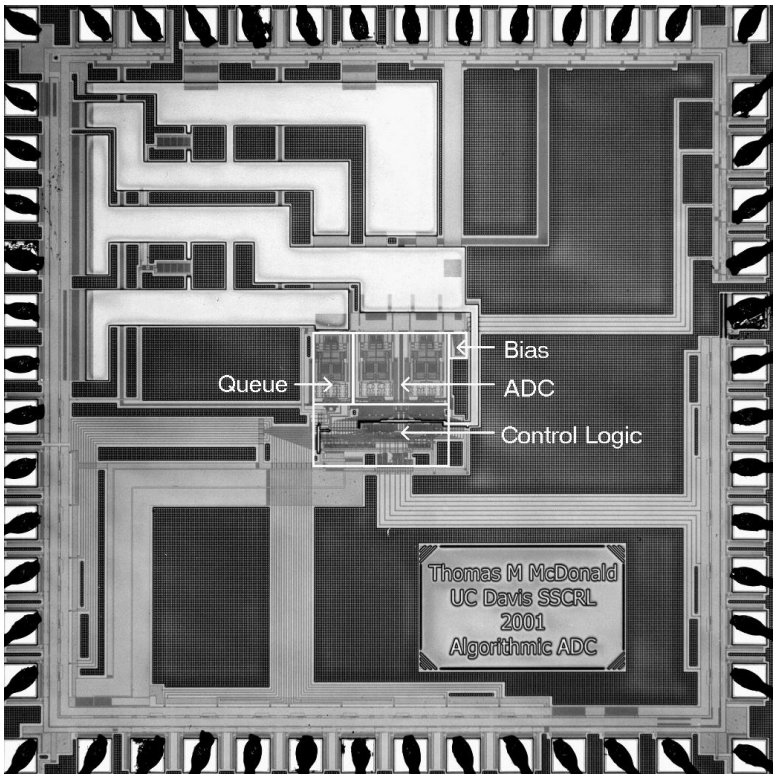

Fig. 4. Die photograph.

TABLE I
MEASURED PERFORMANCE (3 V AND 25°C)

Process	0.35-μm double-poly CMOS
Resolution	8 bits
Sampling rate	20 Msamples/s
Die Size	2.17 mm by 2.17 mm
Total Active Area	0.18 mm^2
Analog Active Area	0.11 mm^2
Analog Power Diss.	11.0 mW
Digital Power Diss.	1.9 mW
Pad Driver Power Diss.	12.5 mW
Total Power Diss.	25.4 mW
Full-Scale Input	1 V peak-to-peak
INL	-0.68 LSB to 0.72 LSB
DNL	-0.71 LSB to 0.61 LSB
THD (f_{in} = 5.9 MHz)	-59 dB
SNDR (f_{in} = 5.9 MHz)	45 dB
SFDR (f_{in} = 5.9 MHz)	62 dB
SNDR (f_{in} = 101 MHz)	39 dB
SFDR (f_{in} = 101 MHz)	52 dB