

A 12-bit 20-MS/s Pipelined ADC with Nested Digital Background Calibration*

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ABSTRACT

A 12-b 20-MS/s pipelined ADC is calibrated using an algorithmic ADC, which is itself calibrated. With background calibration, the peak SNDR and SFDR of the pipeline are 70.8 dB and 93.3 dB, respectively. The total power dissipation is 254 mW from 3.3 V. The active area is 7.5 mm² in 0.35- μ m CMOS.

I. INTRODUCTION

Background calibration improves ADC linearity without interrupting the input conversion. Previously used background-calibration techniques have: (1) limited the input signal bandwidth below half the sampling rate [1]; (2) reduced the input dynamic range through the addition of a calibration input [2], and/or (3) used analog techniques that do not readily scale to new process technologies [3], [4]. In principle, these problems can be eliminated by comparing the output of the ADC under calibration to that of a reference ADC. However, the linearity of the reference ADC limits the accuracy of this approach. To overcome this limitation, the reference ADC can use an algorithmic architecture that is itself calibrated to achieve the required linearity. The calibration of algorithmic ADCs is simple because their performance depends primarily on one parameter: the residue gain [5–7].

II. PIPELINED ADC CALIBRATION

The block diagram of the system is shown in Fig. 1. The combination of the input sample-and-hold amplifier (SHA), the pipelined ADC core (which has thirteen 1.5-b stages), and the digital-correction block forms a conventional pipelined ADC that produces the uncalibrated pipelined output by removing redundancy to overcome the effects of comparator offsets on the pipelined ADC linearity. The raw code of the pipelined ADC consists of two comparator outputs per stage and contains information about interstage gain errors in the pipeline. This information is extracted in the digital error estimation (DEE) block and combined with the uncalibrated output to produce the calibrated output of the pipelined ADC. Meanwhile, the algorithmic ADC samples some of the SHA outputs. Corresponding pipelined and algorithmic outputs are subtracted, producing an error, e , which adjusts the DEE output for a given input. Negative feedback and accumulators in the DEE block minimize the average value of e^2 , and the

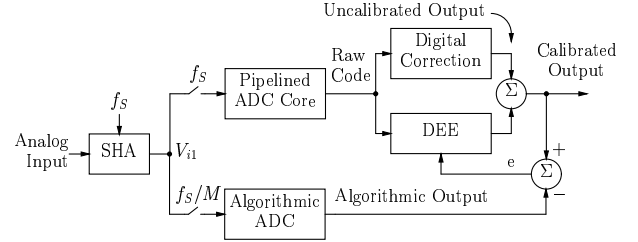
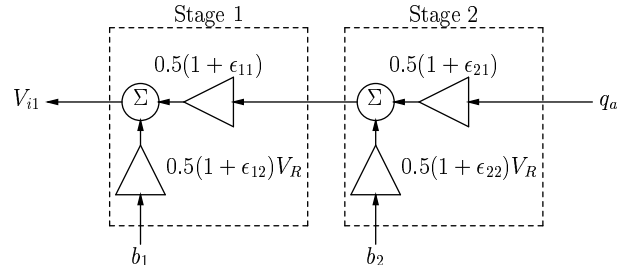


Fig. 1. Block diagram of pipelined ADC with calibration.

calibrated output approaches the algorithmic output in steady state.

In conventional 1.5-b/stage pipelines, interstage SHAs use feedforward that gives an ideal input gain of $1 + C_S/C_F$ and a DAC gain of C_S/C_F , where C_S and C_F are the sampling and feedback capacitors, respectively. As a result, mismatch and finite op-amp gain both cause the input gain error to differ from the DAC gain error. Therefore, each stage contains three error sources that are to be removed by calibration: input gain error, DAC gain error, and SHA offset. With redundancy, interstage SHA offsets can be combined into one equivalent input-referred offset. Therefore, one correction term can compensate for all the interstage offsets, and $2K + 1$ parameters seem to be required to calibrate K stages.



$$V_{i1} = V_R[0.5(1 + \epsilon_1)b_1 + (0.5)^2(1 + \epsilon_2)b_2] + q_a(0.5)^2(1 + \epsilon_3)$$

where

$$\epsilon_1 = \epsilon_{12}, \epsilon_2 = \epsilon_{11} + \epsilon_{22} + \epsilon_{11}\epsilon_{22}, \text{ and } \epsilon_3 = \epsilon_{11} + \epsilon_{21} + \epsilon_{11}\epsilon_{21}$$

Fig. 2. Calculation of the input of a two-stage pipelined ADC for calibration. In stage k , b_k is the raw digital output; ϵ_{k1} is the the output gain error, and ϵ_{k2} is the DAC gain error. The quantization error or residue of the last stage is q_a .

The calibration concept for the pipelined ADC is to calculate the input that corresponds to each raw output code. Fig. 2 shows how the input V_{i1} of a 2-stage pipelined ADC can be calculated from the quantization error or residue of the last stage q_a and the raw digital outputs of the first and second stages b_1 and b_2 , respectively. Although there are four

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independent gain errors, only three parameters (ϵ_1 , ϵ_2 , and ϵ_3) are required for calibration. The detailed expressions for these three parameters are unimportant. Instead, the key point is that one parameter is associated with each raw digital output plus one more parameter is associated with the quantization error. This result can be extended to any number of stages, and $K + 2$ parameters (including one parameter to remove offset mismatch) can be used to calibrate K stages without any loss in generality.

Fig. 3 shows the DEE block. Since the first five pipelined stages are calibrated in the prototype, seven parameters are required for calibration. Each accumulator finds one parameter. For example, the bottom accumulator finds the part of the error e that is correlated with the raw output of the first stage in the pipelined ADC. The result is ϵ_1 , which accounts for DAC gain error in the first stage as in Fig. 2.

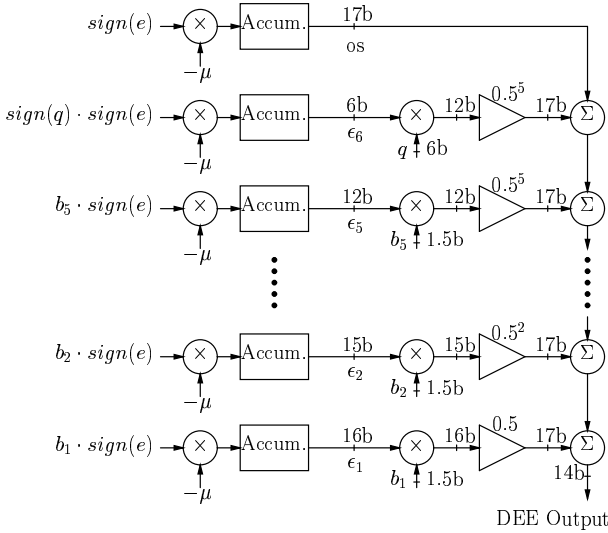


Fig. 3. Structure of the DEE (digital error estimation) block. $\text{sign}(e) = \pm 1$ and q is the first 6 bits of the digital code of q_a , which is the residue of the fifth stage. All accumulators are 20-bits wide.

III. ALGORITHMIC ADC CALIBRATION

Calibration of algorithmic ADCs has been demonstrated previously [5–7]. In [5], a trim array is used to adjust the residue gain to be as close to two as required. In [6], a digital calibration technique is described in which the ideal output of each stage during calibration was zero, allowing a residue amplifier stage with gain error to calibrate itself for errors introduced by capacitor mismatch. In [7], a digital calibration technique was described that could compensate for residue-gain errors introduced not only by capacitor mismatch, but also by finite op-amp gain. The key was to examine the ADC output instead of the stage output and adjust the relative weighting of consecutive digital outputs until the major-carry jump is one LSB. The major-carry jump was measured by setting the ADC input to zero and finding the ADC output when the MSB was set to one (which is D_1) and when the MSB was set to zero (which is D_0). Then $D_1 - D_0 = 1$ LSB under ideal conditions. An error $D_1 - D_0 - 1$ LSB was

computed, and negative feedback adjusted the weighting of the comparator outputs to minimize the mean-squared error.

With this approach, a single comparator is used in the algorithmic ADC, and the residue amplifier gain is reduced so that nonidealities (such as nonzero offset in the comparator and the residue amplifier and residue amplifier gain error) do not produce residue outputs that saturate the remaining conversion range [8]. To increase the amount of comparator and residue amplifier offset that can be tolerated without reducing the residue gain, the algorithmic ADC described in this paper uses two comparators in a 1.5-b/stage configuration [9], [10]. This approach allows the core of the algorithmic ADC to consist of one stage of the pipelined ADC, increasing modularity. Fig. 4 shows an ideal plot of the residue versus the input. Since two comparators are used, two residue jumps are present. To calibrate, the algorithmic ADC input is set approximately equal to the upper comparator threshold ($V_R/4$), and the output is measured twice yielding D_1 when the MSB is forced to $+1$ and D_0 when it is forced to 0. Then the process is repeated for the lower comparator threshold ($-V_R/4$), yielding D_3 when the MSB is forced to 0 and D_2 when it is forced to -1 . Under ideal conditions, $D_3 - D_2 = D_1 - D_0 = 0$. This result stems from the fact that the 1.5-b/stage architecture provides redundancy. As a result, the algorithmic ADC output should be unchanged if the output of either comparator is reversed for an input close to the threshold of that comparator. With constant residue gain error, $D_3 - D_2 = D_1 - D_0$, but the differences are not equal to 0. Some errors, such as common-mode-to-differential conversion in the residue amplifier, cause $D_3 - D_2 \neq D_1 - D_0$. To compensate completely for constant gain errors and partially for asymmetry in the residue amplifier transfer characteristic, the calibration adjusts the digital weighting between adjacent bits to minimize $(D_1 - D_0)^2 + (D_3 - D_2)^2$.

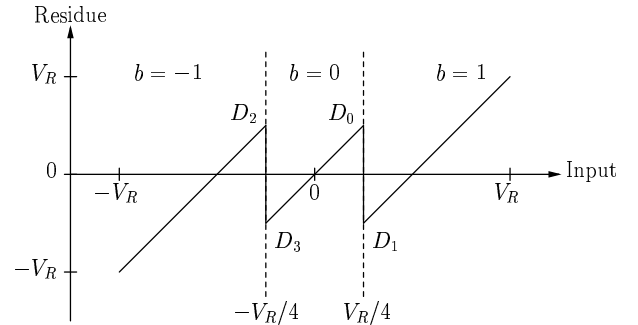


Fig. 4. Residue plot for 1.5b/stage resolution.

The algorithmic ADC rotates through the following sequence. First, it samples and digitizes the output of the SHA in Fig. 1 (V_{i1}). Then, it samples $V_R/4$ to find D_1 . Then, it samples V_{i1} again followed by $V_R/4$ to find D_0 . Next, it samples V_{i1} again followed by $-V_R/4$ to find D_3 . Then, it samples V_{i1} again and finally $-V_R/4$ to find D_2 . This sequence repeats indefinitely. Therefore, the algorithmic ADC alternates between operating on the output of the SHA in Fig. 1 (V_{i1}) and on a calibration input. A feature of the

nested calibration structure used here is that the algorithmic ADC inherently operates in the background for all these inputs because its output is used only to calibrate the pipelined ADC.

IV. PROTOTYPE

Folded-cascode op-amps [11] are used in both the pipelined and the algorithmic ADCs. The comparators in both ADCs use a preamp and the same schematic as in [12]. The input SHA uses a flip-around structure with a folded-cascode op-amp to provide high common-mode input range [13].

The sampling capacitance is scaled in several of the pipelined stages to reduce power dissipation [14], [15]. The sampling capacitance in the input SHA in Fig. 1 is 6 pF. For the next four SHAs in the pipelined ADC, the sampling capacitance is 2 pF, 0.9 pF, 0.4 pF, and 0.2 pF, respectively. The rest of the stages in the pipeline use a sampling capacitance of 0.1 pF. The sampling capacitance in the algorithmic ADC is 0.2 pF. As a result, thermal noise limits its SNDR to about a 9b–10b level. However, noise in the algorithmic ADC is not a limitation here because its effect is reduced by averaging in the accumulators in Fig. 3.

Fig. 5 shows a photograph of the fully differential prototype, which was fabricated in 0.35 μ m CMOS. It includes the input SHA, a pipelined ADC with 14 outputs and an algorithmic ADC with 16 outputs. Other blocks in Fig. 1 have been implemented in software.

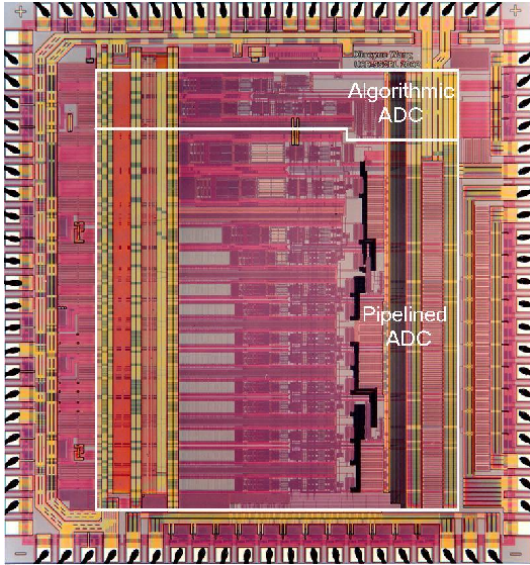


Fig. 5. Die Photo.

V. EXPERIMENTAL RESULTS

Fig. 6 shows the INL of the algorithmic ADC without and with calibration. The sampling and conversion rate of the algorithmic ADC is 1.25 MS/s, but half of its outputs correspond to samples of V_{i1} in Fig. 1, and the other half stem from calibration inputs. Therefore, the input sample rate is 0.625 MS/s.

Fig. 7 shows the INL of the pipelined ADC without and with calibration and the DNL with calibration. The sample rate is 20 MS/s.

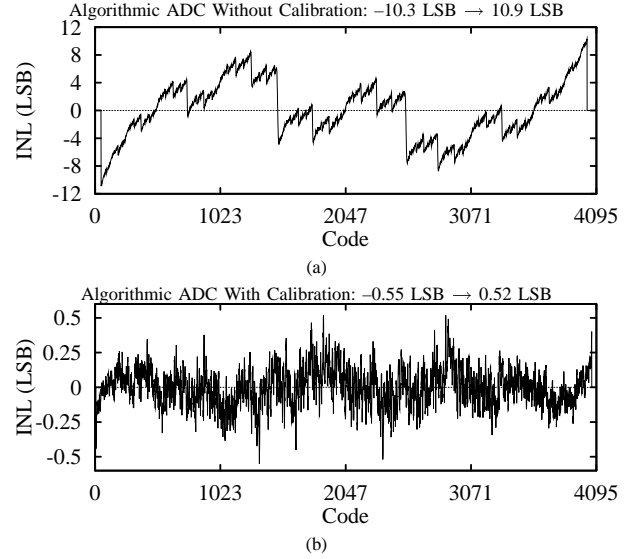


Fig. 6. Integral nonlinearity (INL) of the algorithmic ADC: (a) without calibration and (b) with calibration. The input sample rate is 0.625 MS/s.

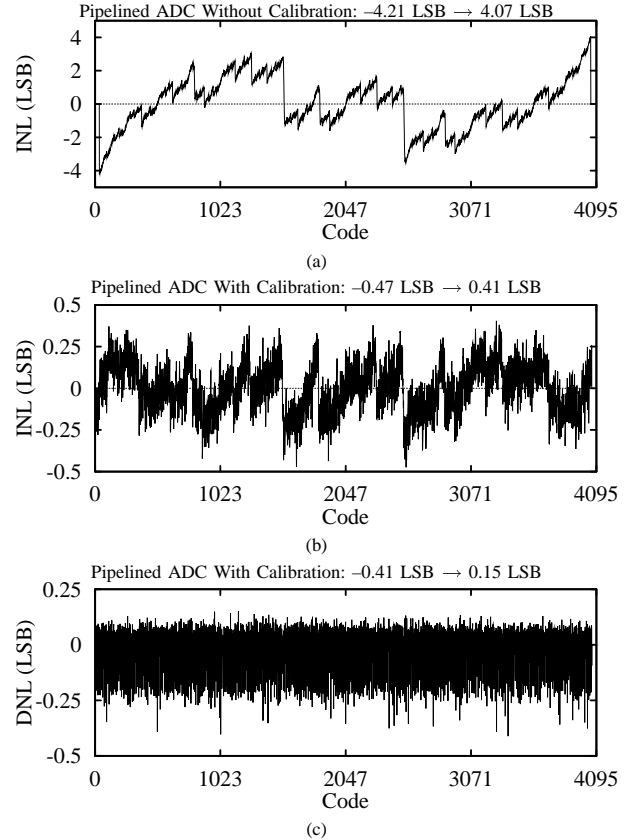


Fig. 7. (a) Integral nonlinearity (INL) of the pipelined ADC without calibration, (b) INL of the pipelined ADC with calibration, and (c) Differential nonlinearity (DNL) of the pipelined ADC with calibration. The sample rate is 20 MS/s.

Fig. 8 shows the measured output spectra of the pipelined ADC without and with calibration. The sampling and conversion rate of the pipelined ADC is 20 MS/s, but its output was down-sampled by a factor of 4 on chip to reduce the

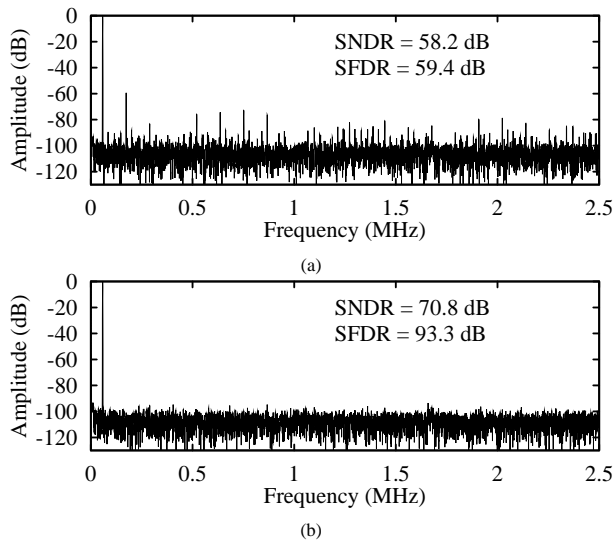


Fig. 8. Pipelined ADC output spectra for $f_s = 20\text{MS/s}$ (down-sampled by a factor of 4), $V_{in} = 1.6\text{ Vp-p}$ and $f_{in} = 58\text{kHz}$: (a) without calibration and (b) with calibration.

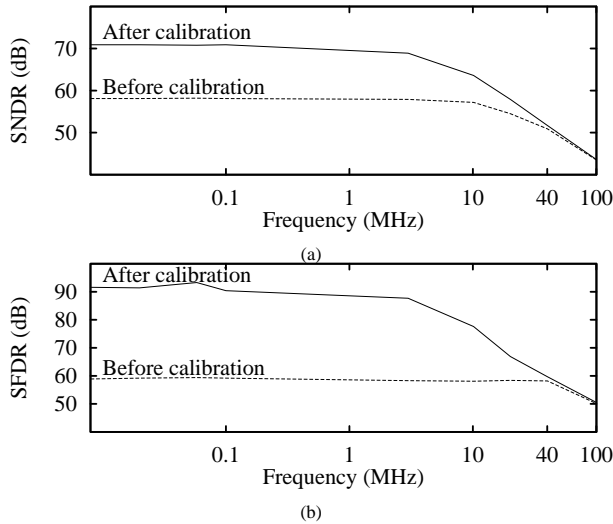


Fig. 9. (a) SNDR and (b) SFDR versus input frequency for the pipelined ADC with $f_s = 20\text{MS/s}$.

required number of output pins. (Each output buffer handles 3 or 4 bits.) Therefore, the plots in Fig. 8 extend to half the pipelined down-sampled rate, or 2.5 MHz. With calibration, the SNDR of the pipelined ADC is 70.8 dB; the SFDR is 93.3 dB, and the THD is -92.9 dB .

Fig. 9 shows the measured SNDR and SFDR of the pipelined ADC versus frequency without and with calibration. The measured results are summarized in Table I.

VI. CONCLUSION

A pipelined ADC with nested digital background calibration based on LMS algorithm has been presented. With calibration, the SNDR of the pipelined ADC is 70.8 dB; the SFDR is 93.3 dB, and the THD is -92.9 dB at 20 MS/s.

TABLE I
MEASURED PERFORMANCE (3.3V AND 25°C)

	Without Cal.	With Cal.
Process	0.35 μm 2P4M CMOS	
Sampling rate	20 MS/s	
Active area	7.5 mm ²	
Full-Scale Input	1.6 Vp-p	
Resolution	9 b	12 b
Analog Power Diss.	190 mW	226 mW
Total Power Diss.	217 mW	254 mW
Max. INL (Alg. ADC)*	10.9 LSB	0.55 LSB
Max. DNL (Alg. ADC)*	0.99 LSB	0.28 LSB
Max. INL (Pip. ADC)*	4.21 LSB	0.47 LSB
Max. DNL (Pip. ADC)*	0.60 LSB	0.41 LSB
SNDR (Alg. ADC)*	49.6 dB	59.6 dB
SFDR (Alg. ADC)*	50.9 dB	78.4 dB
SNDR (Pip. ADC)*	58.2 dB	70.8 dB
SFDR (Pip. ADC)*	59.4 dB	93.3 dB
THD (Pip. ADC)*	-59.4 dB	-92.9 dB
PSRR*	65.0 dB	64.8 dB
CMRR*	73.6 dB	73.4 dB

* $f_{in} = 58\text{ kHz}$

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