A Mixed-Signal RAM Decision-Feedback Equalizer for Disk Drives*

Bret C. Rothenberg†, James E.C. Brown, Paul J. Hurst and Stephen H. Lewis

Solid-State Circuits Research Laboratory
Dept. of Electrical and Computer Engineering
University of California, Davis, CA 95616 USA

ABSTRACT

A mixed-signal RAM decision-feedback equalizer (DFE) that operates at 90 Mb/s is described. The DFE cancels intersymbol interference caused by the past 4 decisions. The RAM contents are adapted using digital circuits. In steady-state operation, power dissipation is 260 mW. The active area is 4.5 mm^2 in a 1-µm CMOS process.

INTRODUCTION

Intersymbol interference (ISI) limits density in hard disk drives. The decision-feedback equalizer (DFE) in combination with a linear forward equalizer can be used in the read channel to cancel ISI [1]. Fig. 1 shows the block diagram of a disk-drive read channel that uses a DFE. The functional blocks are: preamp and automatic gain control (AGC), timing recovery, bandlimiting low-pass filter (LPF), forward equalizer, and DFE. The forward equalizer removes precursor ISI, and the DFE removes the postcursor ISI [2].

In a conventional DFE, a linear combination of past decisions is used to cancel the postcursor ISI. Such a DFE uses a transversal feedback filter in Fig. 1. The feedback filter can be replaced with a look-up table that contains the precomputed filter outputs for every sequence of past decisions. The look-up table can be implemented with a RAM; the resulting structure is referred to as a RAM-DFE [3,4]. A key advantage of the RAM-DFE is that the cancellation values can be any function of the past decisions, so linear and nonlinear postcursor ISI, as well as dc offset, can be canceled. A drawback of the RAM-DFE is that it adapts slower than a conventional DFE in principle because only one value in the RAM can be updated after each decision. In contrast, every coefficient can be updated after each decision in a conventional DFE. In practice, the RAM-DFE adaption time can be reduced by initially loading typical cancellation values into the RAM and/or by using broadcast training [3].

This paper focuses on a mixed-signal RAM-DFE for a disk-drive read channel. A mixed analog-digital implementation has some advantages when compared to a digital implementation [4]. One advantage is that the 7-bit front-end ADC is not needed. Another is that the digital forward equalizer, which is large, would be replaced by an analog forward equalizer [5-8]. These differences should reduce both die area and power dissipation.

RAM-DFE

The operation of a RAM-DFE can be explained using the block diagram in Fig. 2. The slicer makes a binary decision every bit period, T, and feeds a delay line that holds the past 4 decisions. These past decisions are used as an address for the RAM, which acts as a look-up table with 16 entries. The RAM holds a value for canceling the postcursor ISI for each possible sequence of past bits. The currently addressed value is read out from the RAM and used to cancel the postcursor ISI. This allows the slicer to make its binary decision, with little effect from ISI.

* Research sponsored by UC MICRO grants 94-121 and 95-139.
† B. Rothenberg is now with EXAR Corp., Fremont, CA. 94538.

The RAM contents are adapted using the least-mean-square (LMS) algorithm [2]. The LMS algorithm adjusts the RAM values to minimize the mean-squared error, where the error e_k is the difference between the slicer output and input. The LMS update equation is

$$R_{k+1}(Address_k) = R_k(Address_k) + \mu e_k . \qquad (1)$$

Here k is a time index and μ is the update gain. The $Address_k$ is formed by the past 4 binary decisions, $\hat{y}_{k-4}$, $\hat{y}_{k-3}$, $\hat{y}_{k-2}$, $\hat{y}_{k-1}$.

Fig. 3 shows a block diagram of the mixed-signal DFE. All the analog signals are fully differential. In each bit period, a selected value from RAM is converted to analog form by the DAC and added to the DFE input to cancel the postcursor ISI. The summed signal is converted to digital form by the ADC, which outputs the decision and error signals after some delay. The error signal is used to update the RAM output using a delayed version of (1), and the updated value is written back into the RAM.

The DAC input is selected using a two-step, pipelined process. At time k–2, the RAM outputs two values, corresponding to the two possible addresses that will be in the delay line when the next decision is made. These two outputs are latched, and at time k–1 the decision $\hat{y}_{k-1}$ selects one of them to send to the DAC. With this approach, the RAM has a full clock cycle to generate its outputs.

After each decision, the RAM must read out values for the DAC and update logic and write an updated value. To facilitate these operations, a static RAM with 2 read ports and 1 write port is used. The RAM size is 16x10 bits. The LMS update in (1) is implemented by a 10-bit saturating carry-select adder. Complementary pass-transistor logic is used in the adder [9].

During initial convergence (or training) of the RAM, the error e_k is quantized to a 3-bit level and a large μ value is used to give rapid convergence. In steady state, μ is reduced and the error is quantized to only a 1-bit level, allowing adaptation of the RAM contents to continue with most of the comparators in the flash ADC powered-down to reduce power dissipation.

The ADC uses a nonuniform flash structure with a comparator at zero to generate $\hat{y}_k$ and two uniform 3-bit error quantizers, each with 7 comparators, to generate e_k. The error quantizers are centered at $\pm$0.3V, which are the ideal amplitudes of the binary data at the ADC input. Each error quantizer spans a range of 0.23V. Each comparator consists of autozeroed inverters acting as an offset-canceled preamp [10] followed by cross-coupled inverters. In the low-power steady-state mode, 12 of the 15 comparators are powered off. The feedback DAC has 6-bit resolution and uses a metal resistor string with two-level output decoding to achieve high-speed operation.

The DFE input and DAC output are summed by the circuit shown in Fig. 4. The operation of the left half of this circuit is described next. The DFE input is sampled onto the parasitic capacitance at the input of inverter I1 by switch M1. (M3 cancels charge injection.) Identical inverters I1 and I3 are used as v-to-i converters to convert the sampled input and DAC output signals into currents, then the summed currents are converted back to a voltage by inverter I5 acting as a resistive load.

MEASURED DATA

The RAM-DFE was tested by generating a DFE input signal that contains postcursor but no precursor ISI, sending that signal through an arbitrary waveform generator, and adding bandlimited white Gaussian noise to the signal before it enters the DFE. The test signal was generated using a linear, Lorentzian channel model [1] with $PW_{50}=2T$ and a 5-tap finite-impulse-response forward equalizer.

A plot of measured bit-error rate (BER) versus signal-to-noise ratio (SNR) is shown in Fig. 5 for a data rate of 90 Mb/s. The data were gathered by adapting the RAM contents (initially zero), and then measuring BER once the RAM had reached steady-state, with adaptation continuing using the 1-bit error signal. For comparison, simulated BER performance of an ideal DFE under identical conditions is also plotted. Measured performance is within 0.2 dB of the simulated performance for SNR $\leq$ 15 dB.

The die photo is shown in Fig. 6. The IC was fabricated in a 1-μm CMOS process. The active area of the RAM-DFE is 4.5 mm^2. The measured performance is summarized in Table 1.

REFERENCES

[1] J. W. Bergmans, "Density Improvements in Digital Magnetic Recording by Decision Feedback Equalization," *IEEE Trans. on Magnetics*, pp. 157-162, May 1986.

[2] M. L. Honig and D. G. Messerschmitt, *Adaptive Filters*, Kluwer Academic Publishers, Boston, 1984.

[3] K. Fisher, et. al., "An Adaptive RAM-DFE for Storage Channels," *IEEE Trans. on Comm.* , pp. 1559-1568 Nov. 1991.

[4] K. Fisher, et. al., "A 54 MHz BiCMOS Digital Equalizer for Magnetic Disk Drives ," *CICC,* pp. 19.3.1-4, May 1992.

[5] J. Sonntag, et. al., "A High-Speed Low-Power PRML Read Channel Device", *IEEE Trans. on Magnetics*, pp. 1186-1195, March 1995.

[6] B. Rothenberg, S. Lewis and P. Hurst, "A 20 MS/s Switched-Capacitor FIR Filter in 2 μm CMOS,"*ISSCC,* pp. 210-211, Feb. 1995.

[7] R. Gomez, M. Rofougaran and A. A. Abidi, "A Discrete-Time Analog Signal Processor for Disk Read Channels," *ISSCC,* pp. 212-213, Feb. 1993.

[8] R. Yamasaki, T. Pan, M. Palmer, and D. Browning, "A 72 Mb/s PRML Disk-Drive Channel Using an Analog Sampled-Data Signal Processor," *ISSCC,* pp. 278-279, Feb. 1994.

[9] K. Yano, et. al., "A 3.8-ns 16x16-b CMOS Multiplier Using Complementary Pass-Transistor Logic," *JSSC,* pp. 388-394, April 1990.

[10] A.G.F. Dingwall, "Monolithic Expandable 6-Bit CMOS/SOS A/D Converter," *JSSC,* pp. 926-932, Dec. 1979.

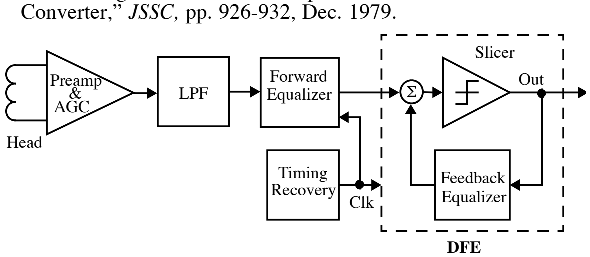

Fig. 1. DFE read channel.

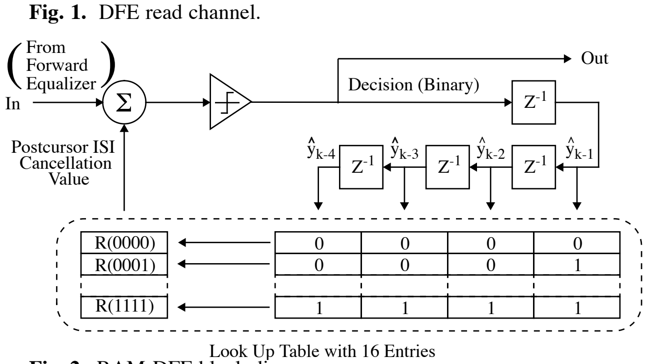

Fig. 2. RAM-DFE block diagram.

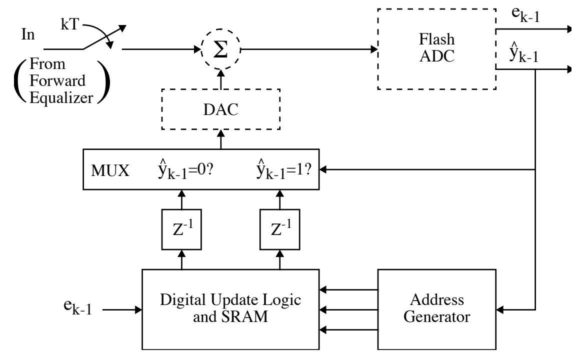

Fig. 3. Mixed-signal RAM-DFE. The analog blocks are shown with dashed lines.

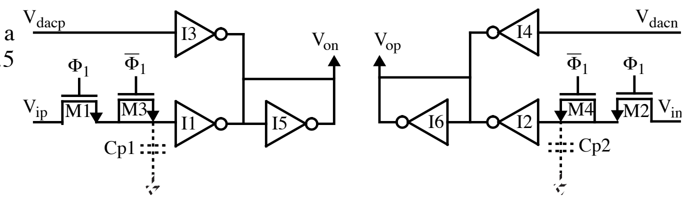

Fig. 4. Summer and input track-and-hold.

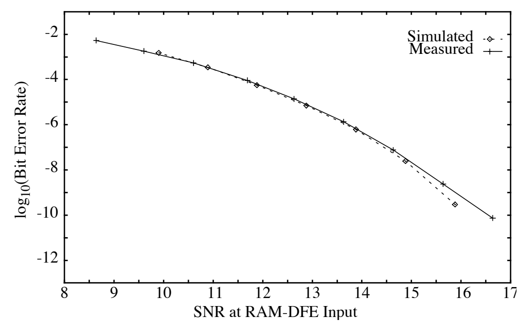

Fig. 5. Measured and simulated BER vs. SNR at 90 Mb/s.

Fig. 6. Die photograph.

Process	1-μm CMOS
Active Area	4.5 mm^2
Power (training/steady-state)	360 mW/260 mW
Data Rate	90 Mb/s
Training time	220 bit periods
RAM Size	16 x 10 bits
Error Quantization (training/steady-state)	3 bits / 1 bit
BER at SNR = 15 dB	2 x 10^{-8}

Table 1. Performance summary with Lorentzian channel model, 5 V supply and 25 ^{o}C.