CMOS CIRCUITS FOR THERMAL ASPERITY DETECTION AND RECOVERY IN DISK-DRIVE READ CHANNELS *

Aaron Lee
Dept. of ECE
UC Davis
(now with AMD)

Paul Hurst
Dept. of ECE
UC Davis

Kiyoshi Fukahori
TDK Semiconductor
Mountain View, CA

ABSTRACT

A thermal asperity detection and recovery scheme for a disk-drive read channel is presented. The circuit design and simulation results for two key blocks, the AC coupler and its tuning loop, in a 0.5μm CMOS process are described.

1. INTRODUCTION

In a modern disk drive, the read head flies so close to the media surface that they occasionally come into contact with each other. When this happens, a large voltage is generated at the output of the read head preamp, and this is called a thermal asperity (TA) [1]. Modern read channels include a TA detection and recovery circuit as part of the front end [2], which is shown in Fig. 1.

The read signal from the preamp, V_{in}, which is a band-pass signal, is input to the AC coupler (ACC), which is a high-pass filter. Then the variable gain amplifier (VGA) amplifies the signal to give the output signal V_{out}. This output signal is fed to the back end of the read channel to extract the data. Also, V_{out} is fed into a 1-pole low-pass filter that has a low bandwidth and outputs the average value of V_{out}, which is referred to as the baseline. The baseline is a constant (zero) under normal operation.

However, when a TA occurs, the baseline experiences a large shift as shown in Fig. 2. A large baseline shift makes data detection difficult and can cause bit errors, as the large amplitude change typically causes clipping in the VGA. The amplitude of the baseline can be used to detect a TA event. If the amplitude of the baseline is larger than some threshold, the comparator output goes high in Fig. 1. Then a signal from the state machine reduces the AC coupler time constant which reduces the time required for the baseline to return to zero. When the baseline falls to within a threshold of zero, the time constant in the AC coupler is returned to its nominal value.

Fig. 3 shows the schematic of the AC coupler. Each NMOS transistor is biased in the triode region with an on-resistance R_f. Assuming an ideal opamp, the circuit has a zero at dc, a pole at $-1/R_fC_f$, and a high-frequency gain of $-C_{in}/C_f$. In normal operation, it should have a well controlled time constant so it passes the entire read signal. We chose R_fC_f = 32ns (–3dB frequency = 5MHz). A tuning circuit is used to set the on-resistance of the transistors by controlling V_{tune} to set the time constant, as described in the next section.

The AC coupler includes two additional transistors in parallel with each M1' that are not shown in Fig. 3. These transistors are identical to M1', and they are normally off with their gates tied low. If a TA is detected, the gates of these transistors are connected to V_{tune}, reducing the time constant by a factor of three to more quickly return the baseline to zero.

A folded-cascode opamp [3] is used in this AC coupler to achieve high gain, large bandwidth and large output swing. With C_{in}=C_f, the opamp must have a unity-gain bandwidth that is about equal to the data rate. Here, the target data rate was 800Mbps, so this opamp dissipates a significant amount of power. To save power, the tuning circuit does not use a replica(s) of the AC coupler.

2. TIME CONSTANT TUNING CIRCUIT

A tuning circuit sets the on-resistance R_f in the AC coupler so that R_fC_f is constant despite changes in C_f due to process variations. For a NMOS device in the triode region with $V_{DS} << V_{GS} - V_t$, the on-resistance R_f is given by

$$R_f \cong \frac{1}{k'\frac{W}{L}(V_{GS} - V_t)} = \frac{1}{g_m}, \qquad (1)$$

so the on-resistance can be varied by adjusting V_{GS}. Eqn. (1) also shows the on-resistance R_f is about equal to $1/g_m$ of an identical, saturated transistor with the same gate and source voltages [3]. Therefore, if we can generate gate and source bias voltages in a reference circuit to give C_f/g_m = 32ns and apply them to M1', then R_f = $1/g_m$ and R_fC_f = 32ns. The tuning scheme used here is based on this idea.

The reference tuning loop uses a Gm cell in feedback as shown in simplified form in Fig. 4 [4]. A constant current I_R is pushed into the Gm cell, producing a voltage $V_{o1} = I_R/g_m$. ϕ_1 and ϕ_2 are two non-overlapping clocks with frequency f_{clock}. During ϕ_1, the capacitor C_1 is charged to V_{o1}. During ϕ_2, the charge on C_1 is transferred to capacitor C_H. Also, a constant current NI_R is drawn from C_H. The average value of the opamp output, V_{f2}, is used to tune the

* This research was funded by UC MICRO Grant 01-084, with support from Broadcom, Intel, Metalink, TDK Semiconductor and TI.

transconductance of the Gm cell.

When the loop reaches steady state, the charge injected onto C_H by C_1 during ϕ_2 equals the charge removed from C_H by NI_R in one clock period. Therefore V_{o2} is periodic and V_{f2} is constant. In steady state,

$$C_1 V_{o1} = NI_R T \ , \qquad (2)$$

where $T = 1/f_{clock}$ is the clock period. Substituting $V_{o1} = I_R/g_m$ into (2) and simplifying gives

$$\frac{C_1}{g_m} = NT = \frac{N}{f_{clock}} \ , \qquad (3)$$

where g_m is the transconductance of the Gm cell. Hence, C_1/g_m depends on the clock frequency f_{clock}, which is derived from a crystal oscillator, and N, the ratio of DC currents that can be accurately defined in a CMOS process.

A more detailed block diagram of the tuning loop is shown in Fig. 5. The clock frequency is 6.25MHz and the DC current ratio N is 0.2. Using these values in (3), C_1 / g_m = 32ns. If C_1 has the same nominal value as C_f (=0.6pF) in the AC coupler, then g_m = 18.8μA/V. With $I_R \leq$ 5μA in Fig. 5, the nominal differential output voltage of the Gm cell is $\leq$ 0.53V. To have a large g_m tuning range, the Gm cell should allow an output swing of >1.0V.

The opamp in the switched-capacitor (SC) integrator in Fig. 5 is a folded cascode. Its DC gain is about 75dB and its gain-bandwidth product is about 120MHz; both are sufficient for this application. The SC low-pass filter (LPF) in Fig. 5 has a bandwidth of about 800kHz. Because its bandwidth is not critical, a passive first-order filter is used to save power. A differential-to-single-ended converter converts the SC LPF output to voltage V_{f2} that sets the tail current and g_m of the Gm cell.

3. THE Gm CELL

Fig. 6 shows the schematic of the Gm cell in Fig. 5. It consists of a differential g_m stage, a common-mode feedback (CMFB) circuit, and an output buffer. The g_m stage consists of transistors M1-M7. M1 and M2 are diode-connected as in Fig. 5. M3-M6 form current sources controlled by the CMFB circuit. M7 is the tail current source with its current set by V_{f2}. Thus, the g_m of M1 and M2 is controlled by V_{f2}.

M201-M204 form the CMFB circuit. Because M1 and M2 are diode connected, the common mode (CM) output voltage can be controlled indirectly by controlling the voltage V_S at node S (the source of M1 and M2). The CMFB circuit forces the voltage V_S to be the same as the applied CM reference voltage V_{ref} = 1.2V.

M101-M103 generate V_{avg}, the average of V_{out+} and V_{out-}. M101, M102 and M103 are copies of M1, M3 and M5 (or M2, M4 and M6), respectively. M5, M6 and M103 mirror the current in M204. These currents are pushed into diode-connected M1, M2 and M101. When the input current is zero (I_R = 0 in Fig. 5), $V_{GS101} = V_{GS1} = V_{GS2}$ because $I_{D5} = I_{D6} = I_{D103}$ and M1 = M2 = M101. In this case, the average gate-to-source voltage of M1 and M2 is just V_{GS1}, which equals V_{GS101}. When I_R is not zero, V_{GS1} is increased by I_R/g_m and V_{GS2} is decreased by the same amount. Therefore the average of V_{GS1} and V_{GS2} is still equal to V_{GS101} and is equal to the DC bias value of the gate-to-source voltage of M1. So

$$V_{avg} = \frac{V_{out+} + V_{out-}}{2} = V_S + \frac{V_{GS1} + V_{GS2}}{2} \ . \qquad (4)$$

Since the CMFB circuit forces $V_S = V_{ref}$, we have

$$V_{avg} = V_S + \frac{V_{GS1} + V_{GS2}}{2} = V_{ref} + V_{GS101} \qquad (5)$$

Therefore the gate voltage of M101 is V_{avg}. V_{avg} is buffered by the voltage buffer formed by M301-M307 that outputs $V_{tune} = V_{avg}$. Circuitry that is not shown generates bias voltages V_{bias} and V_{casc}.

4. USING THE TUNING LOOP TO SET R_fC_f

The purpose of the tuning loop is to set the time constant in the AC coupler in Fig. 3. To do this, C_1 in Fig. 5 is equal to (a copy of) C_f in Fig. 3. Also, the on-resistance R_f of M1' in Fig. 3 is made equal to $1/g_m$ of M1 in Fig. 5. This is achieved by making M1' a copy of M1 and matching the gate and source voltages of M1 and M1'. The gate voltage of M1 is V_{tune} and its source voltage is V_{ref}. If the gate of M1' is connected to V_{tune} and the CM output voltage of the AC coupler is set to V_{ref} as indicated in Fig. 3, then M1 and M1' are biased identically.

One limitation of this tuning scheme is the limited tuning range of the g_m value. Another limitation is that this tuning approach depends on matching between C_f and C_1 and between M1 and M1'. Also, tuning accuracy is limited by offsets in the SC integrator and Gm cell in Fig. 5.

5. SIMULATION RESULTS

The tuning loop in Fig. 5 and the AC coupler in Fig. 3 were simulated using SPICE. In the simulations, all switches and opamps were realized with MOS transistors, and V_{DD} = 3.3V. The simulations used 0.5μm CMOS models, and the R_fC_f product was found for different $C_1 = C_f$. Simulation results are given in column 2 of Table 1 for I_R = 5μA.

Column 2 shows there is a 2% change in R_fC_f when C_1 changes from 1pF to 0.7pF. However, R_fC_f is less than the desired value of 32ns. Possible explanations are that (1) does not accurately describe the relationship between R_f and $1/g_m$ in this sub-micron process and/or parasitic capacitance in parallel with C_1 due to the MOS switches in Fig. 5 effectively increases C_1 so that it is not equal to C_f. For this application, the slightly low value of R_fC_f is acceptable. However, when C_1 is less than 0.6pF, the variation in R_fC_f becomes unacceptably large. This error is caused by nonlinearity in the Gm cell. The linear range of the Gm cell decreases as g_m decreases. To show that reducing nonlinearity reduces this error, the simulations

were repeated with I_R = 1μA. With a smaller input current to the Gm cell, nonlinearity is less of an issue and less change in the R_fC_f product is expected for small capacitance. This is verified by the simulation results in column 3 of Table 1, where the variation in R_fC_f remains small for a wider range of capacitance. As the capacitance changes from 0.4pF to 1pF (a 250% variation), R_fC_f only changes from 31.4ns to 29.6ns (a change of 6%). As the capacitance changes from 0.5pF to 0.7pF (a 40% change), the simulated variation in the R_fC_f product is less than 1%.

Table 1 Tuning Simulation Results

* Loop Does Not Converge

$C_1 = C_f$ (pF)	R_fC_f (ns) for I_R=5μA	R_fC_f (ns) I_R=1μA
1.10	*	*
1.00	29.60	29.60
0.90	29.88	29.79
0.80	30.08	29.92
0.70	30.24	30.10
0.60	31.62	30.24
0.50	34.90	30.40
0.45	54.45	30.56
0.40	*	31.40
0.30	*	33.00
0.25	*	42.50

6. CONCLUSION

A TA detection and recovery scheme for a read channel has been presented. The AC coupler and its tuning loop were described in detail. A Gm cell in the tuning loop is used here to control the on-resistance of a triode MOS transistor in the AC coupler. This approach differs from [4], where a Gm cell in the tuning loop was used to control an identical Gm cell in a filter. A key advantage of the proposed tuning circuit is that it saves IC area and power. Had a replica of the circuit in Fig. 3 been used for tuning, more than twice the power would have been dissipated as the high-bandwidth opamp in Fig. 3 consumes much more power than all the circuits in Fig. 5. With I_R = 1μA, the simulated variation in the filter time constant is less than 6% when there is a 250% variation in the capacitance, and the time-constant variation is 1% for a 40% capacitance variation. While the tuned time constant is slightly less than the design target, the time-constant accuracy is acceptable in a disk drive.

REFERENCES

[1] S.E. Stupp, M.A. Baldwinson, P. McEwen, T.M. Crawford, and C.T. Rogers, "Thermal Asperity Trends," *IEEE Tran. on Magnetics*, pp. 752-757, March 1999.

[2] K.G. Ashar, *Magnetic Disk Drive Technology, Heads, Media, Channel, Interface, and Integration*, IEEE Press, 1997.

[3] K.R. Laker and W.M.C. Sansen, *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, 1994.

[4] J. Silva-Martinez, M.S.J. Steyaert, and W. Sansen, "A 10.7-MHz 68-dB SNR CMOS Continuous–Time Filter with On-Chip Automatic Tuning", *IEEE J. Solid-State Circuits*, pp. 1843-1853, Dec. 1992.

FIGURES

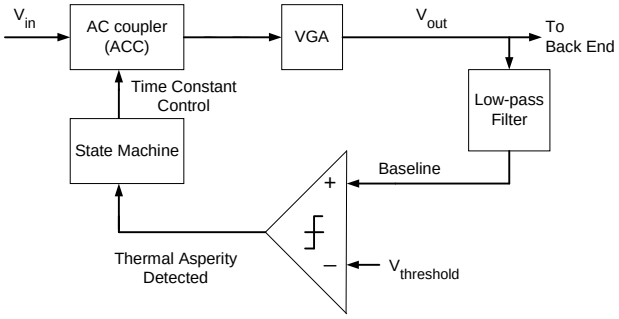

Fig. 1. Block Diagram of a Read Channel Front End.

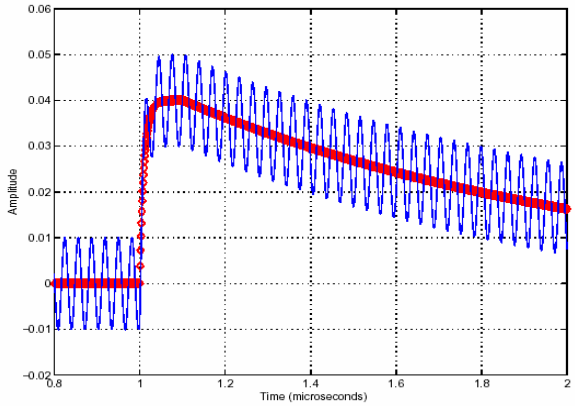

Fig. 2. A TA event: V_{in} (thin line) and its baseline (thick line) are plotted.

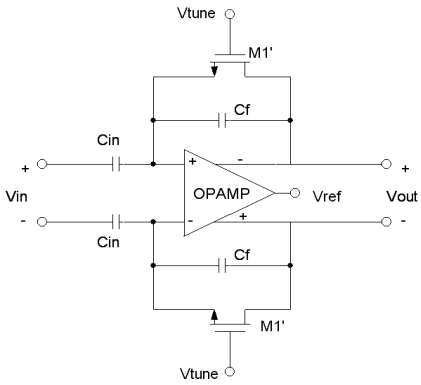

Fig. 3. AC coupler.

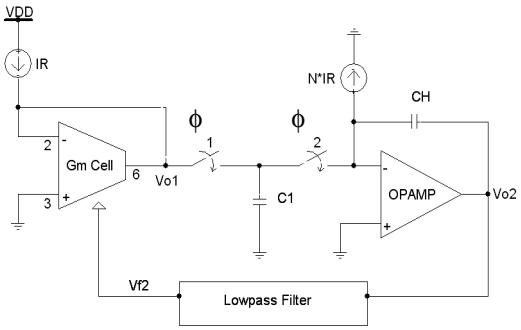

Fig. 4. Simplified Tuning Loop.

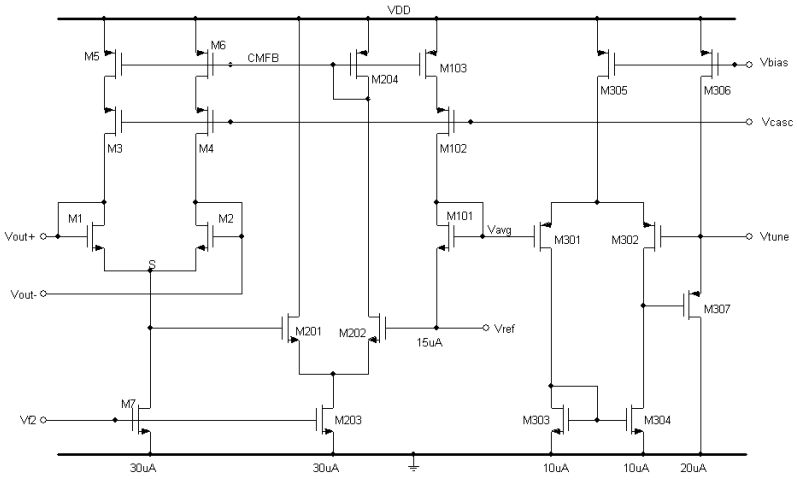

Fig. 6. Gm Cell. Bias currents are along the bottom.

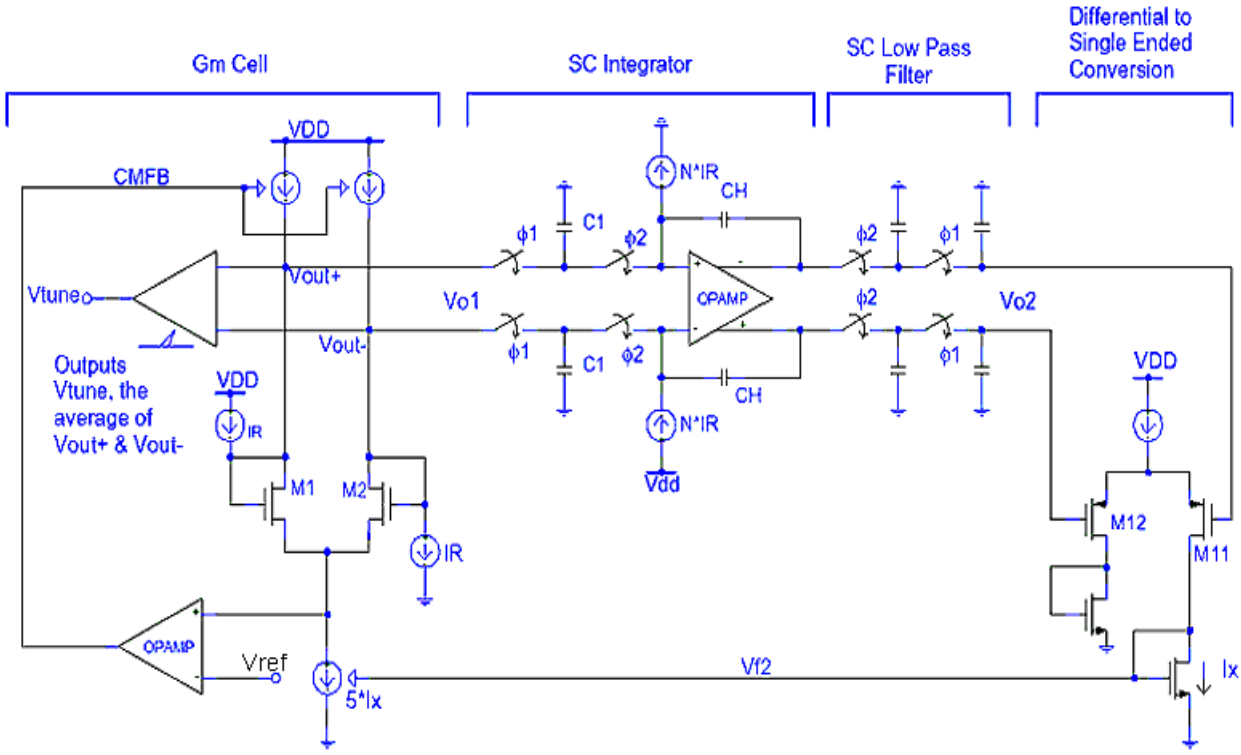

Fig. 5. Detailed Block Diagram of the Tuning Loop. V_{DD} = 3.3V.