An Adaptive Analog Noise-Predictive Decision-Feedback Equalizer*

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INTRODUCTION

This paper describes an adaptive analog noise-predictive decision-feedback equalizer (NPDFE). It consists of an analog finite-impulse response (FIR) forward equalizer (FE), a recursive analog equalizer for noise prediction, and a decision-feedback equalizer (DFE) that uses erasure. All three analog equalizers are adaptive. Area and power are saved by using analog rather than digital equalizers because a high-speed ADC is not required and the analog equalizers used in this prototype are smaller than their digital counterparts. To demonstrate the feasibility of our proposed NPDFE, the prototype was designed for use in a disk-drive read channel.

A block diagram of a conventional DFE-based read channel is shown in Fig 1(a). The DFE consist of the feedback equalizer, summer, and decision slicer. The FE is a linear equalizer that operates on only precursor ISI samples. Continuous-time or discrete-time all-zero forward equalizers have been used in magnetic recording channels [1],[2]. Such a forward equalizer typically provides high-frequency boost to the input signal and the noise. A consequence of this equalization is noise enhancement which results in a lower signal-to-noise ratio (SNR) at the decision slicer input. To eliminate the noise enhancement, noise prediction has been proposed for equalization channels. Noise prediction whitens the noise and increases the SNR at the decision slicer input. Our proposed structure for noise prediction, which is simpler than previously reported structures [3],[4], is shown in Fig. 1(b). Compared to the conventional DFE read channel in Fig. 1(a), our architecture adds a recursive equalizer for noise prediction.

ARCHITECTURE

Our discrete-time analog FE uses a circular buffer architecture [2] as shown in Fig. 2. In our block diagrams, the thick lines represent digital signals while the thin lines represent analog signals. The FE consists of 5 sample-and-hold amplifiers (SHA), a switch matrix, 4 multiplying digital-to-analog converters (MDAC), and 4 10-b digital integrators to implement LMS adaptation; only the integrator for coefficient b_1 is shown in Fig. 2 for clarity. This structure functions as an adaptive 4-tap FIR FE and is much smaller than a fully digital implementation. Based on simulation, only 4 taps are needed to remove precursor ISI for a read channel modeled by a Lorentzian function with $PW_{50} \leq 3T$. After each bit period T, an error $e[n]$ is computed as the difference between the decision slicer input and its output. This error is then quantized to 1 bit, simplifying the adaptive circuits. The quantized error $\hat{e}[n]$ along with the samples stored by the sample-and-hold amplifiers $x[n\text{-}k]$ are used to produce the digital FE coefficients b_k using a sign-sign LMS algorithm. Each MDAC multiplies an analog sample $x[n\text{-}k]$ by a 6-b digital coefficient b_k and produces an analog current output. The sum of the MDAC outputs is the equalized read signal after forward equalization and, thus, contains only postcursor ISI. The noise-predictive equalizer (NPE) uses an adaptive FIR filter connected as shown in Fig. 1(b). It has the same structure as the FE but requires only 3 taps. To allow the clocks to be shared by both the NPE and the FE, both use the same number of SHA's. Since the NPE only needs 3 taps, one SHA output is not used each bit period.

The DFE is shown in Fig. 3. The DFE consists of a 2.5-b flash ADC, a 6-tap feedback equalizer (5 taps for cancelling ISI and 1 for offset cancellation), and 6 10-b digital integrators for sign-error LMS adaptation. In Fig. 3, only the adaptive loop for coefficient c_1 is shown for clarity. Each multiplier in the DFE multiplies a past binary decision by a digital coefficient. This product is converted into an analog current using a current steering DAC. The first two taps in the DFE each use a 7-b DAC while the remaining 4 taps each use a 6-b DAC. Even though each tap requires a DAC, the design is area efficient because the 6-b DAC is about the size of 4 D flip-flops (DFF). The DAC's are small in comparison to the digital integrators, each of which uses 10 DFF's plus a large amount of combinational logic. The analog signal output by the feedback equalizer cancels the postcursor ISI that remains after forward and noise-predictive equalization. Since the DAC's in the DFE and the MDAC's in the FE and NPE produce analog current outputs, we can sum all of the equalizer outputs by simply tying these outputs together.

The output of the decision slicer is the input of the feedback equalizer in a conventional DFE. However, as shown in Fig. 3, our DFE uses erasure, and therefore the input to the feedback equalizer is either the slicer decision $\hat{a}$=±1 or 0 [5]. A '0' is fed into the feedback equalizer whenever the input to the decision slicer falls within a small region $\pm\Delta \approx \pm 0.1$ close to the zero threshold. Thus, unreliable decisions are not used by the feedback equalizer. Using erasures reduces the probability of having error bursts of length 2 or more, which is important when taking error-correcting codes into account [5]. The flash ADC only requires 2 additional preamps and comparators with minimal decode logic to implement erasure.

Due to the nonlinear operation of the decision slicer, noise at the input of the decision slicer is not affected by the feedback equalizer in the DFE. Thus, the z-domain transfer function from white noise added at the FE input to the decision slicer input is $B(z)/[1 + A(z)]$, where $A(z)$ and $B(z)$ are the z-domain transfer functions of the FIR filters in the NPE and FE, respectively. To produce white noise at the slicer input, this transfer function must be all-pass. A front-end automatic gain control (AGC) typically precedes the FE and allows us to set FE coefficient b_4 = 1. With this simplification, the FE and NPE coefficients can be shared using the relationships $b_3 = a_1$, $b_2 = a_2$, and $b_1 = a_3$ which gives an all-pass transfer function for the noise. Stability of the feedback loop that contains the NPE is a concern. However, since the FE only cancels precursor ISI, it will adapt so that its response is maximum

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phase, i.e., all the zeros of the FE are outside the unit circle. Thus, all the poles in the all-pass transfer function $B(z)/[1+A(z)]$ will be inside the unit circle; this guarantees the stability of the feedback loop containing the NPE.

The NPE is disabled during the initial adaptation period and the FE and DFE are adapted to minimize the mean-squared error. Then, the NPE is enabled and its coefficients are simply determined from the FE coefficients as specified earlier. Sharing coefficients in the FE and the NPE eliminates the need for 3 integrators in the NPE, saving area since the integrators consume a large percentage of the die area. Once the initial adaptation period is completed and the NPE is enabled, the FE coefficients are fixed and the DFE is re-adapted. This is necessary since the NPE affects the postcursor ISI when it is enabled.

MEASURED DATA

The test signal was generated using random binary data and a Lorentzian channel model with $PW_{50}=2.5T$. This signal was loaded into an arbitrary waveform generator, and band-limited white Gaussian noise was added to form the test input signal. Fig. 4 shows plots of the measured bit-error rate (BER) versus channel SNR at 100 Mbps for the NPDFE with the NPE enabled and disabled. It also plots the measured BER performance of another conventional DFE-based read channel [1]. Without noise prediction, our read channel gives similar performance to the other conventional read channel. However, there is about a 2 dB performance improvement when the NPE is enabled (solid line). This is a large performance increase. Yet, the NPE only uses 15% of the die area. A die photo is shown in Fig. 5, and performance is summarized in Table 1.

REFERENCES

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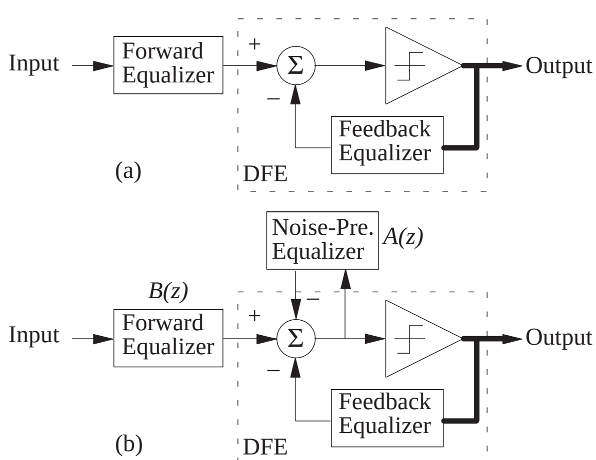

Fig. 1 (a) Conventional DFE-based read channel and (b) NPDFE.

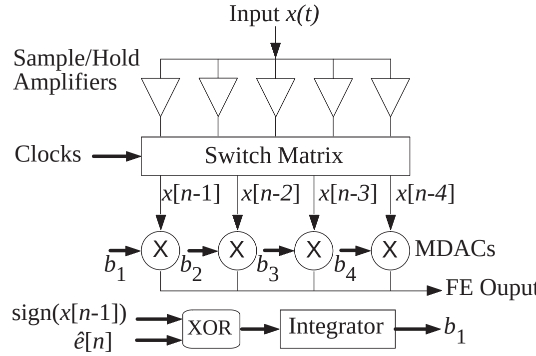

Fig. 2. Forward equalizer architecture.

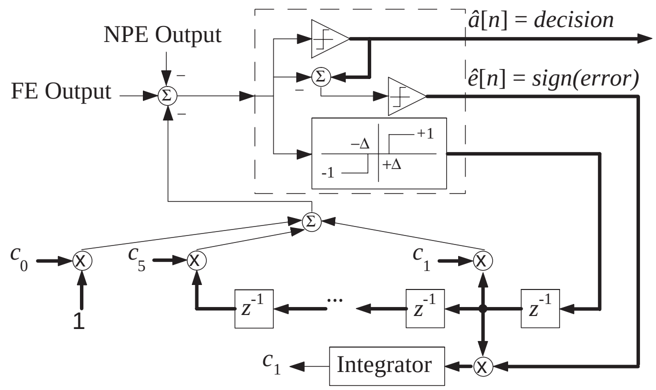

Fig. 3. DFE architecture with erasure.

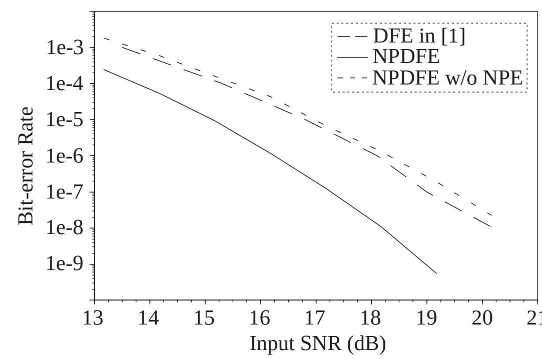

Fig. 4. Measured BER performance.

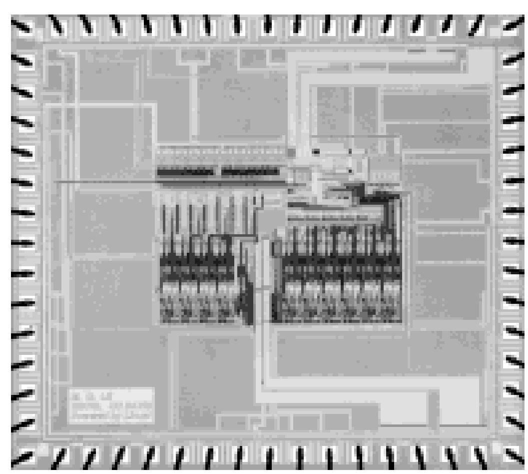

Fig. 5. Die photograph.

Process	0.5-µm CMOS
Active Area	1.3 mm^2
Data Rate	100 Mbps
Power Dissipation	130 mW

Table 1. Measured performance with 3.3V supply and 25°C.