

An Adaptive Analog Noise-Predictive Decision-Feedback Equalizer *

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ABSTRACT

In this paper, an adaptive noise-predictive decision-feedback equalizer (NPDFE) is presented. The NPDFE architecture and its implementation are described. The NPDFE consists of an analog finite-impulse-response (FIR) forward equalizer, a recursive analog equalizer for noise prediction, and a decision-feedback equalizer (DFE). The recursive equalizer reduces noise enhancement and improves the signal-to-noise ratio (SNR) at the decision slicer input. The prototype targets a magnetic recording channel modelled by a Lorentzian impulse response. Measured results show that compared to a conventional DFE with FIR forward equalizer, the NPDFE achieves a SNR improvement of about 2 dB with $PW_{50}=2.5T$. The NPDFE consumes 130 mW at a data rate of 100 Mbps and occupies 1.3 mm² of die area in a 0.5- μ m CMOS process.

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I. Introduction

In modern disk drives and many digital communication systems, intersymbol interference (ISI) is severe. Systems using partial-response maximum-likelihood (PRML) detection have been developed and used extensively to combat this problem [1]. Detection methods other than PRML, such as decision-feedback equalization and fixed-delay tree search with decision-feedback, have also been proposed [2],[3].

Decision-feedback equalization was first introduced by Austin [4]. Such equalizers are usually used in conjunction with a linear forward equalizer to remove ISI. One drawback of the linear equalization used in both PRML and DFE detectors is that it typically introduces high-frequency boost, which causes noise enhancement. To alleviate this problem, architectures that incorporate noise prediction have been investigated [5],[6],[7]. This paper describes an adaptive analog noise-predictive decision-feedback equalizer (NPDFE). Area and power are saved by using analog rather than digital equalizers because a high-speed ADC is not required and the analog equalizers in this prototype are smaller than their digital counterparts. To demonstrate the feasibility of our proposed NPDFE, the prototype was designed for use in a disk-drive read channel.

This paper is organized as follows. Section II provides background. Section III introduces the noise-predictive DFE. The IC implementation is covered in Sections IV, V and VI. Measured results are presented in Section VII, which is followed by a conclusion.

II. Background

Figure 1 shows a block diagram of a conventional decision-feedback equalizer-based read channel that can remove ISI. The read signal is first passed through a low-noise preamp and automatic gain control (AGC) circuit that adjusts the signal amplitude to a desired level. Then, the output of the AGC is sent through a low-pass filter (LPF) to remove out-of-band noise. Finally, the output of the LPF is passed through the forward equalizer (FE) and decision-

feedback equalizer (DFE). The FE is a linear filter that removes precursor ISI. The DFE consists of the feedback equalizer, summer, and slicer as shown in the dashed box of Figure 1. The slicer makes binary decisions that are estimates of the recorded data on the disk. The feedback equalizer in the DFE is a FIR filter and, thus, its output is a linear combination of past decisions that cancel the postcursor ISI remaining after forward equalization. Usually, these equalizers are adaptive to compensate for channel variations.

Typically, a FIR forward equalizer is used to remove the precursor ISI. The FIR forward equalizer is often constrained to generate its output from samples of the input waveform at and before the cursor [8]. Such an equalizer has a high-pass transfer function that boosts the input signal at high frequency [9]. This equalizer also boosts the input noise at high frequency causing noise enhancement, which degrades the SNR at the slicer input. The SNR is defined as the ratio of the signal power to the noise power (which consists of channel noise filtered by the FE and uncanceled ISI) measured at the slicer input. For a read channel with $PW_{50}=2.5T$ (where PW_{50} is the time between the half amplitude points on the Lorentzian waveform and T is the bit period), the simulated SNR loss due to noise enhancement is about 1.9 dB, and this SNR loss increases as the recording density increases.

Performance improvement is possible if the noise enhancement of the forward equalizer can be reduced or eliminated. Recently, there has been interest in using an all-pass forward equalizer instead of a FIR filter to remove precursor ISI [6],[10],[11],[12]. A low-order pole-zero all-pass forward equalizer (APFE) can effectively remove precursor ISI without enhancing the channel noise. To see how the APFE removes precursor ISI, assume that the sampled Lorentzian step response can be approximated in the z -domain by

$$L(z) = \prod_{i=1}^M \frac{1}{(1-\lambda_i z^{-1})(1-\lambda_i z)} \quad |\lambda_i| < 1, \quad (1)$$

which has poles at λ_i and $1/\lambda_i$ [10]. The poles λ_i are inside the unit circle and model the postcursor ISI; the poles $1/\lambda_i$ outside the unit circle model the precursor ISI. The transfer function of an APFE that has zeros that cancel the precursor ISI in (1) can be expressed in the z -domain by

$$APFE(z) = K \prod_{i=1}^M \frac{(1-\lambda_i z)}{(1-\lambda_i z^{-1})}, \quad (2)$$

where K is a constant scale factor. The magnitude response of the APFE is given by

$$\left| APFE(e^{j\omega T}) \right| = K. \quad (3)$$

Therefore, the noise at the APFE output is white if the input noise is white. The APFE has M zeros outside the unit circle that cancel precursor ISI due to the poles at $1/\lambda_i$ in (1). However, its transfer function also has M poles inside the unit circle.

There are two main problems with an APFE that stem from these poles. First, the poles and zeros must adapt. However, adaptation of the poles in an APFE is problematic since one or more poles could move outside the unit circle and cause instability during the adaptation process. In practice, this problem has been dealt with by presetting the filter coefficients to an *a priori* known set that equalize the nominal channel response [12]. The coefficients can then be adapted to compensate for the slight variation in the channel. Another problem with an APFE is that the poles of the APFE cause the postcursor ISI at the output of the APFE to be longer. If the sampled step response in (1) is fed into the APFE in (2), the APFE output can be expressed in the z -domain by

$$APFE \text{ Output} = K \prod_{i=1}^M \frac{1}{(1-\lambda_i z^{-1})^2}, \quad (4)$$

The order of the denominator here is $2M$. When an all-zero FIR FE is used to cancel the precursor ISI in (1), the order of the denominator of the z -domain representation of the FE output is M . Hence, an APFE removes precursor ISI at the expense of making the residual postcursor ISI longer than the postcursor ISI when an all-zero FE is used. As a result, a DFE with more taps would be required to remove the trailing ISI, which increases the design complexity and implementation costs. In the next section, an architecture that does not suffer from these problems is presented.

III. Noise-Predictive DFE

A block diagram of the proposed NPDFE is shown in Figure 2. This architecture uses a noise-predictive equalizer (NPE) $A(z)$ along with a forward equalizer $B(z)$ and a feedback equalizer $C(z)$. $A(z)$, $B(z)$, and $C(z)$ are FIR transfer functions. The noise $N[n]$ added at the forward equalizer input models channel noise and is assumed to be white. To minimize the noise power at the slicer input, the noise at the slicer input should also be white [5]. With the proper choice of coefficients in $A(z)$, $B(z)$, and $C(z)$, the noise-predictive DFE can produce white noise at the slicer input as will be shown below. Therefore, there is no noise enhancement resulting from the equalization in this architecture. An important assumption is that the noise added at the forward equalizer input is white. If that is not the case, the performance improvement will vary depending on the spectrum of this noise.

Due to the nonlinear operation of the slicer in Figure 2, the decision $\hat{a}[n]$ is noise free assuming no decision error. Thus, the noise at the slicer input is not affected by the feedback equalizer $C(z)$. Using this key observation, the z -domain transfer function from noise $N[n]$ added at the forward equalizer input to the slicer input $y[n]$ can be expressed as

$$H_n(z) = \frac{Y(z)}{N(z)} = \frac{B(z)}{1+A(z)} = \frac{b_0 + b_1z^{-1} + \dots + b_qz^{-q}}{1 + a_1z^{-1} + \dots + a_pz^{-p}}, \quad (5)$$

where b_0 to b_q are the forward equalizer coefficients and a_1 to a_p are the noise-predictive equalizer coefficients. To produce white noise at the slicer input, this transfer function must be all-pass. Therefore, we need $p=q$ and the i -th pole and the i -th zero must have the following relation

$$p_i = \frac{1}{z_i^*}, \quad (6)$$

where the $*$ denotes the complex conjugate. From this relation, the coefficients a_k in the noise-predictive equalizer can be computed from the forward equalizer coefficients b_k as

$$a_k = \frac{b_{q-k}}{b_q}. \quad (7)$$

In the read channel, the front-end automatic gain control can scale the input signal $x[n]$ so we can set $b_q=1$ without loss of generality. With this choice, the calculation of a_k from the b coefficients does not require the division in (7) (i.e. $a_k = b_{q-k}$), which simplifies the implementation.

If the read signal is well equalized, the slicer input $y[n]$ is equal to the decision $\hat{a}[n]$ plus noise that has been filtered by $B(z)$ and $A(z)$. If we linearize the slicer (treating it as a linear amplifier with unity gain), the transfer function from the sampled input signal $x[n]$ to the slicer input $y[n]$ is given by

$$H_s(z) = \frac{Y(z)}{X(z)} = \frac{B(z)}{1 + [A(z) + C(z)]}. \quad (8)$$

This transfer function depends on both the noise-predictive equalizer $A(z)$ and the feedback equalizer $C(z)$. The forward equalizer $B(z)$ cancels precursor ISI while the feedback equalizer and noise-predictive equalizer operate on and cancel the postcursor ISI.

Figure 3(a) shows a conventional FIR forward equalizer and DFE combination that can be used instead of a NPDFE. This structure will be referred to as the FIR+DFE. Figure 3(b) shows the proposed NPDFE. Comparing the two figures, the key difference between the two structures is the presence of the noise-predictive equalizer $A(z)$. If we linearize the slicers,

compute the transfer functions from $x[n]$ to $\hat{a}[n]$ in Figures 3a and 3b and then equate these transfer functions, the feedback equalizers in the two structures can be related as follows

$$D(z) = A(z) + C(z) . \quad (9)$$

If the FIR+DFE has optimum coefficients b_k and d_k (i.e. coefficients that minimize the mean-squared value of the error $e[n]$ [8], where $e[n]$ is defined in Section V), then the coefficients c_k in the NPDFE can be computed using (9) as

$$c_k = d_k - a_k , \quad (10)$$

The coefficients b_k in the forward equalizers are the same in both structures. If coefficient b_q is fixed and set to 1, the noise-predictive equalizer coefficients can be computed using (7) as

$$a_k = b_{q-k} , \quad (11)$$

so the NPE coefficients are simply the FE coefficients reordered.

Because $A(z)$ is used in a feedback loop, stability of the NPE is a concern. Since the FIR forward equalizer $B(z)$ only operates on the precursor ISI samples, it will adapt so that its response is maximum phase. This adaptation is described in Section V below. As a result, all of the zeros of $B(z)$ will be outside the unit circle. Since the coefficients of the transfer function $H_n(z)$ in (5) are chosen so that $H_n(z)$ is all-pass, the magnitudes of the poles and the zeros are the reciprocals of each other as noted in (6). Thus, the poles associated with the NPE in (5) will be inside the unit circle; this guarantees the stability of the NPE.

IV. Implementation

A block diagram of the analog NPDFE is shown in Figure 4. The forward and noise-predictive equalizers are both discrete-time analog equalizers. All three equalizers produce analog current outputs, which are summed by connecting their outputs together. The result is converted into a voltage using a resistor and then sliced to produce the binary decision $\hat{a}[n]$. The feedback equalizer in a conventional DFE uses the binary decision $\hat{a}[n]$ as its input. Here, we use erasures. Thus, the input to the feedback equalizer is driven by a separate quantizer that has

three possible output values $f[n] = \{+1, 0, -1\}$. The quantizer output is zero whenever the magnitude of its input y is small and close to zero (i.e. $|y| < \Delta$). Using erasures in the DFE gives a modest decrease in the bit-error rate (BER) and reduces the number of long error bursts [13]. This reduction in the number of long error bursts can be important when error-correcting codes are used. The performance of such codes is often dependent on the assumption of isolated errors and can be significantly degraded if the probability of long error bursts is high.

Figure 5 shows a detailed block diagram of the analog NPDFE prototype. The thin lines represent analog signals while the thick lines represent digital signals. The adaptive loops are not shown for clarity. Based on simulation, only 4 taps are needed in the forward equalizer to remove precursor ISI for a read channel modeled by a Lorentzian function with $PW_{50} \leq 3T$. The analog discrete-time forward equalizer and noise-predictive equalizer both use a circular buffer architecture [14]. In each of these equalizers at any given time, one of the sample-and-hold amplifiers (SHAs) is sampling its input while the other SHA outputs are held constant and used to generate the equalizer output. The SHAs are selected in a circular fashion by a switch matrix controlled by the bit clock divided by five.

To allow sharing of the clocks between the forward equalizer and the noise-predictive equalizer, the noise-predictive equalizer also uses five SHAs. Since the noise-predictive equalizer only uses three feedback taps, one SHA is not used to sample data or equalize the read signal each clock cycle. The samples stored in the SHAs are multiplied by 6-b digital coefficients using multiplying digital-to-analog converters (MDACs). Each MDAC produces an analog current at its output, which is summed with the other MDAC outputs to form the forward equalizer output.

Each of the first five taps in the feedback equalizer multiplies a past slicer output with the appropriate coefficient c_k to produce an analog current output. A sixth tap with coefficient c_0 is used to cancel the DC offset at the slicer input. The six most significant bits of each coefficient

c_k in the feedback equalizer are converted into an analog current using a binary weighted DAC. The first two feedback taps (c_1 and c_2) each use a 7-b DAC while the remaining 4 taps each use a 6-b DAC. The extra bit is required since the first two coefficients have a larger range of values than the other coefficients. Even though each tap requires a DAC, the design is area efficient because the 6-b DAC is about the size of 4 D flip-flops (DFFs). The DACs are small in comparison to the digital integrators used to adapt the coefficients; each of which uses 10 DFFs plus a large amount of combinational logic.

Since the MDACs in the FE and NPE and each tap in the feedback equalizer produce differential analog current outputs, the equalizer outputs are summed by simply tying these lines together. The resulting current is amplified by a factor of two and then converted to a voltage by a transresistance (or I2V) stage consisting of polysilicon resistors followed by a buffer. The output of the buffer is then sliced by a comparator to produce the binary decision $\hat{a}[n]$ at the output.

V. Adaptation

The forward equalizer is adapted using a sign-sign least-mean squared (LMS) algorithm, and the feedback equalizer is adapted using a sign-error LMS algorithm. Each integrator used in the adaptive loops is formed by cascading a 4-b pre-counter and a 6-b up/down counter. The operation of the 4-b pre-counter and 6-b digital up/down counter (which together act as a discrete-time integrator) is similar to the mixed-signal integrator described in [15]. The use of the pre-counter reduces the coefficient variation (or tap noise). The output of the 6-b up/down counter is the digital coefficient value that is used by the MDAC or DAC in each of the equalizer taps. After each bit period T , an error $e[n]$ is computed as the difference between the decision slicer input and its output. This error is then quantized to 1 bit, simplifying the adaptive circuits. The quantized error $\hat{e}[n]$ and the quantized past input sample $\text{sign}(x[n-k])$ are used to adapt the FE coefficient b_k . This adaptation can be expressed as

$$b_k[n] = b_k[n-1] - \mu \hat{e}[n] \text{sign}(x[n-k]) \quad \text{for } k = 0, 1, 2 . \quad (12)$$

Coefficient b_3 is fixed and set to one. The small scale factor $\mu > 0$ governs the convergence rate and steady-state variance of the coefficients. In the feedback equalizer, the past decision $\hat{a}[n-k]$ is multiplied by the 1-b error $\hat{e}[n]$ and then integrated to form the coefficient c_k :

$$c_k[n] = c_k[n-1] + \mu \hat{e}[n] \hat{a}[n-k] \quad \text{for } k = 1, 2, \dots, 5 . \quad (13)$$

The error $\hat{e}[n]$ is integrated to form the coefficient c_0 in the DC offset tap as given by

$$c_0[n] = c_0[n-1] + \mu \hat{e}[n] . \quad (14)$$

The equalizer coefficients are adapted using the following procedure. The NPE is disabled (i.e. all $a_k = 0$) during the initial adaptation period, and the FE and DFE in Figure 3a are adapted using the LMS adaptation. After this adaptation is complete, the NPE is enabled and its coefficients are simply determined from the FE coefficients using (11). This simple relationship between the coefficients in the FE and the NPE eliminates the need for three additional integrators to adapt the three NPE coefficients, saving area since the integrators consume a large percentage of the die area [15]. Once the initial adaptation period is completed and the NPE is enabled, the FE coefficients are fixed and the feedback equalizer is readapted. This is necessary because the NPE affects the postcursor ISI at its output when it is enabled. Alternatively, the new DFE coefficients could be computed using (10). However, we readapt to save hardware.

A block diagram of the adaptive forward equalizer is shown in Figure 6. A comparator produces the sign of the input signal x each bit period. The output of this comparator feeds a shift register and the adaptive circuitry for the forward equalizer as shown in Figure 6. To adapt each FE coefficient, the sign of the input signal (delayed) is multiplied with the 1-b slicer error using a simple XOR gate since both inputs are 1-b signals. The output of each multiplier is then integrated using the 4-b pre-counter and 6-b up/down counter combination described previously to give each FE coefficient. Advantages of using an all digital integrator include the fact that an

initial set of coefficients can easily be loaded into the equalizer and that the coefficients can be frozen during steady-state operation. By freezing the coefficients in steady-state operation, noise at the slicer input produced by the variation of the coefficients is eliminated. The adaptive loops for the feedback equalizer coefficients are implemented in a similar manner using the adaptive algorithm in (13).

VI. Circuit Blocks

Figure 7 shows the sample-and-hold amplifier (SHA) used in the forward equalizer and noise-predictive equalizer. The cascode transistors connected to V_{GG} operate in saturation to boost the output impedance. V_{BB} sets the bias current of about 500 μA in each branch. The clock phases ϕ_1 and ϕ_2 are non-overlapping. Phase ϕ_1 has duration T , while ϕ_2 lasts the remainder of the $5T$ clock period, where $1/T$ is the bit rate. For the prototype fabricated, the individual clock signals required for the 5 SHAs were generated using an off-chip pulse generator. During ϕ_1 , the outputs are shorted to the gates of the input transistors M1 and M2 by closing the switches controlled by ϕ_1 and opening switches controlled by ϕ_2 . The SHA input signal is tracked during this phase and is stored across the 100 fF capacitors C_1 and C_2 . The 100 fF capacitors are formed using a "sandwich" of poly and 3 metal layers. The outer capacitor plate is formed using the poly and metal 2 layers and the inner plate is formed using metal 1 and metal 3. A drawback to using the poly layer in the capacitor structure is that the parasitic capacitance from poly to the substrate is larger than the parasitic from metal layer, and this parasitic capacitance adds to the loading at the input (on ϕ_1) and output (on ϕ_2) of the SHA. During ϕ_2 , the outer capacitor plates are connected to the outputs by closing the switches labeled ϕ_2 and opening the switches labeled ϕ_1 . Then the SHA is in the hold mode. The SHA gain from V_{in} (on ϕ_1) to V_{out} (on ϕ_2) is about 1. The simulated unity-gain frequency of the open-loop amplifier in Figure 7 is about 800 MHz with a phase margin of 70 degrees when driving a 250 fF load capacitance. The DC gain of this

amplifier is about 300 and draws a total current of about 1 mA. Based on simulation, the SHA requires less than 2 ns to settle to within 1% of its full-scale differential output voltage of 500 mV.

Each MDAC consists of binary weighted Gm cells that are connected in parallel. Figure 8 shows one of the Gm cells used in the MDAC. The polarity of the current output of each Gm cell is controlled by an input bit D_i of a 6-b digital coefficient a_k or b_k . M1 and M2 produce a differential current that is proportional to the input voltage V_{in} . The PMOS transistors controlled by D_i steer the current to the output and operate in saturation to boost the output impedance when they are enabled. An equation that describes the operation of the MDAC is

$$Gm_{out} = \frac{I_{out}}{V_{in}} = Gm_0 + Gm_1(D_1) + Gm_2(D_2) + \dots + Gm_6(D_6), \quad (15)$$

where the digital bits $D_i = \pm 1$, D_1 is the MSB, and D_6 is the LSB. Here, Gm_0 sets the nominal transconductance of each MDAC. It is set to a normalized value of 1 for tap b_3 , -0.5 for taps b_2 and a_2 , and zero for the other forward equalizer and noise-predictive equalizer taps (based on simulation results).

Figure 9 shows the structure of one feedback equalizer tap. The 6-b DAC used in each tap is constructed using two cascaded 3-b binary-weighted sub-DACs to reduce the number of unit elements in the implementation. The current output of each 6-b DAC is then multiplied by +1, -1, or 0 (which is the output of the quantizer in the feedback loop) using the multiplier that consists of the 4 NMOS transistors shown in Figure 9. When an erasure occurs (i.e., the erase signal is high) and the current must be multiplied by 0, all NMOS transistors are turned on and this results in zero differential output current. When an erasure does not occur (i.e., the erase signal is low), the DAC output current is simply multiplied by the past decision, which is equal to ± 1 , by enabling the outer or inner pairs of NMOS transistors, respectively. These transistors operate in saturation to increase the output impedance when they are enabled.

A flash ADC is used to generate the binary decision, 1-b error signal, and the erasure signal. A block diagram of the ADC is shown in Figure 10. The ADC has a latency of 1 bit period, which accounts for the $[n-1]$ time index in the ADC outputs. For clarity, the block diagram only shows the single-ended version of the ADC. However, a fully differential architecture is used in the prototype. The ADC consists of 5 preamplifiers and comparators, decode logic and latches at each ADC output. Each comparator is preceded by a preamplifier to reduce the effect of the offset at the comparator input. VRH , VRM , VRL , VEP , VEN are off-chip reference voltages. Based on system simulations, the error in the thresholds (due to offsets in the comparators and inaccuracies in the reference voltages) should be less than about 15mV to keep the SNR loss small (<0.25 dB). VRM is the decision slicer threshold voltage which is nominally set to 1.0 V. $VRH=1.25$ V and $VRL=0.75$ V are reference voltages used to generate the 1-b error signal that is used in the adaptive loops. These voltages define the ideal voltages at the slicer input for $\hat{d}[n]=\pm 1$. The ideal differential signal is ± 500 mV at the slicer input.

The IC was fabricated in a 0.5 μ m single-poly triple-metal CMOS process. The core area is 1.0 mm x 1.3 mm. The entire chip including pads is 2.4mm x 2.7 mm. A photograph of the die core is shown in Figure 11. The circular buffers for the FE and NPE are located along the left half of the upper edge. The switch matrix and 7 MDACs are located beneath these buffers. The feedback equalizer uses 6 DACs. The digital logic occupies the lower half of the active area. It consists of 10 4-b pre-counters, 10 6-b up/down counters, and control logic.

VII. Measured Results

Shown in Figure 12 is the measured bit-error rate (BER) performance of the analog noise-predictive DFE during steady-state operation at a data rate of 100 Mbps. The prototype was designed to run at a higher data rate, but an alignment problem between the multiple clock phases prevented the prototype from operating properly at higher clock speeds. The thick solid line plots the BER performance of the noise-predictive DFE. The thin solid line plots the BER of

the NPDFE with the noise-predictive equalizer disabled, and the dashed line plots the measured BER of a conventional mixed-signal FE and DFE by Brown, et al. [16] that does not use noise prediction. Without noise prediction, our circuit gives similar performance to the conventional FE and DFE. However, there is about a 2 dB performance improvement when the noise-predictive equalizer is enabled. This is a significant performance increase. Yet, the noise-predictive equalizer only uses 15% of the die area on the prototype. Therefore, a significant performance improvement is achieved for a small increase in die area.

The measured plots in Figure 13 show the effect of the erasure threshold on the BER for three SNR values. The erasure threshold (Δ in Figure 5) is plotted as a fraction of the ideal peak slicer input voltage, which is 500 mV differential. When the erasure threshold is zero, the feedback equalizer behaves as a conventional DFE that does not use erasures. As the erasure threshold increases, the BER decreases initially but then starts to increase as the threshold gets larger than 0.2. This increase occurs because when the erasure threshold is too large, the number of erasure events is high and thus the feedback equalizer becomes less effective. From this plot, optimum performance is obtained by using a normalized erasure threshold of 0.15 when the input SNR is 18 dB.

Figure 14 shows measured histograms of the number of error events versus the length in bits of the error bursts when operating the NPDFE at an input SNR of 12 dB. This figure shows the error burst lengths of the NPDFE when erasure is turned on and off for 2 million data samples. As seen in Figure 14, using erasures effectively reduces the probability of long error bursts by a factor of two or better.

The measured performance of the prototype is summarized in Table 1.

VIII. Conclusions

A mixed-signal DFE-based read channel that uses a recursive noise-predictive equalizer has been presented. The described NPDFE is simpler than but achieves performance that is

similar to an all-pass forward equalizer plus DFE. The NPDFE read channel outperforms the typical FIR forward equalizer and DFE combination. The measured SNR improvement is about 2 dB, and this improvement is achieved with a small increase in die area. A method for adapting the coefficients in this NPDFE has been described. Reliable convergence and stability are assured by this adaptation scheme. A prototype was fabricated in a 0.5- μm CMOS process to demonstrate the feasibility of the NPDFE. The NPDFE may be useful in read channels and digital-communication receivers that must cancel both precursor and postcursor ISI.

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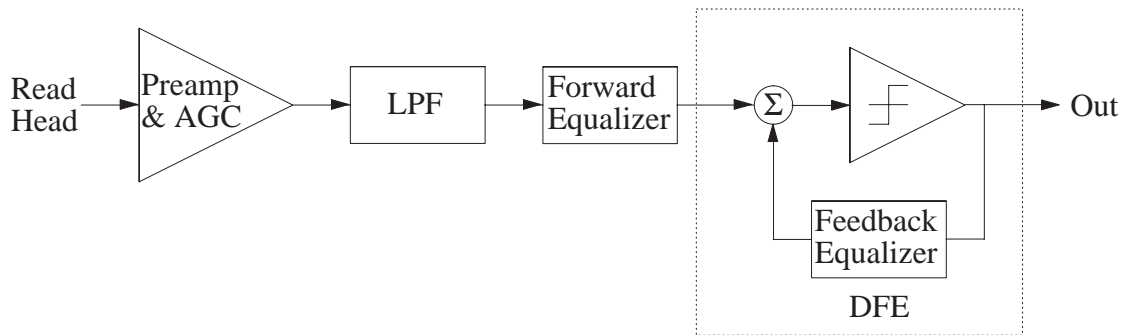


Figure 1. Conventional DFE-based read channel.

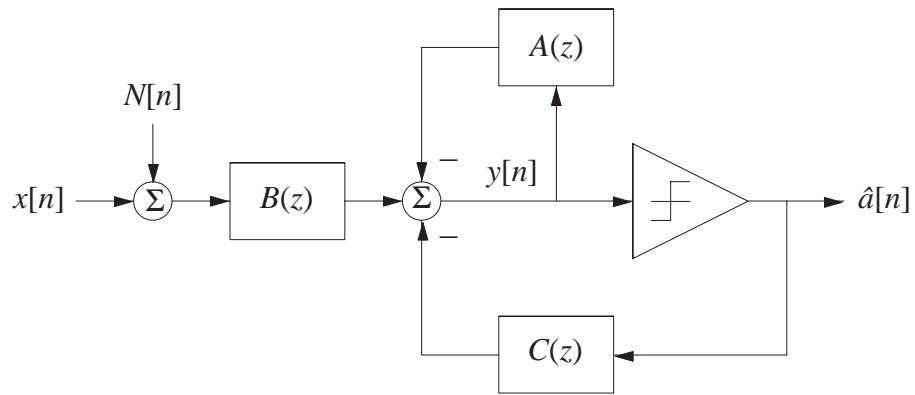


Figure 2. Proposed noise-predictive DFE.

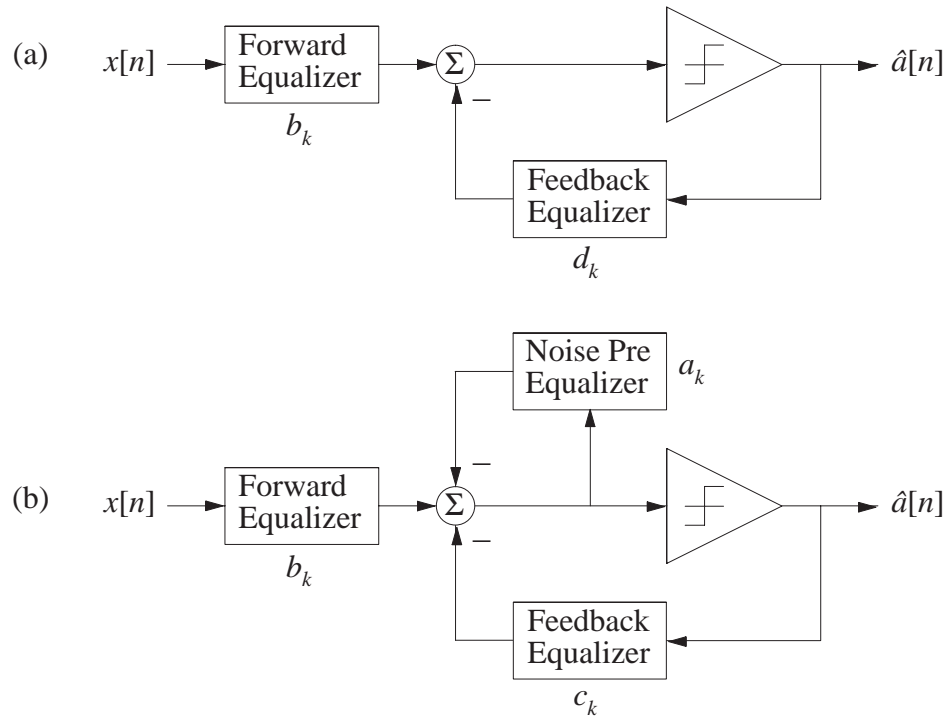


Figure 3. (a) FIR+DFE and (b) NPDFE.

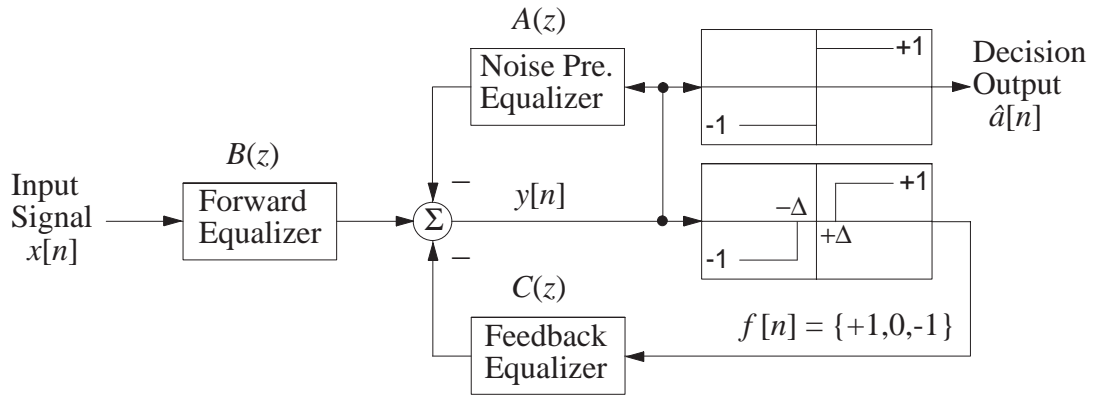


Figure 4. Block diagram of the NPDFE using erasure.

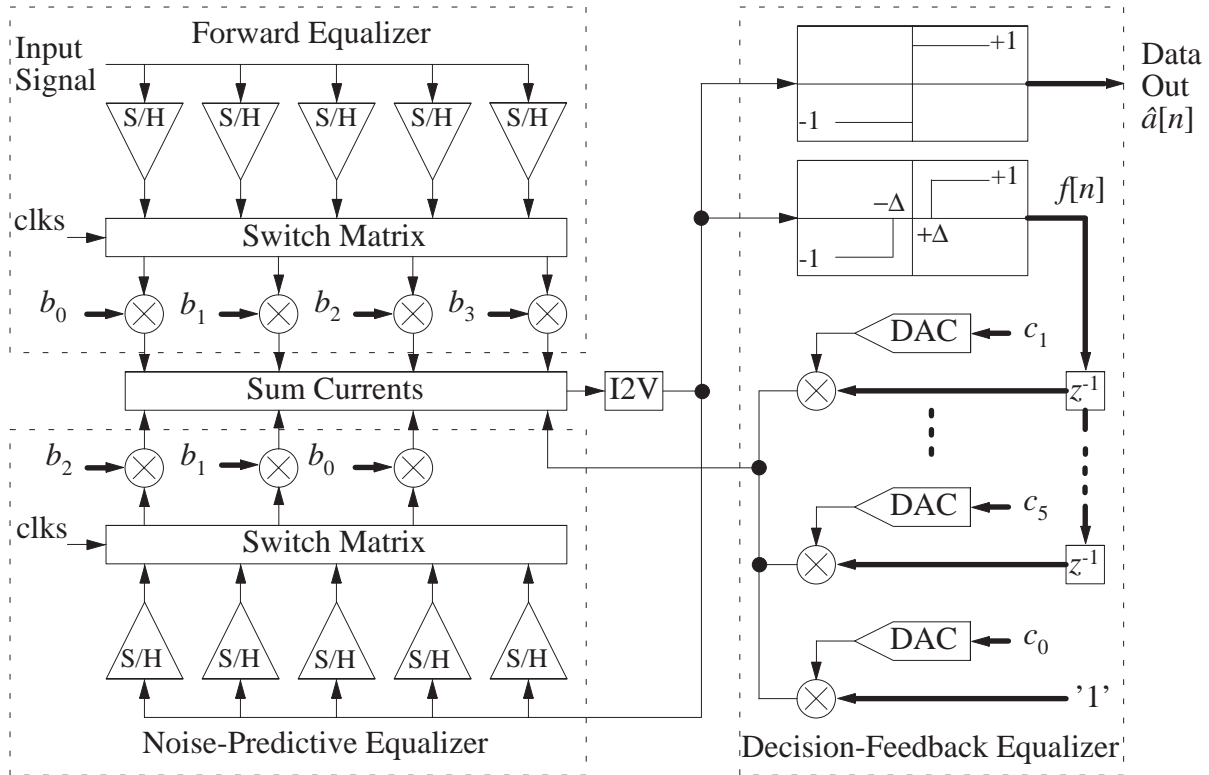


Figure 5. Detailed block diagram of the NPDFE, adaptive loops are not shown.

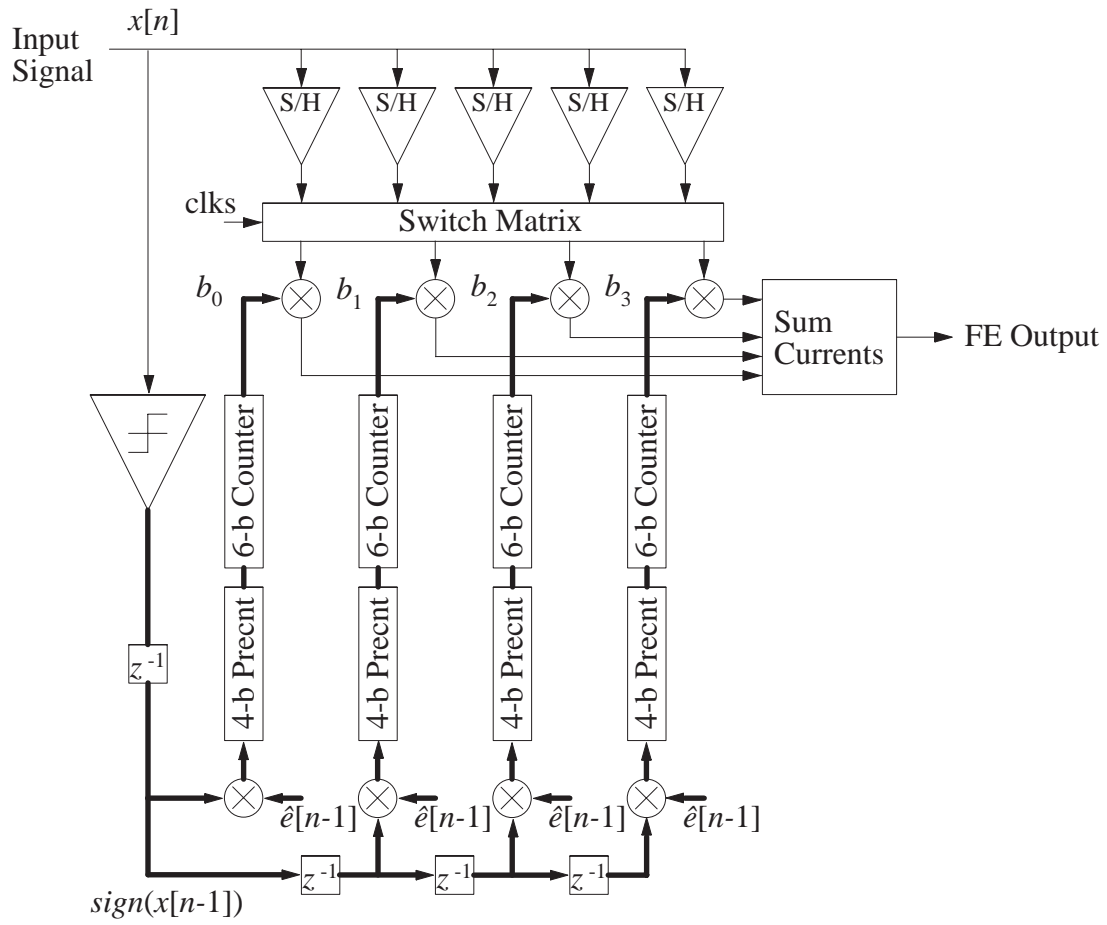


Figure 6. Forward equalizer showing the adaptive loop.

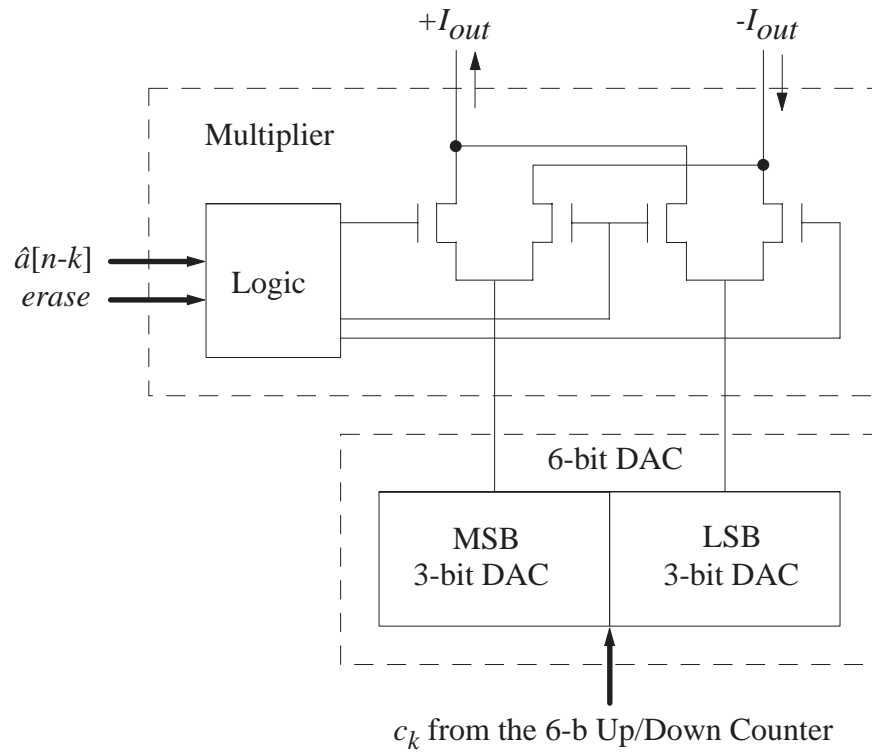


Figure 9. A DFE tap.

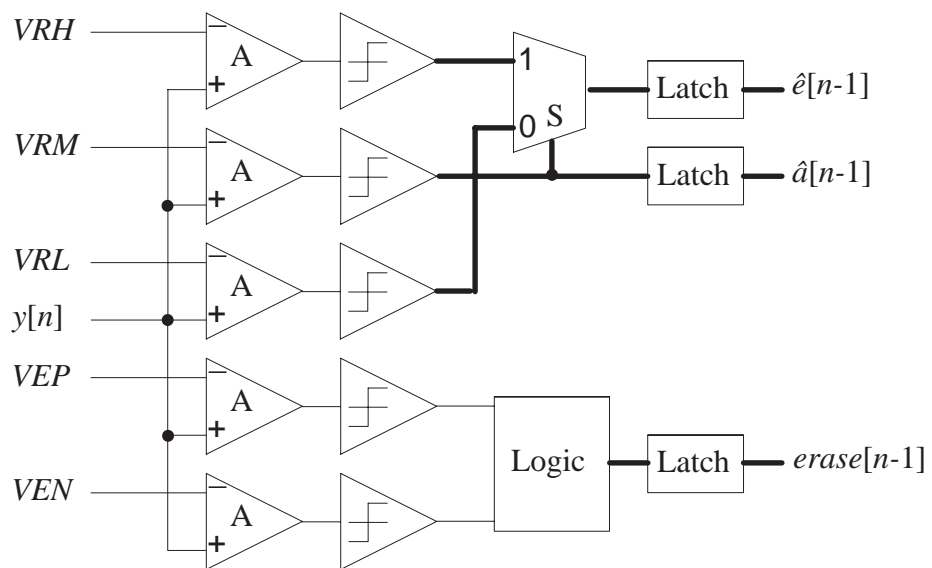


Figure 10. Flash ADC structure

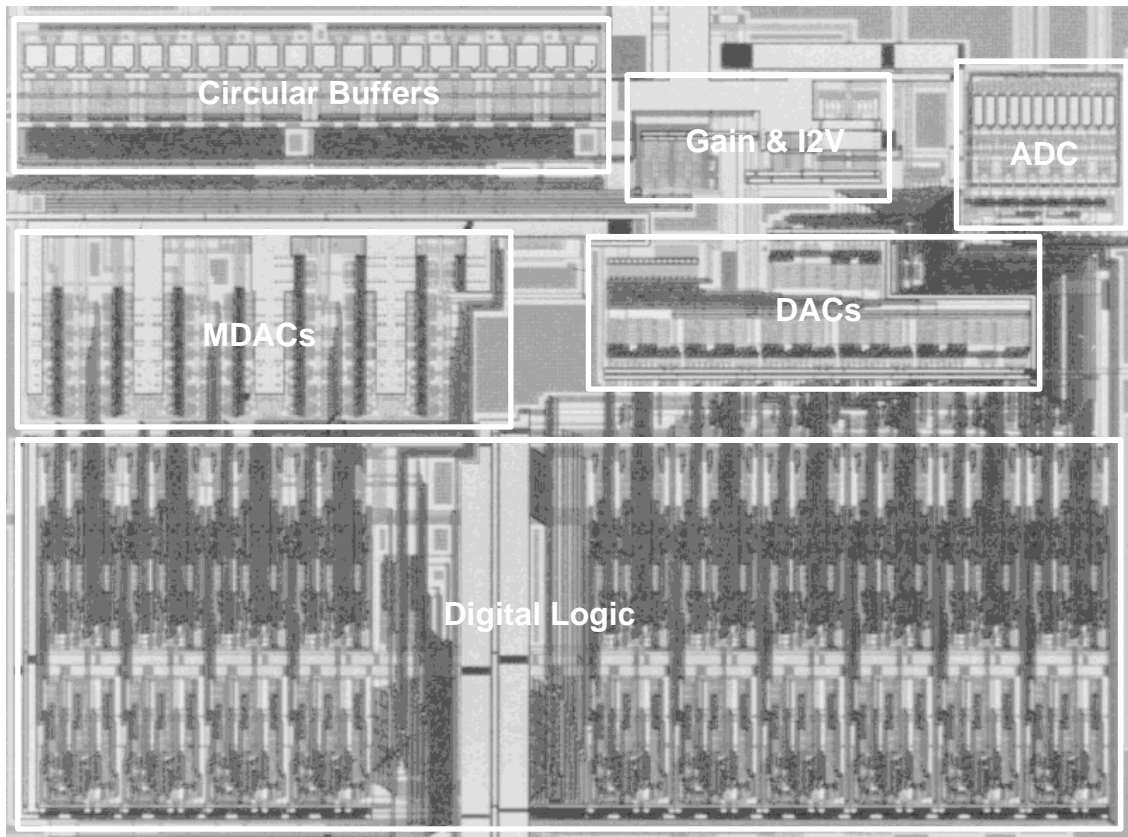


Figure 11. Photograph of active die area.

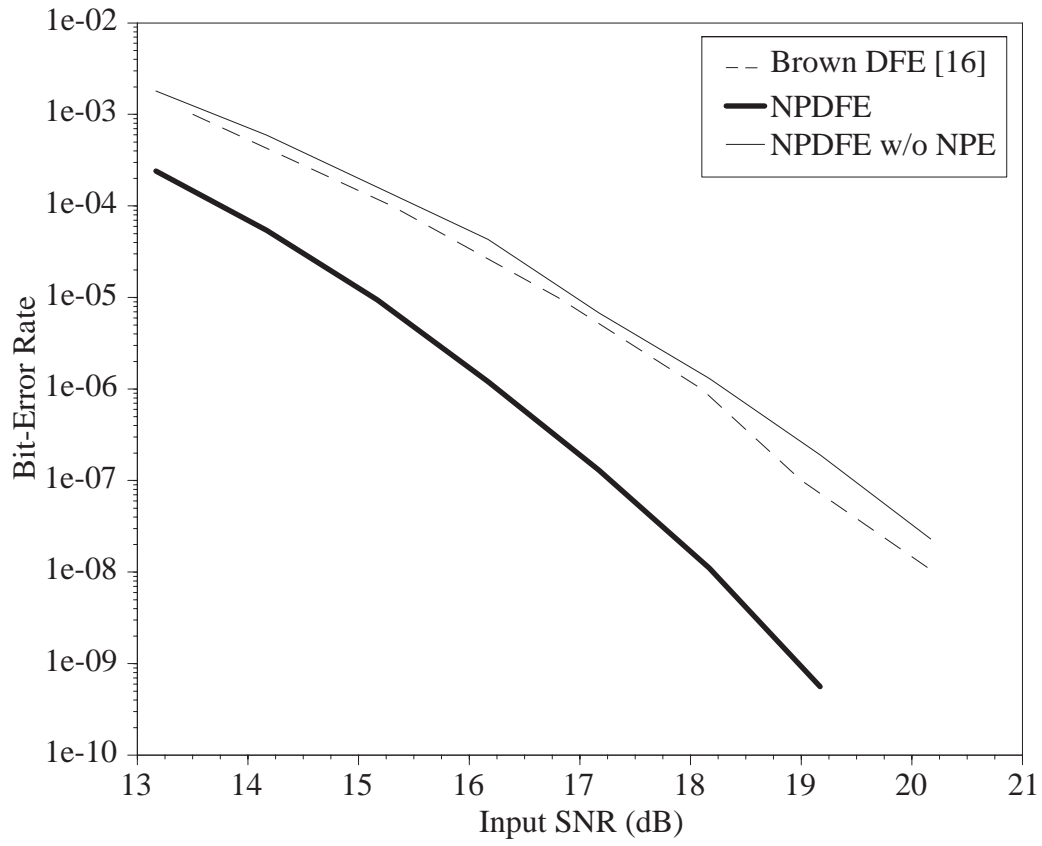


Figure 12. Measured BER at 100 Mbps and $PW_{50}=2.5T$.

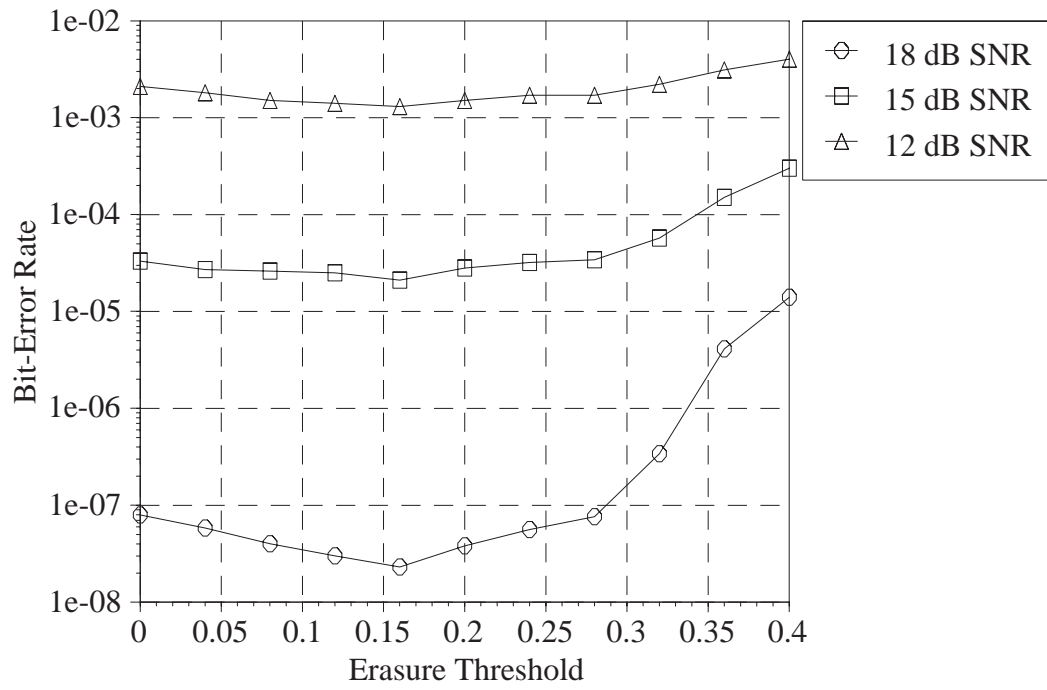


Figure 13. Effect of normalized erasure threshold on BER.

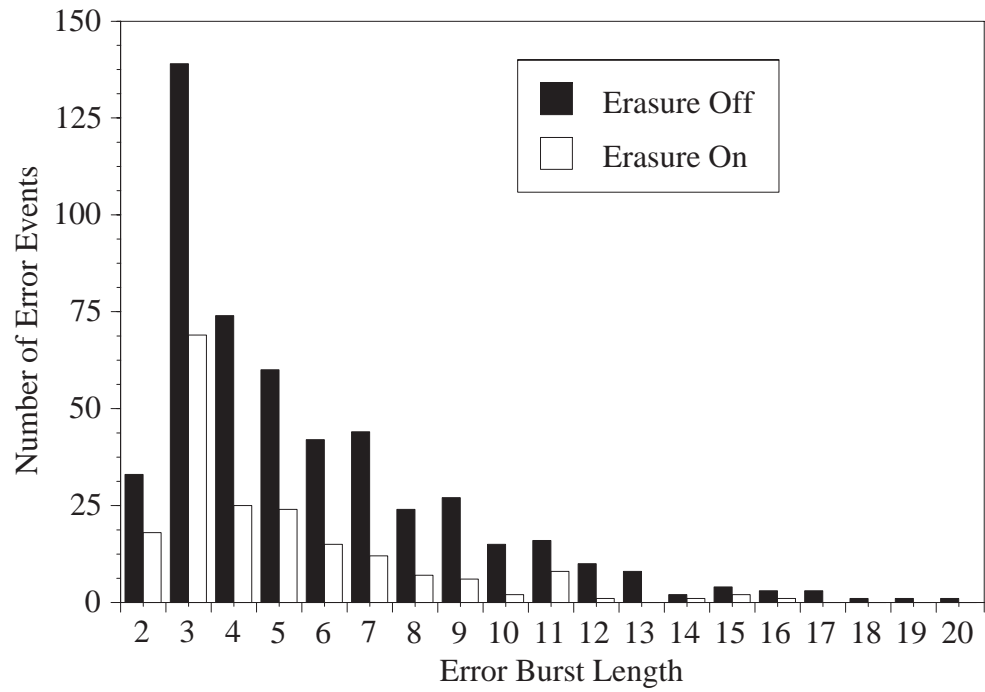


Figure 14. Error histogram with erasure on and off.

Technology	0.5 μ m SPTM CMOS
Core Area	1.3 mm ²
Equalizer Structure	FE = 3rd order FIR NPE = 3rd order DFE = 5 taps for ISI + 1 DC offset tap
Power Dissipation	130 mW
Max Data Rate (1/T)	100 Mbps
SNR for 10 ⁻⁸ BER	18.3 dB

Table 1. NPDFE measured performance summary with $PW_{50} = 2.5T$, $V_{DD} = 3.3$ V, and 25^o C.