A Mixed-Signal Decision-Feedback Equalizer That Uses Parallelism

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ABSTRACT

A mixed-signal decision-feedback equalizer (DFE) that uses parallelism is described. The parallelism in the look-ahead DFE achieves an increase in the data rate over that of a conventional DFE. The DFE occupies 23 mm^2 in a 2-μm CMOS process, operates at 55 Mb/s and dissipates 450 mW.

INTRODUCTION

Decision-feedback equalization is a sampling detector that can be used when intersymbol interference (ISI) is present, such as in a disk-drive read channel [1,2,3] or other communication channels [4]. The decision-feedback equalizer (DFE) is used in combination with a linear forward equalizer to remove all ISI. Fig. 1 shows the block diagram of a complete hard-disk read channel that uses a DFE. The read channel contains many components in addition to the DFE: timing recovery, forward equalizer, automatic gain control (AGC), and preamp.

This paper describes a mixed-signal implementation of a look-ahead DFE for a disk-drive read channel. This DFE is an extension of a previous mixed-signal DFE design [5]. The key difference here is the use of parallelism in the look-ahead structure, which achieves an increase of the data rate of the DFE. The data rate of the new DFE is 55 Mb/s, while the DFE in [5] operates at 35 Mb/s. Both DFEs are fabricated in the same technology and use many of the same circuits.

DFE BACKGROUND

The forward equalizer in Fig. 1 is responsible for removal of precursor ISI. The DFE removes the remaining postcursor ISI by using a linear combination

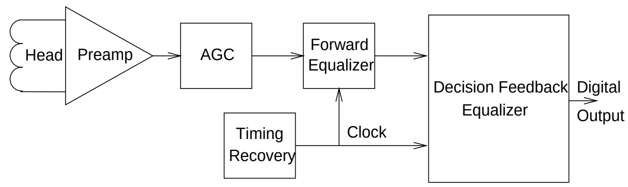

Fig. 1: Disk-drive read channel block diagram

of past decisions to cancel the interference [1,4]. The postcursor ISI, ISI^+, at time nT can be expressed as a weighted summation of past bits, plus an offset:

$$ISI^{+}(n) = h_{offset} + \sum_{k=1}^{M} h(k)\hat{y}(n-k) \qquad (1)$$

where $\{h(k)\}$ is the response of the disk channel plus forward equalizer sampled at bit times kT, $\{\hat{y}(n-k)\}$ is past binary data, and h_{offset} is the d.c. offset. M is the number of bits that contribute significant postcursor ISI.

Fig. 2 shows an adaptive 5-tap DFE, which can cancel the postcursor ISI. Four taps cancel postcursor ISI, and one tap cancels the d.c. offset. Based on simulations using a Lorentzian channel model [1] with $PW_{50} = 2T$ and appropriate forward equalization, a 5-tap DFE is sufficient to achieve MSE < –25 dB for a noise-free channel, where MSE = $E(e^2(n))$ is the mean-squared error and $e(n) = \hat{y}(n) - \tilde{y}(n)$ is the error across the slicer.

The coefficients d_k in Fig. 2 can be determined by adapting the DFE using an algorithm which minimizes the MSE. Once the DFE has adapted, the DFE coefficients are $d_k = -h(k)$ for $1 \le k \le M$ and $d_0 = -h_{offset}$. Here d_k is the coefficient at tap k, d_0 is the d.c. offset cancellation coefficient, and M is the number of taps. With these coefficients, the ISI^+ is canceled by the DFE.

The DFE coefficients can be adapted using the sign-LMS algorithm [4,6]:

$$d_k(n+1) = d_k(n) + \beta \mathrm{sign}(e(n))\hat{y}(n-k) \quad \text{for } 1 \le k \le M$$

and $$d_0(n+1) = d_0(n) + \beta \mathrm{sign}(e(n)) \ , \qquad (2)$$

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where $\beta << 1$ is the gain of the update integrator and n is time. The sign-LMS update equation for each coefficient can be implemented by a L-bit up/down counter if $\beta = 2^{-L}$ because $\text{sign}(e(n))\,\hat{y}(n-k)$ is either +1 or –1. The sign-LMS update for coefficient d_1 is shown in Fig. 2.

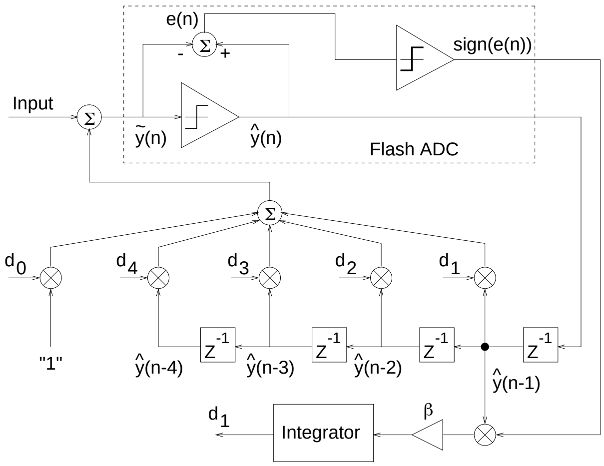

Fig. 2: DFE with sign-LMS update shown for coefficient d_1. Z^{-1} is a delay of a bit period T.

A MIXED-SIGNAL DFE ARCHITECTURE

Fig. 3 shows a block diagram of a mixed-signal DFE, which is practically identical to the design in [5]. (The only difference is that the ADC outputs a 2-level sign(e) here rather than the 3-level quantized error signal $q(e)$ in [5].) The look-ahead DFE that is described in the next two sections is a modification of this mixed-signal DFE and uses many of these circuit blocks. The input is an analog current coming from a preceding analog forward equalizer [7-11]. A current-to-voltage (I2V) converter feeds a small flash ADC which outputs the binary decision $\hat{y}(n)$ and $\text{sign}(e(n))$ using only 3 comparators. Digital logic and 10-bit counters are used in the coefficient update. The digital output of the counters feed resistor-string 6-bit digital-to-analog converters (DACs) that drive current-output multipliers [12]. The multipliers perform the multiplication of the past binary decision $\hat{y}(n-k)$ by the analog coefficient value d_k. The current outputs are all summed at the I2V input simply by connecting them together.

LOOK-AHEAD DFE CONCEPT

The critical, speed-limiting feedback loop in Fig. 3 is through the I2V converter, flash ADC and d_1 multiplier. This feedback loop must have a total delay less than one bit period, T. Although shown as a separate delay element, most of the Z^{-1} delay in this critical loop is in the flash ADC. To reduce T and thereby increase the data rate of the DFE, parallelism can be used.

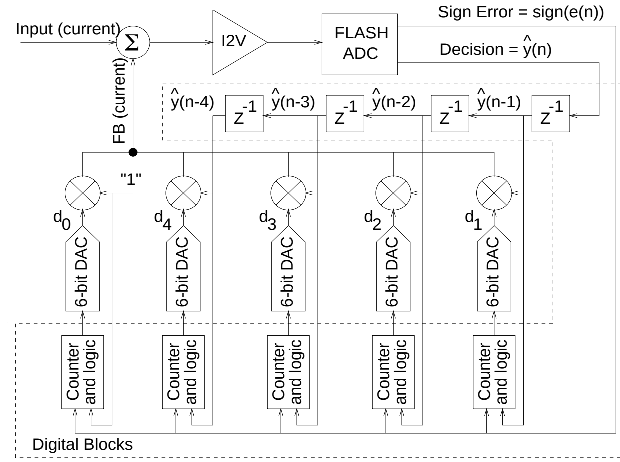

Fig. 3: Mixed-signal DFE showing analog and digital circuit blocks. The digital blocks are enclosed by the dashed line.

Parallelism is used in the look-ahead (LA) DFE to change the critical, speed-limiting feedback loop to being through the d_2 multiplier rather than the d_1 multiplier [13]. The LA DFE can be explained conceptually using Fig. 4. There are two parallel processing paths in the LA DFE. Each path is a copy of the DFE of Fig. 2 with the following changes. The upper path always assumes $\hat{y}(n-1) = +1$ and uses that value in its convolution calculation. The lower path always assumes and uses $\hat{y}(n-1) = -1$. Both paths use the same d_k coefficients and the same (correct) values of $\hat{y}(n-2)$, $\hat{y}(n-3)$ and $\hat{y}(n-4)$ in the convolution calculation. The two parallel paths produce inputs to the upper and lower ADCs that output two tentative decisions $\hat{y}_{+1}(n)$ and $\hat{y}_{-1}(n)$, where $\hat{y}_{+1}(n) = [\,\hat{y}(n)$, if $\hat{y}(n-1) = +1\,]$ and $\hat{y}_{-1}(n) = [\,\hat{y}(n)$, if $\hat{y}(n-1) = -1\,]$.

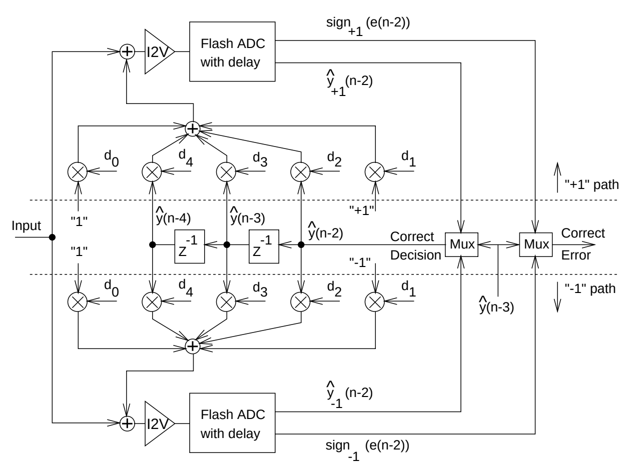

Fig. 4: LA DFE block diagram. LMS update hardware is not shown.

Selection between tentative decisions $\hat{y}_{+1}(n)$ and $\hat{y}_{-1}(n)$ could be made using $\hat{y}(n-1)$, if these values were available at time n. However, at time n, the tentative decisions and $\hat{y}(n-1)$ are essentially 'stuck' inside the ADC and are not available. Therefore, the selection is delayed and is made between the delayed tentative decisions $\hat{y}_{+1}(n-2)$ and $\hat{y}_{-1}(n-2)$, with the selection determined by the value of $\hat{y}(n-3)$. At start-up, a training sequence of known data is used for rapid and reliable convergence [4]. This sequence of known data initializes the selection process, giving known values for the select signal $\hat{y}(n-3)$ during training. At the end of the training data, the selection process can continue to operate using the correct delayed decision that is output by the LA DFE. The two paths also output tentative sign(e) signals, one of which is selected by the past decision $\hat{y}(n-3)$. The selected sign($e(n-2)$) signal is used to update the coefficients, using a delayed version of the sign-LMS coefficient update algorithm [14]:

$$d_k(n+1) = d_k(n) + \beta \operatorname{sign}(e(n-2))\hat{y}(n-k-2) \quad \text{for } 1 \le k \le M$$

and

$$d_0(n+1) = d_0(n) + \beta \operatorname{sign}(e(n-2)) \ . \tag{3}$$

In the LA DFE, the critical, speed-limiting feedback loop is through the d_2 multiplier and now must have a total delay less than $2T$. More than half of this loop delay ($>T$) is in the flash ADC and the rest ($<T$) is in the mux, d_2 multiplier, and I2V.

LOOK-AHEAD DFE DESIGN

The two paths in the LA DFE in Fig. 4 use the architecture shown in Fig. 3. All analog circuits are fully differential to minimize the coupling of digital noise into the analog signal paths. An I2V converter followed by a flash ADC is used in each of the upper and lower paths. The ADC uses pipelined comparators to allow decisions to be made at a $1/T$ rate, with a delay less than $2T$ through the ADC. The comparators are as described in [15], except that a different input sampling network is used [16]. The critical feedback loop through the d_2 multiplier allows a total delay of $2T$ through the I2V, flash ADC, mux and multiplier. The I2V and multipliers are the same as those used in [5], and the DACs and ADCs use the same structures as in [5] but have undergone minor modifications.

The LMS update circuitry and DACs (not shown in Fig. 4) and decision delay line are shared by the two paths. The update circuitry can be shared because only the selected past decisions and error signal are used to update the coefficients. This sharing saves both power and IC area. To further reduce area, one up/down counter is shared for updating the five d_k coefficients. The logic design is such that two clock cycles are required to update a coefficient. Therefore, each coefficient is updated every 10th clock cycle, and its value is stored in a register after updating. This scheme slows convergence but does allow coefficient adaption. Since the main goal of this work is to demonstrate that parallelism in the analog signal paths can increase the data rate without a significant degradation of performance, speed of convergence was not a major concern. The LA DFE could easily be modified to have a dedicated counter for each coefficient.

The two parallel paths in the LA DFE must be identical in order to achieve the same performance as the conventional DFE in Fig. 2. In an IC implementation, the analog circuits in these paths will be mismatched to some extent. The effect of d.c. offset mismatch between the two paths and convolution-path gain mismatch were simulated [17]. The results of these simulations are that the LA DFE can tolerate convolution-path gain mismatch of 10% and large offsets with negligible degradation. In the LA DFE, coefficient d_0 cancels the average input-referred offset in the two paths, and d_1 cancels mismatch in the offset of the two paths in addition to ISI caused by $\hat{y}(n-1)$ [17]. To achieve good matching between the upper and lower paths, circuits that have similar functions (the I2Vs, flash ADCs and convolution multipliers) are placed close together with identical orientations.

MEASURED PERFORMANCE

The LA DFE was tested by generating a realistic DFE input signal that contains only postcursor ISI using software, sending that signal through an arbitrary waveform generator, and adding bandlimited noise to the signal before it enters the LA DFE. The test signal is generated using a Lorentzian channel model with $PW_{50}=2T$ and a 5-tap FIR forward equalizer.

A plot of measured bit-error rate (BER) versus signal-to-noise ratio (SNR) is shown in Fig. 5 for a data rate of 55 Mb/s. This data was gathered using coefficients that were found by adapting, but adaption was turned off when measuring BER. The sampling phase is adjusted by hand. For comparison, simulated BER performance of the DFE in Fig. 2 is also plotted. This early data shows that the LA DFE is functional and operates faster than the DFE in [5]. That DFE used similar circuitry, the same CMOS technology, and the architecture in Fig. 3. It had a maximum operating speed of 35 Mb/s. The parallelism is allowing faster operation.

The IC layout is shown in Fig. 6. The IC was fabricated in a 2-μm CMOS process. The total active area of the LA DFE is 23 mm^2. The measured performance is summarized in Table 1.

CONCLUSION

A mixed-signal look-ahead DFE was presented that increases the data rate by using parallelism. The area increase due to parallelism is much less than a factor of two because all blocks do not have to be duplicated.

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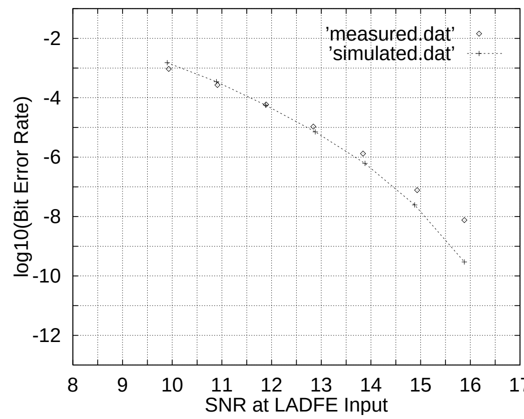

Fig. 5: Measured BER vs. SNR at 55 Mb/s, and simulated BER of a DFE.

Fig. 6: Layout plot of the LA DFE IC.

Parameter	**Value**
Process	2 μm CMOS
Active Area	23 mm^2
Power Supply	5 V
Power Dissipation	450 mW @ 55 Mb/s
Data Rate	55 Mb/s
Number of taps	4 for ISI, 1 for d.c. offset

Table 1: LA DFE Performance Summary