MODELING MEMORY ERRORS IN PIPELINED ANALOG-TO-DIGITAL CONVERTERS

John P. Keane, Paul J. Hurst, and Stephen H. Lewis
Dept. of Electrical and Computer Eng.
University of California,
Davis, CA 95616, USA.
email: jpkeane@ieee.org

ABSTRACT
Switched-capacitor implementations of pipelined ADCs contain several sources of memory errors, including capacitor dielectric absorption/relaxation, incomplete stage reset at high clock rates, and parasitic capacitance effects when op amps are shared between subsequent pipeline stages. This paper describes these sources of memory errors and presents a unified model for their effect. The dependence of these errors on circuit parameters and ADC sampling rate is also discussed. The effect of these errors on ADC linearity is then analyzed, showing how memory errors can limit the performance of a pipelined ADC.

KEY WORDS
Analogue circuits, analog-digital conversion, switched capacitor circuits, modelling, dielectric materials.

1 Introduction

A conventional pipelined analog-to-digital converter (ADC) architecture is shown in Figure 1. It consists of an input sample-and-hold amplifier (SHA) and N pipelined stages. All signals shown are normalized to the reference voltage V_{ref} (e.g. $x_0 = V_{in}/V_{ref}$ where V_{in} is the ADC input voltage). The SHA samples the input signal x_0 at a uniform rate $f_s = 1/T$ where T is the sample period, multiplies it by a gain G_0 (where $G_0 \approx 1$ in general) and holds the output x_1 as the input of the first pipeline stage.

Each pipeline stage consists of an analog-to-digital sub-converter (ADSC), a digital-to-analog sub-converter (DASC) and a SHA with nominal gain G_i. The ADSC generates a digital estimation d_i of the stage input x_i. Using a DASC, d_i is converted to an analog signal $K_i d_i$ that is subtracted from x_i to form the residue y_i.

$$y_i = x_i - K_i d_i \tag{1}$$

This residue is multiplied by a gain G_i and then sampled and held as the input x_{i+1} to the next pipeline stage. In general, the final stage N is simply an ADSC as only its decision output d_N, and not its amplified residue, is required. The transfer function of each stage can be written

$$x_{i+1} = G_i(x_i - K_i d_i) \tag{2}$$

The ADC produces a digital output $\widehat{x}_0[k]$ that is a digital estimate of the normalized analog input $x_0[k] = V_{in}(kT)/V_{ref}$. This output is generated using digital logic to calculate a weighted sum of the stage decision outputs $\underline{d} = (d_1, d_2, \ldots, d_N)^T$ using the weights $\underline{w} = (w_1, w_2, \ldots, w_N)^T$

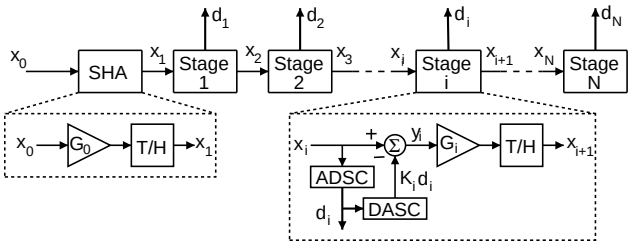

Figure 1. Pipeline ADC

$$\widehat{x}_0 = \underline{w}^T \underline{d} = \sum_{i=1}^{N} w_i d_i \tag{3}$$

By referring each DASC output to the ADC input, the ideal values of these weights are computed as

$$w_i = K_i \prod_{j=0}^{i-1} \frac{1}{G_j} \tag{4}$$

If the ideal weights in (4) are used in (3) then, assuming all components are ideal and noiseless,

$$\widehat{x}_0 = x_0 + q \tag{5}$$

where the quantization error q is given by

$$q = (K_N d_N - x_N) \prod_{j=0}^{N-1} \frac{1}{G_j} \tag{6}$$

As additional stages are added to the pipeline, q becomes smaller, and the resolution of the converter increases. In order to simplify the digital calculation in (3), the gains K_i and G_i are usually designed to be integer powers of 2.

In practice, accurate interstage gain is difficult to ensure in a modern VLSI process due to factors such as capacitor mismatch and limited op amp gain. In order to correct

for linearity errors that would result from interstage gain inaccuracy, calibration techniques[1, 2] can be used. While these calibration techniques allow correction for interstage gain errors, they assume that each stage of the pipeline is memoryless. In practice, this assumption may not be true, and memory effects can cause linearity errors that are not correctable using these conventional techniques. This paper describes some sources of these memory errors and the effect that they have on pipelined ADC linearity.

2 Sources of Memory Effect

2.1 Capacitor dielectric absorption / relaxation effects

The memory effect of dielectric relaxation on successive-approximation ADCs was described in [3]. Recently this effect was also shown to limit the linearity of a pipelined ADC[4] for a process using a silicon nitride (SiN) dielectric rather than conventional silicon dioxide (SiO_2) dielectric for capacitors. SiN capacitors have the advantage of much higher density than SiO_2 capacitors and so have the potential to reduce die cost when large capacitors are required. However, these capacitors exhibit a much larger memory effect due to capacitor dielectric absorption/relaxation. This phenomenon is essentially due to carriers being trapped in the dielectric and slowly released over time and can be observed [4, 5] by the following three-phase procedure:

1. Charge a capacitor to a voltage $V_C = V_{init}$.
2. At time $t = 0$, discharge the capacitor by shorting its terminals together until time $t = t_0$.
3. Allow the capacitor to float until time $t = t_f$.

The charge trapped in the dielectric during phase 1 above tends to gather back on the capacitor plates during phase 3, ideally following a logarithmic law[3, 4]

$$V_C(t_f, t_0) = \gamma V_{init} \tag{7}$$

where $\gamma = \kappa ln(t_f/t_0)$ and κ is determined by the intensity of the trap/release process in the dielectric.

A common switched-capacitor implementation[6] of the pipeline stage in Fig. 1 is shown in simplified form in Fig. 2(a). Although a single-ended circuit is shown for simplicity, in practice a fully differential circuit would be used. A timing diagram for the clocks ϕ_1 and ϕ_2 used in this stage are shown in Fig. 2(b). Although short non-overlapping times are often used between clock phases in practice[6], these are not shown here for simplicity and the durations t_1 and t_2 of $\phi_1$and ϕ_2, respectively are both chosen to be $T/2$. If the op amp is ideal (i.e. $a \to \infty$, offset=0) and there is no memory effect, then the output at the end of phase 2 can be found from

$$\begin{aligned} C_f V_{i+1}(kT + T/2) = (C_f + C_{in})V_i(kT) \\ -C_{in}V_{DASC}(kT + T/2) \end{aligned} \tag{8}$$

The parasitic capacitor C_p has no effect in (8) as the inverting terminal of the op amp is at the ground potential at the end of each phase.

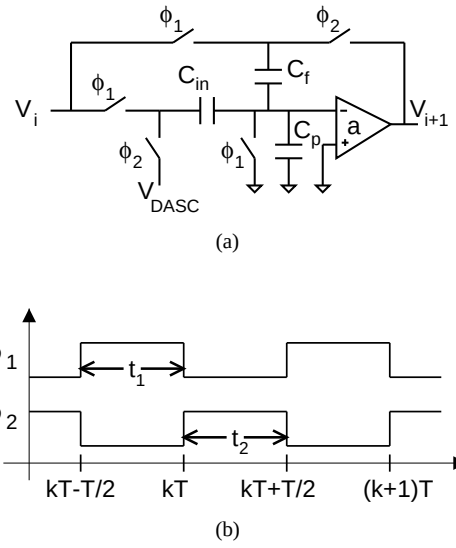

Figure 2. (a)Switched-capacitor pipeline stage using flip-around architecture, (b) timing diagram (ϕ_1 and ϕ_2 are non-overlapping).

In this paper, the time index n (e.g. $d_i[n]$) is used to denote the signals corresponding to a given ADC input sample and conversion cycle. Although the stages in a pipelined ADC operate at different times on residues that correspond to one ADC input sample, any signal that refers to the conversion of the same input sample will be given the same index. For example, although each stage output decision $d_i[n]$ for a given input sample is generated at a different time, $d_i[n]$ refers to the decision of stage i corresponding to the conversion of the input sample $x_0[n] = x_0(nT)$. Using this convention, define the normalized variables

$$x_i[n] = V_i(kT)/V_{ref} \tag{9}$$

$$x_{i+1}[n] = V_{i+1}(kT + T/2)/V_{ref} \tag{10}$$

$$d_i[n] = V_{DASC}(kT + T/2)/K_{DASC} \tag{11}$$

where K_{DASC} is the DASC gain in volts. In a typical pipelined ADC[6], all stages, including the SHA, have a delay of T/2. In this case $k = n + 0.5i$ in (9), (10) and (11). Substituting these expressions into (8) gives

$$x_{i+1}[n] = G_i\left(x_i[n] - K_i d_i[n]\right) \tag{12}$$

$$G_i = (1 + C_{in}/C_f) \tag{13}$$

$$K_i = (K_{DASC}/V_{ref})\, C_{in}/\left(C_{in} + C_f\right) \tag{14}$$

Hence, for ideal linear capacitors without memory effect, this switched-capacitor pipeline stage can be modeled as shown in Fig. 1 with the transfer function given in (2).

In [4] a simple model for the memory effect caused by capacitor dielectric absorption/relaxation was given, representing the phenomenon as a simple one-tap finite-impulse response effect. In this case, only relaxation due to charge absorbed in the immediately preceding phase is considered.

Using normalized variables, the stage transfer function including this memory effect can be written as:

$$x_{i+1}[n] = G_i\left(x_i[n] - K_i d_i[n]\right) + \gamma_f x_{i+1}[n-1] + \gamma_{in} G_i K_i d_i[n-1] \quad (15)$$

where G_i and K_i are the same as for (12) above. Here γ_{in} and γ_f model the memory effect of C_{in} and C_f, respectively. From (7),

$$\gamma_{in} = \kappa_{in} ln(T/t_1) = \kappa_{in} ln(2) \quad (16)$$
$$\gamma_f = \kappa_f ln(T/t_1) = \kappa_f ln(2)$$

as $t_1 = T/2$ in this case. If both C_f and C_{in} use the same dielectric material $\kappa_{in} \approx \kappa_f$ and so $\gamma_{in} \approx \gamma_f$. From (16), it can be seen that in this case the magnitude γ of this memory effect is *independent* of the sampling rate $f_s = 1/T$.

2.2 Incomplete stage reset effects

In general, the period T is chosen to be long enough to allow settling in each phase of the residue amplifier operation to the required accuracy of the converter. For high speed operation, this requires large switches with low on-resistance, and a high-speed op amp to minimize the settling time during the amplification phase ϕ_2.

Incomplete settling during ϕ_2 can be modeled as errors in the interstage gain G_i and the DASC gain K_i if the settling is linear [2]. Such errors can be compensated for using calibration techniques for interstage gain errors [1, 2]. However, incomplete settling during the reset phase ϕ_1 causes memory-effect errors that can not be corrected using these approaches. To illustrate this point, consider again the pipeline stage in Fig. 2. Let the voltages on the capacitors C_{in} and C_f be $V_{C_{in}}$ and V_{C_f}, respectively. Ideally, $V_{C_{in}} = V_{C_f} = V_i$ at the end of ϕ_1. However, if the duration of ϕ_1 is too short to allow complete resetting of the voltages across C_{in} and C_f, $V_{C_{in}}$ and V_{C_f} at the end of ϕ_1 depend in part on the voltage changes that the circuit tries to impress during ϕ_1. From Fig. 2(b), phase ϕ_1 of sample period k begins at time $t = kT - T/2$ and ends at $t = kT$. If linear settling can be assumed, then

$$V_{C_f}(kT) = V_i(kT)\left(1 - \gamma_f\right) + \gamma_f V_{C_f}\left(kT - \frac{T}{2}\right) \quad (17)$$

$$V_{C_{in}}(kT) = V_i(kT)\left(1 - \gamma_{in}\right) + \gamma_{in} V_{C_{in}}\left(kT - \frac{T}{2}\right) \quad (18)$$

where the factors γ_f and γ_{in} are constants determined by the duration t_1 of ϕ_1 and the settling time constants of C_f and C_{in}. A fraction of the previous capacitor voltage is retained after the reset phase in (17) and (18) resulting in a memory effect similar to that described in Section 2.1. In this case, the values of γ_f and γ_{in} can be reduced by operating at a lower rate $f_s = 1/T$, which increases t_1.

If the op amp is ideal and complete settling is assumed during ϕ_2, then the stage transfer function in this case is given by (15), but with

$$G_i = (1 - \gamma_f) + (1 - \gamma_{in}) C_{in}/C_f. \quad (19)$$

Hence, the stage output $x_{i+1}[n]$ depends on its previous output $x_{i+1}[n-1]$ and DASC input $d_i[n-1]$, which constitutes a memory effect that can not be corrected for using interstage gain calibration techniques.

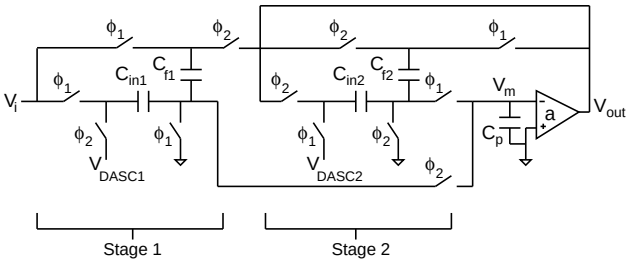

Figure 3. Switched-capacitor pipeline stage using shared op amp. $V_{out} = V_{i+1}$during ϕ_2 and $V_{out} = V_{i+2}$ during ϕ_1.

2.3 Op amp sharing effects

As described above, the pipeline stage shown in Fig. 2 operates in two phases. During the reset phase ϕ_1 the capacitors are reset by charging them to the stage input voltage V_i. During the amplification phase ϕ_2, the op amp is used to perform the subtracting and amplification functions of the stage. In general, subsequent stages of the pipeline operate in opposite phases, i.e. while stage 1 amplifies, stage 2 is reset and vice-versa. Since the op amp is only required during the amplification phase, op amp sharing between subsequent stages has been proposed [7] in order to reduce the number of required op amps by a factor of 2 and hence reduce power and area requirements. The structure used in [7] is shown in Fig. 3. Comparing to Fig. 2 shows that Fig. 3 contains two cascaded pipeline stages that share a single op amp. During ϕ_2 the op amp generates the output $V_{out} = V_{i+1}$ of stage 1, while driving the input of stage 2. During ϕ_1, the op amp generates the output $V_{out} = V_{i+2}$ of stage 2 and drives subsequent stage 3. Additional switches are added to the negative op amp input terminal (the summing node), to allow it to be switched between the two stages.

While this architecture can yield significant power savings, it can result in memory effects due to the parasitic capacitance C_p at the negative terminal of the op amp, as noted in [7]. This memory effect occurs when the op amp gain a is limited and so the voltage $V_m = -V_{out}/a$ at the end of the amplifying phase is significant. At the end of ϕ_2, the op amp output $V_{out} = V_{i+1}(kT - T/2)$, so its input is $V_m = -V_{i+1}(kT - T/2)/a$. At $t = kT + T/2$ the op amp is switched from stage 1 to stage 2 and the capacitor C_p injects a charge $-C_p V_{i+1}(kT - T/2)/a$ at the summing node of the second stage while it is generating $V_{out} = V_{i+2}(kT)$ during ϕ_1. The transfer function of stage 2 can be calculated as

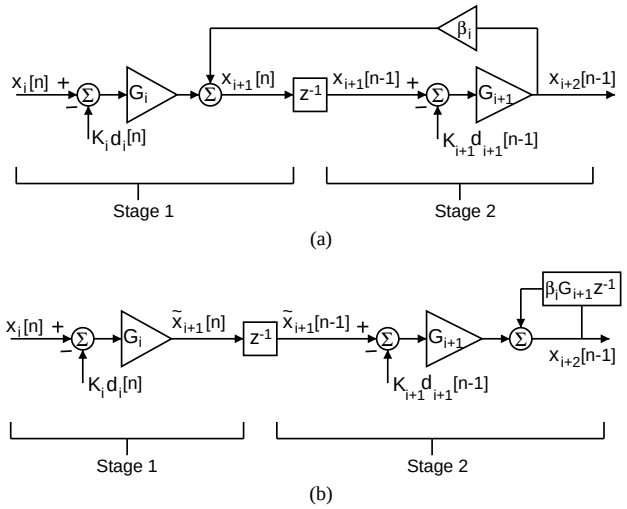

Figure 4. Model of opamp sharing

$$x_{i+2}[n] = G_{i+1}\left(x_{i+1}[n] - K_{i+1}d_{i+1}[n]\right) \quad (20)$$

$$G_{i+1} = \frac{C_{f2} + C_{in2} + C_p/a}{C_{f2} + (C_{f2} + C_{in2} + C_p)/a} \quad (21)$$

$$K_{i+1} = \left(\frac{K_{DASC2}}{V_{ref}}\right)\frac{C_{in2}}{C_{f2} + C_{in2} + C_p/a} \quad (22)$$

Since the output $x_{i+2}[n]$ in (20) depends only on the current input $x_{i+1}[n]$ and stage decision $d_{i+1}[n]$, no memory effect results. The parasitic capacitor C_p causes only a change in the factors K_i and G_i.

Now consider stage 1 when the op amp is switched from generating $V_{out} = V_{i+2}(kT)$ during ϕ_1 to generating $V_{out} = V_{i+1}(kT+T/2)$ during ϕ_2. In this case, the capacitor C_p injects a charge $-C_pV_{i+2}(kT)/a$ onto the summing node of stage 1 during ϕ_2. The transfer function of stage 1 can be calculated as

$$x_{i+1}[n] = G_i\left(x_i[n] - K_i d_i[n]\right) + \beta_i x_{i+2}[n-1] \quad (23)$$

$$G_i = \frac{C_{f1} + C_{in1}}{C_{f1} + (C_{f1} + C_{in1} + C_p)/a} \quad (24)$$

$$\beta_i = \frac{C_p/a}{C_{f1} + (C_{f1} + C_{in1} + C_p)/a} \quad (25)$$

$$K_i = \left(\frac{K_{DASC1}}{V_{ref}}\right)\frac{C_{in1}}{C_{f1} + C_{in1}} \quad (26)$$

Since the output x_{i+1} of stage 1 in (23) depends on the previous output x_{i+2} of stage 2, a memory effect exists that can result in nonlinearity. Combining (20) and (23) gives the model shown in Fig. 4(a). This model shows that a delayed version of the output of the even stage is added to the output of the odd stage. The model can be changed so that the memory effect is completely contained withing one stage, as shown in Fig. 4(b). The key step in this transformation is to note that an even stage follows and processes the output of each odd stage. Therefore, this memory effect can be modeled entirely in the even stages without changing the output of a pipelined ADC that consists of a cascade of the structures shown in Fig. 3. In this case, an equivalent model for the ADC transfer function is given when each stage is modeled as

$$x_{i+1}[n] = G_i\left(x_i[n] - K_i d_i[n]\right) + \gamma_i x_{i+1}[n-1] \quad (27)$$

and $\gamma_i = 0$ for i odd and $\gamma_i = G_i\beta_{i-1}$ for i even. Eqn. (25) shows that the memory effect in this case is *independent* of the sampling rate $f_s = 1/T$ but can be reduced by increasing the op amp gain a and/or decreasing the parasitic capacitance C_p. Alternatively, an additional clock phase can be added to reset C_p after ϕ_1, but this adds extra complexity and may reduce the maximum conversion rate.

3 Linearity errors due to memory effects

To consider the effect on converter accuracy of the memory effect in each stage, consider the stage transfer function. The result in (15), which applies to the memory effects described in Sections 2.1 and 2.2, can be summarized by the expression:

$$\begin{aligned} x_{i+1}[n] = {} & G_i\left(x_i[n] - K_i d_i[n]\right) \\ & + \gamma_i x_{i+1}[n-1] + \delta_i G_i K_i d_i[n-1] \end{aligned} \quad (28)$$

where γ_i and δ_i correspond to the memory effects γ_f and γ_{in} of the stage output and DASC output of stage i, respectively. The memory effect described in Section 2.3 resulted in the equivalent stage transfer function given in (27). This is identical to (28) except that $\delta_i = 0$ for all stages in this case. Computing the z-transform of (28) and rearranging terms gives

$$\begin{aligned} X_i(z) = {} & (1 - \delta_i z^{-1})K_i(z)D_i(z) \\ & + \frac{1}{G_i}(1 - \gamma_i z^{-1})X_{i+1}(z) \qquad 1 \le i \le N-1 \end{aligned} \quad (29)$$

where $X_i(z)$ and $D_i(z)$ are the z-transforms of $x_i[n]$ and $d_i[n]$, respectively. The input SHA (stage 0) can also be modeled by (29) if it is considered as a stage with the DASC removed (i.e. $D_0(z) = 0$). From (29), $X_{i+1}(z)$ is given by

$$X_{i+1}(z) = \frac{G_i}{1 - \gamma_i z^{-1}}\left(X_i(z) - (1 - \delta_i z^{-1})K_i D_i(z)\right) \quad (30)$$

The stage model using (30) is shown in Fig. 5(a). For the case where $\delta_i = 0$, as in the opamp sharing memory effect described in Section 2.3, the stage can be modeled as in Fig. 5(b). For the case where $\delta_i = \gamma_i$, as can often be assumed for the memory effects described in Sections 2.1 and 2.2, (30) can be rewritten as

$$X_{i+1}(z) = \frac{G_i}{1 - \gamma_i z^{-1}}X_i(z) - G_i K_i D_i(z) \quad (31)$$

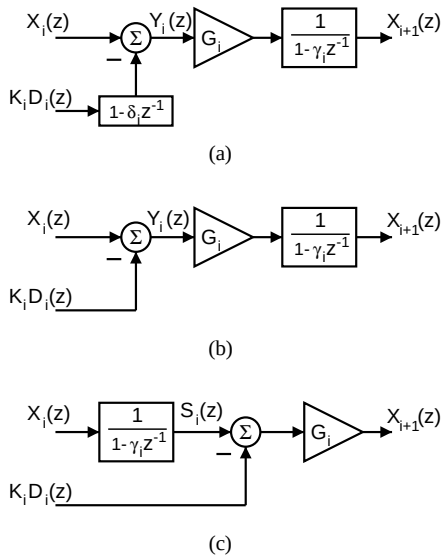

Figure 5. Pipeline stage model (a) including memory effect, (b) with $\delta_i = 0$, (c) with $\delta_i = \gamma_i$.

and modeled as shown in Fig. 5(c).

In general, the final pipeline stage (stage N) consists of an ADSC only and hence does not suffer from the memory effects discussed in Section 2. In this case, from (6), $X_N(z)$ can be written as

$$X_N(z) = K_N D_N(z) - Q(z) \prod_{k=0}^{N-1} G_K \tag{32}$$

where $Q(z)$ is the z-transform of the ADC quantization error $q[n]$. Starting with the definition (32) for $X_N(z)$, (29) is recursively applied for $i = N-1, N-2, \ldots, 0$ to give

$$\begin{aligned} X_0(z) = &\sum_{i=1}^{N} \left[w_i D_i(z)(1-\delta_i z^{-1}) \prod_{k=0}^{i-1}(1-\gamma_k z^{-1}) \right] \\ &-Q(z) \prod_{k=0}^{N-1}(1-\gamma_k z^{-1}) \end{aligned} \tag{33}$$

where w_i are the weights as defined in (4) and $\delta_N = 0$ when the final stage is an ADSC only.

If the expression in (3) is used to calculate the digital output $\widehat{x}_0[n]$, its z-transform $\widehat{X}_0(z)$ is given by

$$\widehat{X}_0(z) = \sum_{i=1}^{N} w_i D_i(z) \tag{34}$$

In this case, combining (33) and (34) gives

$$\begin{aligned} \widehat{X}_0(z) = &\frac{X_0(z)}{\prod_{k=0}^{N-1}(1-\gamma_k z^{-1})} + Q(z) \\ &+ \sum_{i=1}^{N} w_i D_i(z) \left(1 - \frac{1-\delta_i z^{-1}}{\prod_{k=i}^{N-1}(1-\gamma_k z^{-1})} \right) \end{aligned} \tag{35}$$

The first term in (35) corresponds to a linearly filtered version of the input $X_0(z)$. The second term corresponds to the quantization error of the converter. The last term contains a weighted sum of past stage decisions. This is the term that contributes nonlinearity to the overall ADC transfer function. To demonstrate the effects of this term on converter linearity, first consider only memory effect in the SHA (i.e. $\gamma_i = 0$ for $i > 0$ and $\delta_i = 0$ for all stages). Here, (35) becomes

$$\widehat{X}_0(z) = \frac{X_0(z)}{1-\gamma_0 z^{-1}} + Q(z) \tag{36}$$

Note that (36) has only linear filtering of $X_0(z)$, and hence will not degrade the linearity of the converter, although it will add a high-frequency pole to its frequency-domain transfer function, resulting in some low-pass filtering.

Next, consider memory effect only in the SHA and first pipeline stage (i.e. $\gamma_i = 0$ and $\delta_i = 0$ for $i > 1$). Here (35) becomes

$$\begin{aligned} \widehat{X}_0(z) = &\frac{X_0(z)}{(1-\gamma_0 z^{-1})(1-\gamma_1 z^{-1})} \\ &+ \frac{K_1 D_1(z)}{G_0} \left(\frac{\delta_1 - \gamma_1}{1-\gamma_1 z^{-1}} \right) z^{-1} + Q(z) \end{aligned} \tag{37}$$

An additional pole has been added to the linear filtering of the input $X_0(z)$ due to the memory effect of stage 1. The second term in (37) involves the previous values of the first stage decision d_1. Since these past decisions are correlated with the the current input X_0 in general, nonlinearity in the form of spectral tones will result from this term. However, in the common case where $\delta_1 \approx \gamma_1$, the second term in (37) will almost disappear and so the memory effect of the first stage *will not cause* significant ADC nonlinearity.

Extending the memory effect to two stages gives

$$\begin{aligned} \widehat{X}_0(z) = &\frac{X_0(z)}{\prod_{i=0}^{2}(1-\gamma_i z^{-1})} \\ &+ \frac{K_1 D_1(z)}{G_0} \left(\frac{(\delta_1 - \gamma_1 - \gamma_2) z^{-1} + \gamma_1 \gamma_2 z^{-2}}{(1-\gamma_1 z^{-1})(1-\gamma_2 z^{-1})} \right) \\ &+ \frac{K_2 D_2(z)}{G_0 G_1} \left(\frac{\delta_2 - \gamma_2}{1-\gamma_2 z^{-1}} \right) z^{-1} + Q(z) \end{aligned} \tag{38}$$

In this case the output contains terms relating to previous decisions d_1 and d_2 of stage 1 and stage 2, respectively. Even in the case where $\gamma_i = \delta_i$, terms relating to previous values of d_1 will remain, causing converter nonlinearity.

Intuitively, the reason that memory effect in the first stage does not cause nonlinearity when $\gamma_1 = \delta_1$ is that the memory effect of the output x_2 and the decision d_1 combine to form an equivalent memory effect on the first stage input x_1 only, as shown in Fig. 5(c). Since x_1 contains no quantization error, only linear filtering of the input results. However, since the output of each stage in a pipelined ADC is an amplified version of the quantization error of

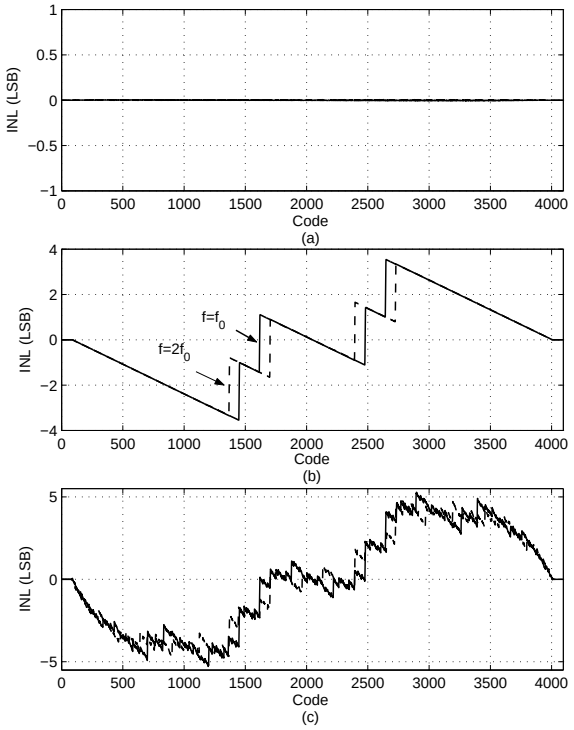

Figure 6. Simulated INL at 12-bit level for 1.5b/stage pipeline ADC with $\gamma_i = \delta_i = 0.005$ (a) for first stage only, (b) for first 2 stages, and (c) for all 12 stages with input full-scale sinewave at frequencies $f_0 \approx 0.007/T$ (solid) and $2f_0$ (dashed).

the previous stage, memory effects in subsequent stages will include this nonlinear quantization error and hence cause overall converter nonlinearity. This is shown when the memory effect is extended to 2 stages in (38).

Fig. 6 shows the simulated converter integral nonlinearity (INL) at 12-bit level for a conventional 12-stage 1.5 bit/stage pipeline ADC[6]. A 1.5 bit stage has nominal gain $G_i = 2$, ADSC thresholds at $\pm V_{ref}/4$ and DASC levels of $0, \pm V_{ref}/2$. The test signal is an input sinewave with amplitude 95% of full-scale at frequencies $f_0 = 0.007/T$. (solid) and $2f_0$ (dashed). The result in Fig. 6(a) is for memory effect with $\gamma_i = \delta_i = 0.005$ for the first stage only. Since the ADC is otherwise ideal, the INL is almost zero in this case. This verifies that memory effect in the first stage when $\gamma_1 = \delta_1$ does not cause nonlinearity. In Fig. 6(b), the INL is shown where the first two stages have a memory effect with $\gamma_i = \delta_i = 0.005$ and all others are ideal. The memory effect results in an INL of ± 3.7 LSB. When the input sinewave frequency is doubled from f_0 to $2f_0$, the width of the INL discontinuities around the first stage ADSC thresholds of $\pm V_{ref}/4$ increases. Hence, the measured INL is frequency-dependent. These discontinuities are caused when an input sample is immediately preceded by a sample that is on the other side of an ADSC threshold. In this case, the DASC output jumps by one level, but a memory still exists of the previous DASC output resulting in a memory error. When the input frequency increases, the difference between the current and last input sample increases, so INL errors occur due to this effect occur for codes further away from the ADSC thresholds. When the memory effect is extended to all stages, Fig. 6(c) shows the resulting converter INL of ± 5.3 LSBs. This slight increase shows that the memory error in this case is dominated by the second stage. The INL in this case can also be seen to vary slightly with the input frequency.

4 Conclusion

Sources of memory effects in pipelined ADCs due to capacitor dielectric absorption/relaxation, incomplete stage reset, and op amp sharing have been described and modeled. While errors due to incomplete stage reset can be reduced by decreasing the ADC conversion rate $f_s = 1/T$, the other effects described are independent of f_s.

These memory effects can limit the ADC linearity. However, for common cases, memory effects in the SHA and first pipeline stage do not cause ADC nonlinearity. This allows some flexibility of the design of these stages, which typically dominate the power and area of a pipelined ADC due to noise considerations.

Acknowledgements

This research was supported by UC MICRO Grant No. 03-051 and by NSF Grant No. CCR-9901925

References

[1] A. N. Karanicolas, H.-S. Lee, and K. L. Barcrania, A 15-b 1-Msample/s digitally self-calibrated pipeline ADC, *IEEE Journal of Solid-State Circuits*, 1993, *28*(12), 1207–15.

[2] J. Ming and S. H. Lewis, An 8-bit 80-Msample/s pipelined analog-to-digital converter with background calibration, *IEEE Journal of Solid-State Circuits*, 2001, *36*(10), 1489–1497.

[3] J. W. Fattaruso, M. de Wit, G. Warwar, K-S. Tan, and R. K. Hester, The effect of dielectric relaxation on charge-redistribution A/D converters, *IEEE Journal of Solid-State Circuits*, 1990, *25*(6), 1550–1561.

[4] A. Zanchi, F. Tsay, and I. Papantonopoulos, Impact of capacitor dielectric relaxation on a 14-bit 70-MS/s pipeline ADC in 3-V BiCMOS, *IEEE Journal of Solid-State Circuits*, 2003, *38*(12), 2077–2086.

[5] H. Reisinger, G. Steinlesberger, S. Jakschik, M. Gutsche, T. Hecht, M. Leonhard, U. Schroder, H. Seidl, and D. Schumann, A comparative study of dielectric relaxation losses in alternative dielectrics, *Int. Electron Devices Mtg. Tech. Dig.*, Washington, D.C., USA, 2001, 267–270.

[6] S. H. Lewis, H. S. Fetterman, G. F. Gross Jr, R. Ramachandran, and T. R. Viswanathan, A 10-b 20-Msample/s analog-to-digital converter, *IEEE Journal of Solid-State Circuits*, 1992, *27*(3), 351–358.

[7] K. Nagaraj, H. S. Fetterman, J. Anidjar, S. H. Lewis, and R. G. Renninger, A 250-mW, 8-b, 52-Msamples/s parallel-pipelined A/D converter with reduced number of amplifiers, *IEEE Journal of Solid-State Circuits*, 1997, *32*(3), 312–320.