A Second-Order Double-Sampled Delta-Sigma Modulator using Individual-Level Averaging †

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Abstract

A second-order double-sampled delta-sigma modulator is described. It uses an individual-level-averaging switching scheme to convert capacitor mismatch into high-pass noise. With a sampling rate of 25 MHz and an oversampling ratio of 128, the maximum measured signal-to-noise-and-distortion ratio is 82.2 dB, and the total harmonic distortion is -91.0 dB when the input is 2.5 dB below full scale. The modulator is fully differential, occupies 3.75 mm^2 in a 1.2-μm CMOS process, and dissipates 25.9 mW (10.2 mW analog and 15.7 mW digital).

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I. Introduction

Double sampling is a technique that increases the maximum sample rate of switched-capacitor circuits without requiring faster operational amplifiers (op amps) or new process technologies [1]. The increase in sampling rate is achieved by interleaving two sampling capacitors in time. When straightforward double sampling is applied to delta-sigma modulators (ΔΣMs), however, a key limitation arises from mismatch in the sampling capacitors. The problem stems from the fact that the integrator(s) in switched-capacitor ΔΣMs accumulate charge provided by the sampling capacitors. If the capacitance of each sampling capacitor is constant, the charge provided by each sampling capacitor is proportional to its capacitance. Therefore, mismatch in the time-interleaved sampling capacitors causes amplitude modulation of the charge provided by the sampling capacitors. This modulation degrades the baseband signal-to-noise ratio (SNR) because some of the high-frequency noise in the feedback signal is mixed down to the baseband, where it adds to the noise floor.

Several solutions to this problem have been described but retain some sensitivity to capacitor mismatch [2, 3] or require additional clock phases [4]. Another solution that achieves low sensitivity to capacitor mismatch with only two main clock phases uses additive-error switching [5, 6] to convert the mismatch into an additive out-of-band tone. However, this approach requires three capacitors to be connected by switches to the summing node of each op amp during charge transfer. This connection reduces the feedback factor of each integrator and limits the increase in the sample rate to less than the ideal maximum of 100%.

To increase the feedback factor and therefore the sample rate, individual-level averaging (ILA) can be used. ILA is one of several dynamic-element-matching techniques [7-10] that have been shown to improve the linearity of ΔΣMs with multibit feedback. The use of ILA in a double-sampled ΔΣM increases the feedback factor around each integrator and simplifies the finite-state machine required for switch control compared to the additive-error algorithm. This paper describes a prototype second-order double-sampled ΔΣM using ILA [11] and is organized as follows. Section II describes the application of

ILA to double-sampled ΔΣMs. The prototype modulator is described in Section III. Section IV presents the experimental results.

II. Double Sampling and Individual-Level Averaging

Fig. 1 shows a schematic of a double-sampled first-order ΔΣM with individual-level averaging (ILA). It consists of a pair of switched sampling capacitors (C_{s_1} and C_{s_2}), a fixed integrating capacitor (C_i), an op amp, a latched comparator, a finite-state machine (FSM), and a digital-to-analog converter (DAC). To double sample the input, C_{s_1} and C_{s_2} simply alternate. During ϕ_1, C_{s_1} samples the input and C_{s_2} dumps charge onto C_i. During ϕ_2, C_{s_2} samples the input and C_{s_1} dumps charge onto C_i. If $C_{s_1} \neq C_{s_2}$, the change in the sampling capacitance from one phase to the next modulates the input. If the input is a low-frequency signal, the mismatch mixes V_i to a frequency band near $f_s/2$. Because signals in this frequency band are greatly attenuated by the digital low-pass filter that operates on the output of the ΔΣM, the effect of this mixing is of little consequence here. However, even for low-frequency inputs, the DAC output can have a large high-frequency content because the ΔΣM output contains high-pass-filtered quantization noise. To avoid modulation of the DAC feedback signal, capacitors C_{s_1} and C_{s_2} do not process the reference signal.

Fig. 2 shows a schematic of the DAC. Capacitors C_1–C_4 are controlled by FSM outputs w–z and their nonoverlapping complements $\overline{w}$–$\overline{z}$ to carry out the ILA algorithm. ILA is a dynamic element matching technique first proposed by Leung and Sutarja to overcome the effects of DAC nonlinearity in ΔΣMs using multibit feedback [7]. Here, ILA converts capacitor mismatch in a one-bit double-sampled DAC into high-pass noise.

ILA cycles the DAC elements on a per-level basis. All elements used to represent an individual digital code are exercised sequentially. No more than one of the four main control signals (w–z) is high at any given time. This means that no more than one of the four capacitors is connected to the op-amp input at any given time. When the ΔΣM output is high ($d = 1$), positive charge is delivered to the integrator by selecting either C_1 (w=1) or C_2 (x=1) and switching the left side of the selected capacitor from ground to V_r. Similarly, when $d = 0$, negative charge is delivered to the integrator by selecting either C_3 or C_4 and switching the left side of the selected capacitor from V_r to ground. If d is constant, one pair ($\{C_1, C_2\}$, or $\{C_3, C_4\}$) is used and the capacitor selected within that pair alternates. For example, if $d = 1$ and is constant, C_1 and C_2 alternate. Similarly, C_3 and C_4 alternate if $d = 0$ and is constant. On the other hand, when d alternates, both pairs are used alternately and the capacitor selected within each pair is the one not most recently selected.

Although $C_1 = C_2 = C_3 = C_4$ under ideal conditions, mismatches are unavoidable in practice. Define $C_t = (C_1 + C_2)/2$, $\Delta C_t = C_1 - C_2$, $C_b = (C_3 + C_4)/2$, and $\Delta C_b = C_3 - C_4$. Then

$$C_1 = C_t + \Delta C_t/2, \tag{1}$$
$$C_2 = C_t - \Delta C_t/2, \tag{2}$$
$$C_3 = C_b + \Delta C_b/2, \text{ and} \tag{3}$$
$$C_4 = C_b - \Delta C_b/2. \tag{4}$$

First, suppose $C_t \neq C_b$. Since C_1 and C_2 are used to deliver positive charge to the integrator, a change in their average value is equivalent to a change in the positive full-scale reference. Similarly, a change in the average of C_3 and C_4 is equivalent to a change in the negative full-scale reference. Therefore $C_t \neq C_b$ causes gain and/or offset errors in the modulator. ILA does not correct these errors, but offset and gain errors are not key limitations in many applications. Second, suppose $\Delta C_t \neq 0$ and/or $\Delta C_b \neq 0$. These conditions generate an additive DAC error sequence that is determined by the ΔΣM output sequence $d(k)$, where k is a time index. The problem of finding the spectrum arising from such capacitor mismatch is similar to finding the spectrum of a line code known as Alternate Mark Inversion (AMI).

Fig. 3(a) shows an AMI coder. It consists of an exclusive-or gate, a delay cell, and a subtracter. AMI is a line code that converts a set of source bits $b(k)$ (where k is a time index) into another set of transmitted symbols $a(k)$. It is used in the phone companies' T1-carrier system to produce a spectral null at d.c. and concentrate the transmitted power spectrum at frequencies where the connecting cable has low loss. Fig. 3(b) shows the corresponding truth table. Note that $b(k)$=0 at the input is always encoded to

$a(k)$=0 at the output. On the other hand, $b(k)$=1 is encoded to either $a(k) = \pm 1$, depending on the value of the previous output of the exclusive-or gate $c(k-1)$. If $b(k) = 1$ and is constant, $a(k)$ alternates between ± 1.

Analysis of the AMI coder is difficult due to the nonlinearity in the exclusive-or gate. Analysis is possible when the input sequence $b(k)$ is independent, which is assumed below. To find the power spectrum of the output $S_a(e^{j\omega T})$ (where T is the bit period), let p represent the probability that $b(k) = 1$ and find the autocorrelation function of the output $a(k)$ using a Markov model. The power spectral density is the z-transform of the autocorrelation function evaluated on the unit circle (where $z = e^{j\omega T}$). Fig. 3(c) shows the result [12]. The power is concentrated at half the clock rate, $f_s/2$. As p increases, the peak at $f_s/2$ increases because the fraction of outputs that alternate between ± 1 increases. The spectrum is null at d.c. because the back end of the AMI coder is a first-order difference $(1 - z^{-1})$, which produces a zero at $z = 1$.

Fig. 4 shows two copies of the AMI coder. The input to the top coder is the $\Delta\Sigma$M output $d(k)$, and the input to the bottom coder is $\bar{d}(k)$. The outputs of the two AMI coders, $a_t(k)$ and $a_b(k)$, are scaled and summed to produce $y(k)$, which represents the charge error contributed by $\Delta C_t \neq 0$ and $\Delta C_b \neq 0$. Since the inputs of the two coders are complementary, either $a_t(k) = 0$ or $a_b(k) = 0$ for each k. Therefore, only one coder at a time contributes to $y(k)$. When $d = 1$ and is constant, a_t alternates between ± 1. After scaling a_t, y corresponds to the error that arises from mismatch when C_1 or C_2 is selected to deliver the feedback in the $\Delta\Sigma$M. On the other hand, when $d = 0$ and is constant, a_b alternates between ± 1. After scaling a_b, y corresponds to the error that arises from mismatch when C_3 or C_4 is selected. Analysis of a four-state Markov model shows that the states of the two coders are uncorrelated even though the inputs are correlated [13]. The resulting power spectral density $S_y(e^{j\omega T})$ is:

$$S_y(e^{j\omega T}) = \frac{2p(1-p)(1-cos\,\omega T)\delta_t^2}{1+(1-2p)^2-2(1-2p)\cos\omega T} + \frac{2p(1-p)(1-cos\,\omega T)\delta_b^2}{1+(1-2p)^2+2(1-2p)\cos\omega T}, \tag{5}$$

where $\delta_t = V_r \Delta C_t/2$ and $\delta_b = V_r \Delta C_b/2$ [13]. The $1-cos\,\omega T$ terms in Equation (5) cause the power spectrum to have a high-pass characteristic. This characteristic stems from the $1 - z^{-1}$ operations in each coder, which can be pushed to the output of the Fig. 4 because the back end of each AMI coder is linear. The analysis when the input sequence is independent is useful in giving some insight into the ILA algorithm. Simulations show that the DAC error has a high-pass frequency response even when the input sequence to the coder is correlated and equals the DSM output.

The ILA switching scheme was explained above using a first-order ΔΣM for simplicity, but it can be applied to higher-order loops. Fig. 5 shows a block diagram of the second-order prototype. It consists of two double-sampled integrators contained in dashed boxes, a latched comparator, and a finite-state machine (FSM). The two integrators are identical, and each is built with three pairs of capacitors to implement ILA as shown in Figures 1 and 2. The capacitor values are given in Table 1. In both integrators, C_1–C_4 are controlled by the FSM and the C_s capacitors simply alternate. The use of identical integrators simplified the design and layout of the ΔΣM. The mismatch of the C_s capacitors in the second integrator mixes high frequencies at the output of the first integrator to the baseband. However, little high-frequency energy exists there due to the low-pass action of the first integrator, and any signals mixed to the baseband after the first integrator are reduced by the gain of the first integrator when referred to the input of the ΔΣM. Therefore mismatch of these capacitors is not a limitation.

On each clock phase, one capacitor from $\{C_{s_1} – C_{s_2}\}$ and one from $\{C_1 – C_4\}$ is switched to the input of each op amp. An advantage of this approach is that it makes the performance of the prototype insensitive to offset and finite open-loop gain errors in the op amps [6]. Another advantage of this approach is that it requires only two capacitors to be switched to each op-amp input at a time. In contrast, three capacitors are switched to each op-amp input during charge transfer using the additive-error algorithm to give it similar sensitivity properties [6]. A simplified analysis of the resulting feedback factor around each op amp shows that the speed of the ΔΣM with ILA is 13% faster than with additive-error switching [13].

III. Prototype

To increase the noise immunity, dynamic range and power supply rejection, and to reduce the even-order harmonic distortion, the entire prototype is fully differential. Two identical op amps are used. To provide both high gain and fast settling, both op amps have a telescopic cascode structure [14]. Common-mode feedback is provided through two time-interleaved switched-capacitor sense circuits [15]. To limit the baseband error penalty caused by finite op-amp gain to about 1 dB, the open-loop gain of the op amp should be more than the oversampling ratio, which is 128. According to simulation, the op-amp gain is about 600 and the settling time to 0.05% accuracy is less than 15 ns.

Although comparator offset has little effect on modulator performance, the comparator must be fast here because it makes a decision each sample period. Therefore, a simple latch-based comparator was used [16].

Fig. 6 shows a gate-level diagram of the FSM. It is included on the prototype along with circuits that make the control signals and their complements nonoverlapping. All capacitors are switched using bottom-plate sampling techniques [17].

IV. Experimental Results

The ΔΣM was tested by applying a low-distortion sine wave, capturing the 1-bit digital output and post-processing the output on a workstation. Fig. 7 shows the spectrum of the modulator output for a 760-Hz input that is 2.5 dB below full scale and sampled at 25 MHz. Fig. 8 shows a plot of SNDR versus input level for the prototype. The oversampling ratio was 128, the sampling rate was 25 MHz, and the input frequency was 760 Hz. For simplicity, a sinc^3 decimation filter was implemented in software to filter the output of the prototype, and the SNDR was found using the sinusoidal-minimum-error approach [18]. The peak SNDR is 82.2 dB, which is 6.7 dB less than predicted by circuit-noise calculations and simulations. The reason for this difference is unknown but could be caused by measurement limitations and/or a slew-rate limitation in the op amp for example.

Table 2 shows that the performance of the ILA and the additive-error (AE) prototypes [6] is similar except that the ILA prototype in a 1.2-μm technology is five times faster than the AE prototype in a 2-μm technology. According to simulation, the op amps were about three times faster in the 1.2-μm process than in the 2-μm process. Although the oversampling ratio (OSR) is 256 for most of the data shown in [6], Table 2 uses an OSR=128 for both modulators.

Fig. 9 shows plots of the peak SNDR versus oversampling ratio (OSR) for both modulators. When the OSR < 64, the peak SNDR rises at 15 dB per octave in both plots, which means that quantization noise is dominant. When the OSR > 64, however, the slopes of both plots are reduced, which shows that quantization noise is no longer dominant.

The SNDR of a double-sampled ΔΣM using ILA is insensitive to mismatch that causes $\Delta C_t \neq 0$ and/or $\Delta C_b \neq 0$. One way to demonstrate this property is to build a programmable capacitor mismatch directly into the prototype. A simpler approach, however, is to use identically drawn capacitors and to connect them to different reference voltage inputs. For the test results presented above, the reference voltage inputs are connected together. To induce mismatch, these reference inputs are connected separately to reference voltages with different values. This connection induces a charge mismatch that is equivalent to that obtained with one reference and mismatched capacitors.

Fig. 10 shows a plot of peak SNDR versus mismatch in the reference voltages connected to C_1 and C_2. For mismatches less than 10%, the variation in the peak SNDR is less than about 3 dB. For mismatches greater than 10%, the SNDR in Fig. 10 decreases rapidly because the noise generated from mismatch becomes the dominant noise source. In contrast, the additive-error prototype exhibits only about 3-dB drop in peak SNDR for mismatches up to 100% [6]. The greater insensitivity to mismatch there results from the conversion of mismatch into an additive out-of-band tone, which is almost completely removed by a digital filter. (The mismatch here is converted into high-pass noise, and some of this noise falls into the baseband.) For the capacitor mismatch expected in practice (less than 1%), however, the performance of the two prototypes is similar.

Fig. 11 shows a photograph of the modulator. The chip is 1.9 mm by 1.9 mm (including the pads) and was made in a 1.2-μm, n-well, double-polysilicon CMOS process.

Acknowledgment

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TABLE AND FIGURE CAPTIONS

TABLE 1
Element and signal values for Fig. 5.

$C_{s_1} = C_{s_2}$	0.5 pF
$C_1 = C_2$	0.25 pF
$C_3 = C_4$	0.25 pF
C_i	1 pF
NMOS Switches	W/L = 12 µm/1.2 µm
PMOS Switches	W/L = 12 µm/1.2 µm
Amplitude of Clocks	5 V
V_r	2 V

TABLE 2
Typical Performance (5 V and 25°C)

	ILA	AE
Technology (CMOS)	1.2-µm	2-µm
Area (mm^2)	3.75	5
Power Dissipation (mW)	25.9	13
Sampling Rate (Msamp/s)	25	5
Oversampling Ratio	128	128
Full Scale (V)	4	4
Dynamic Range (dB)	82.4	82.3
Maximum SNDR (dB)	82.2	84.0
THD (dB)	-91.0	-88.8
PSRR (dB)	59	53
CMRR (dB)	68	63

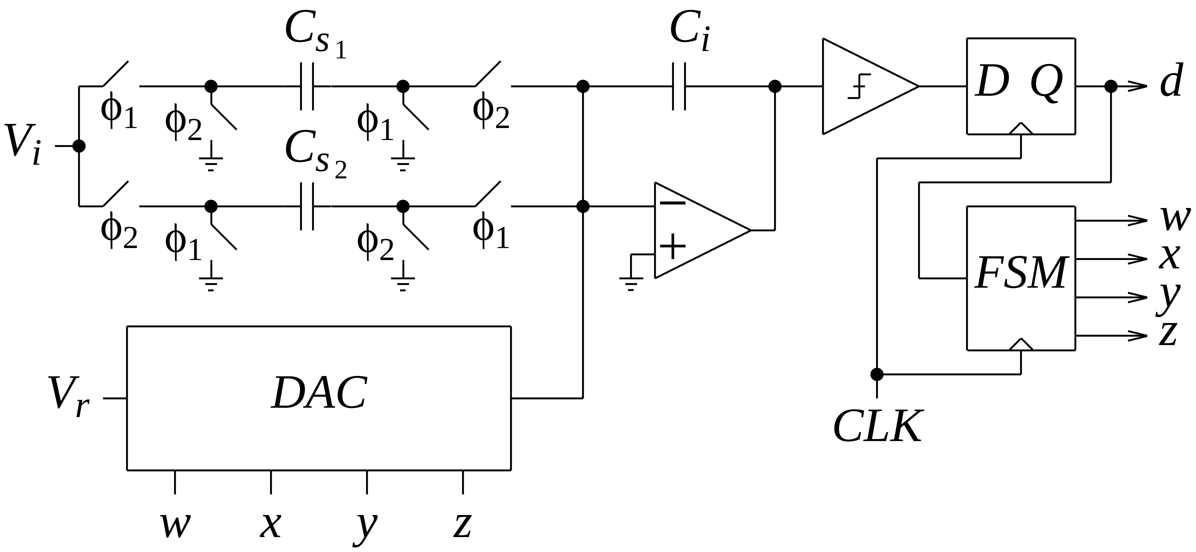


Fig. 1: A first-order double-sampled ΔΣM using individual-level averaging.

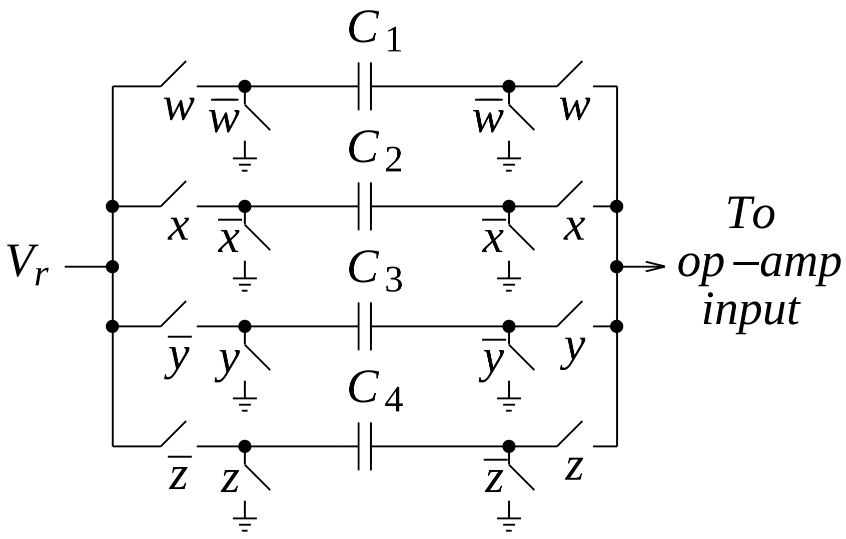
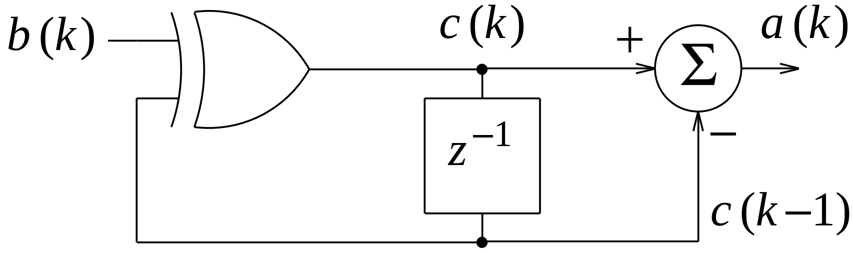


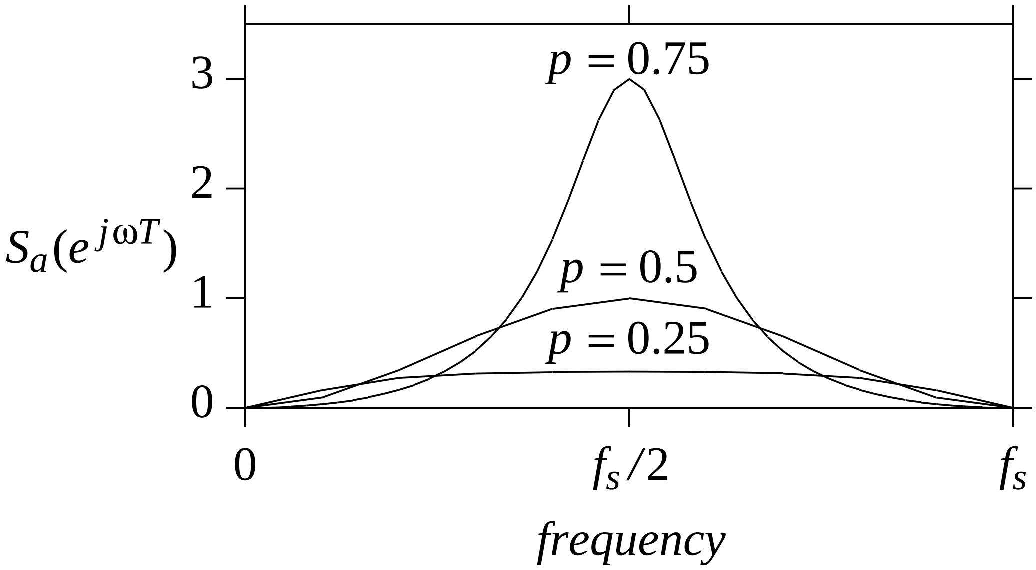
Fig. 2: The individual-level averaging DAC.



(a)

$b(k)$	$c(k-1)$	$c(k)$	$a(k)$
0	0	0	0
0	1	1	0
1	0	1	1
1	1	0	−1

(b)



(c)

Fig. 3: Alternate mark inversion a) coder, b) truth table, c) power spectral density

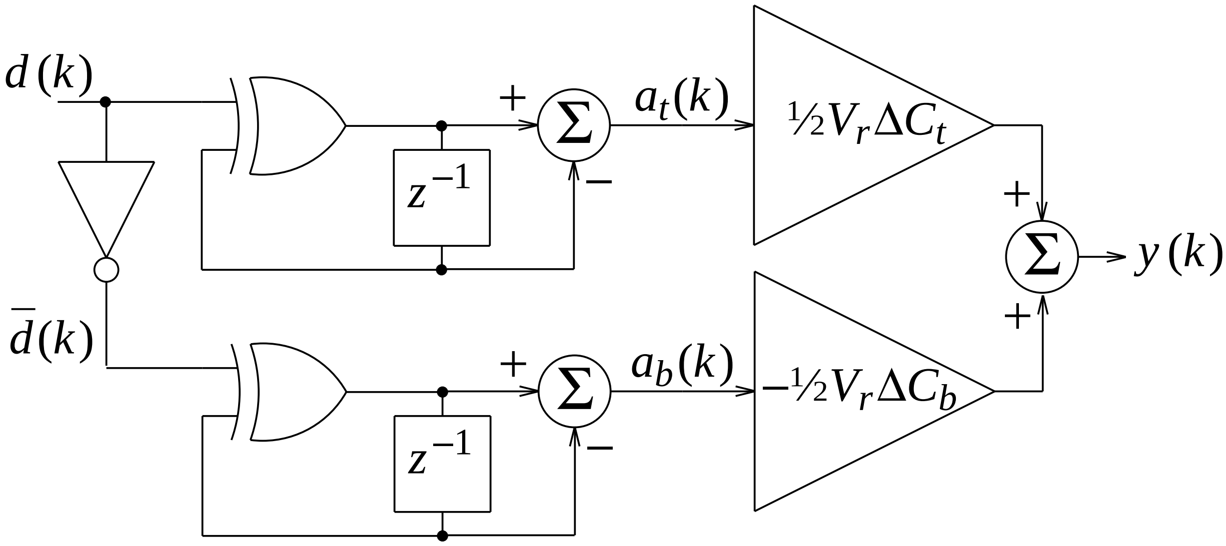


Fig. 4: Alternate mark inversion model of individual-level-averaging error.

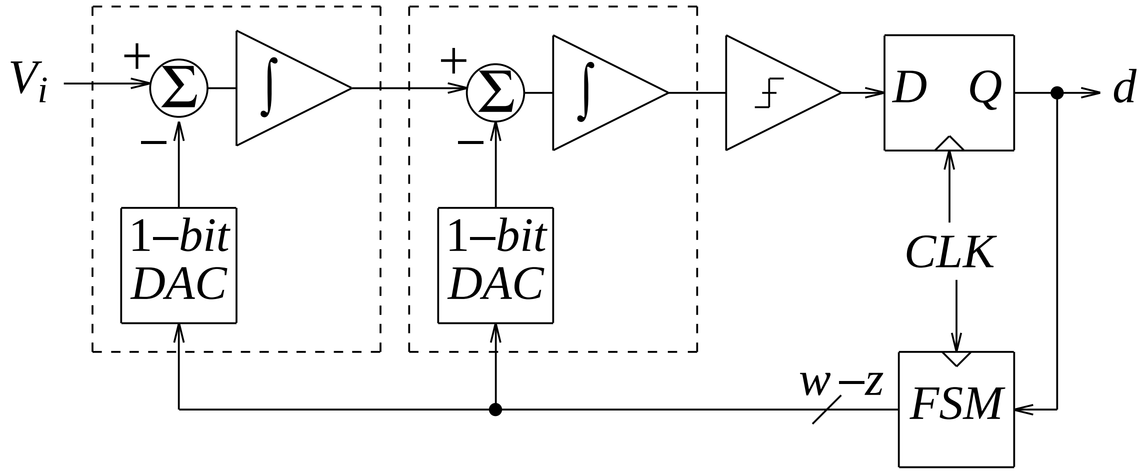


Fig. 5: A second-order double sampled ΔΣM using individual-level averaging.

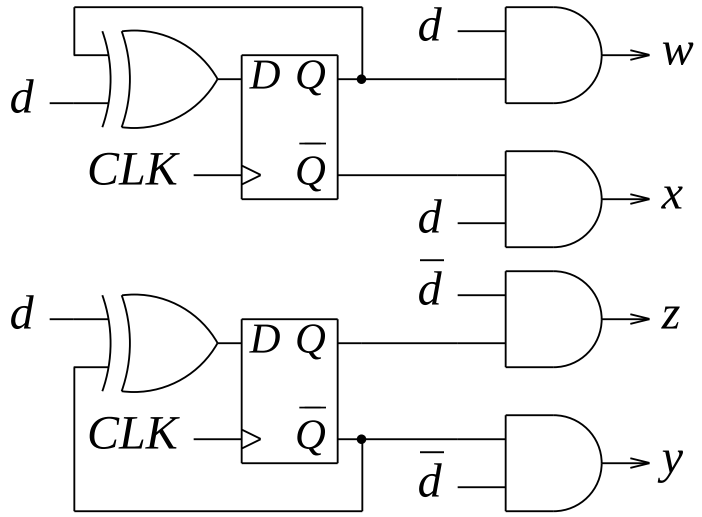
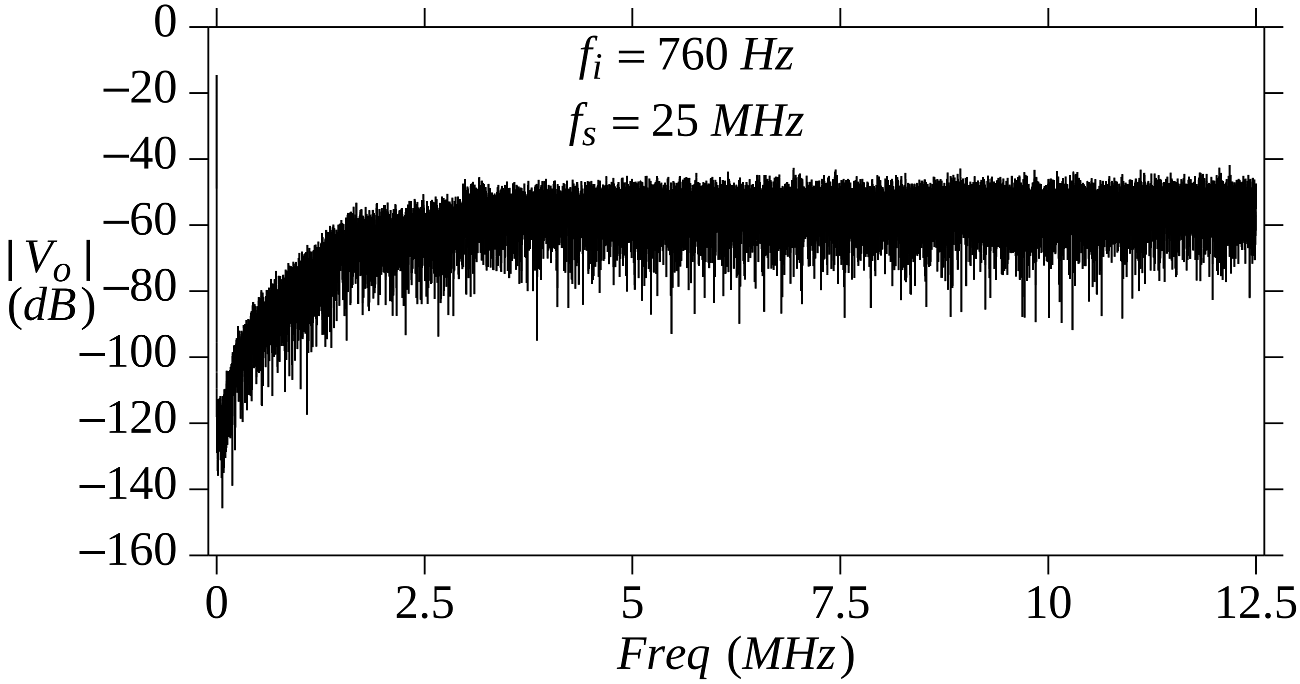
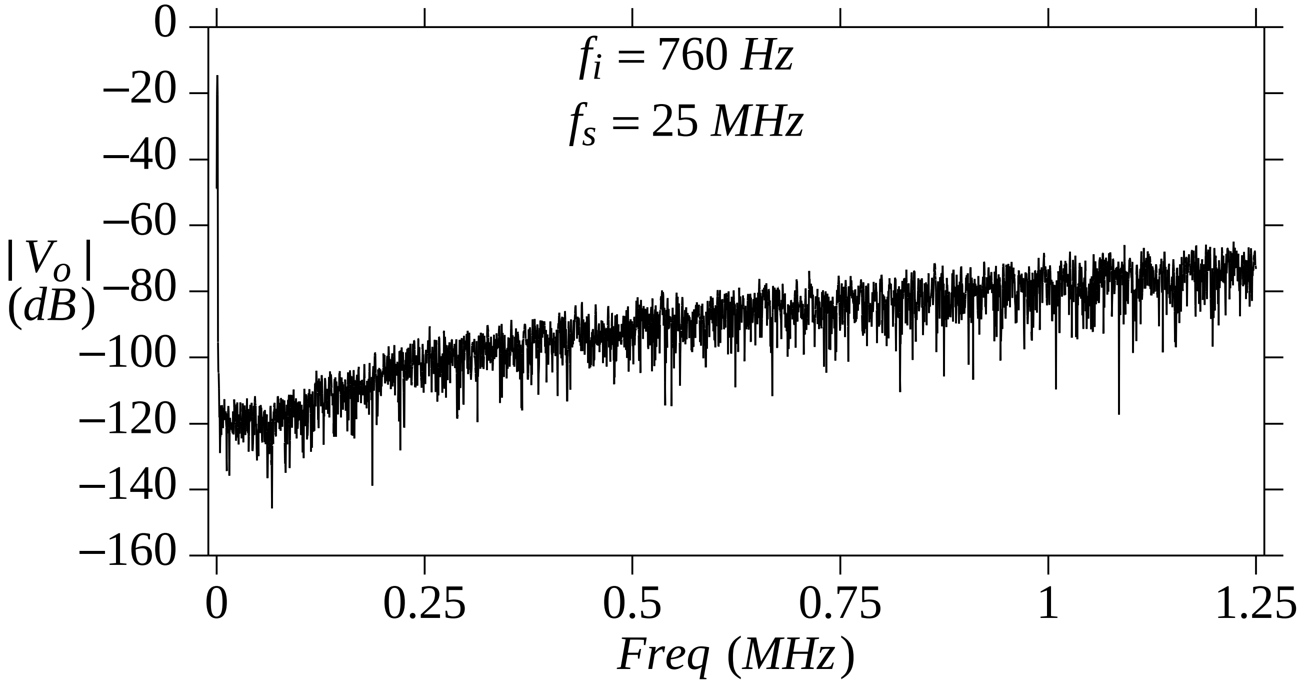


Fig. 6: Finite state machine.



(a)



(b)

Fig. 7: Measured output spectrum: (a) from zero to $f_s/2$ and (b) from zero to $f_s/20$

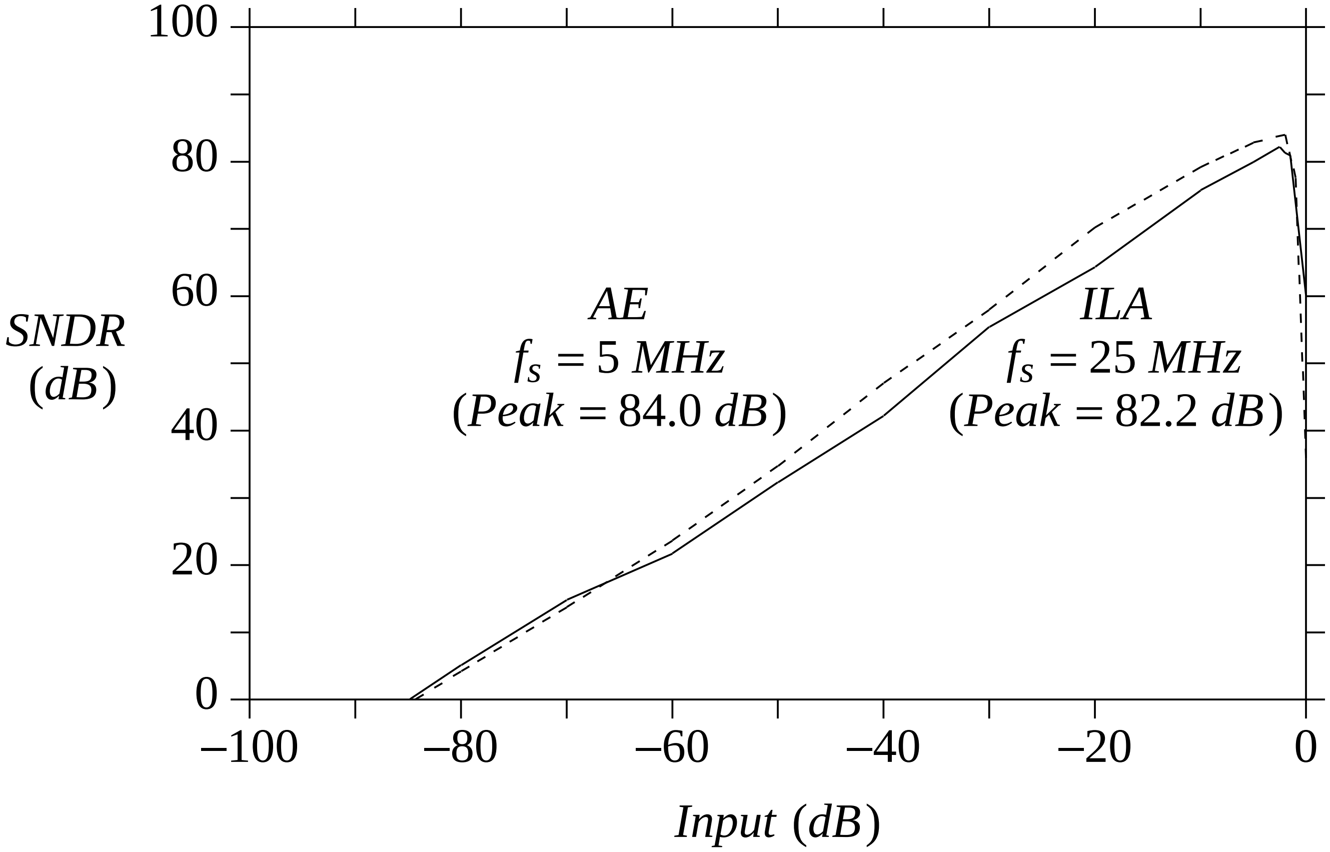


Fig. 8: SNDR vs. input amplitude.

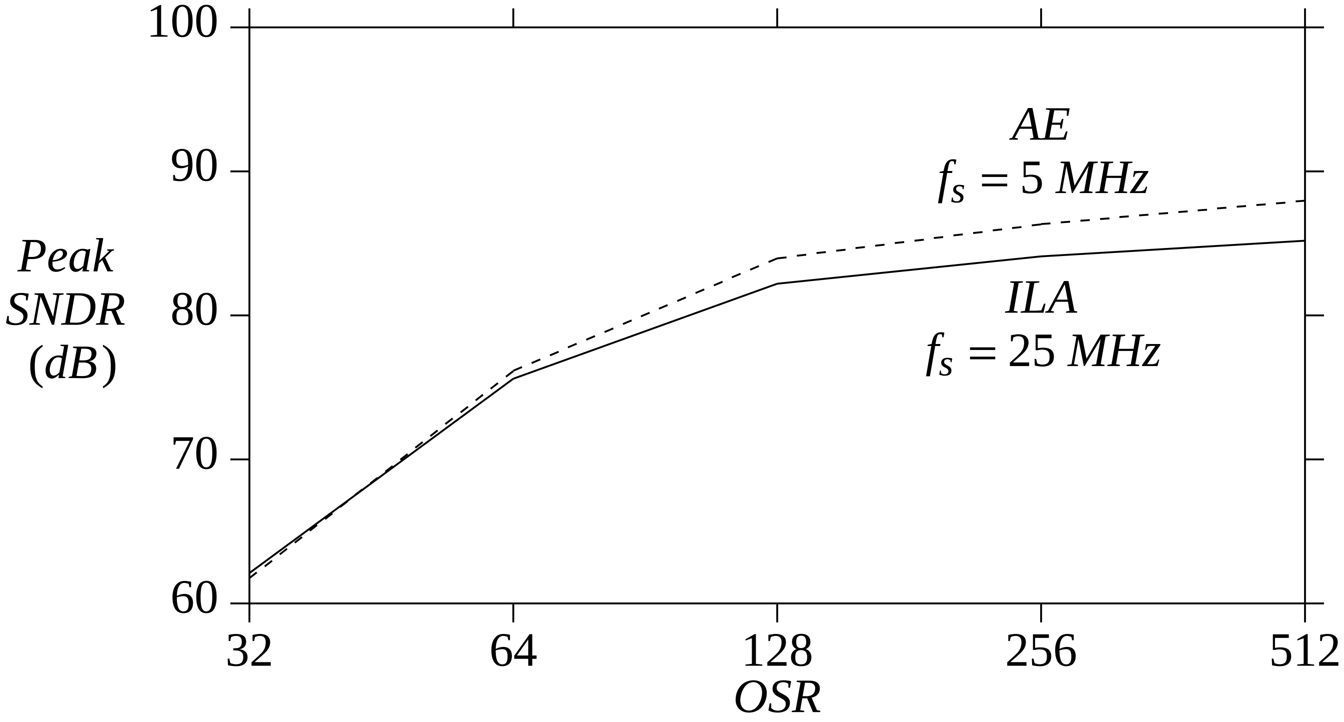


Fig. 9: Peak SNDR vs. oversampling ratio

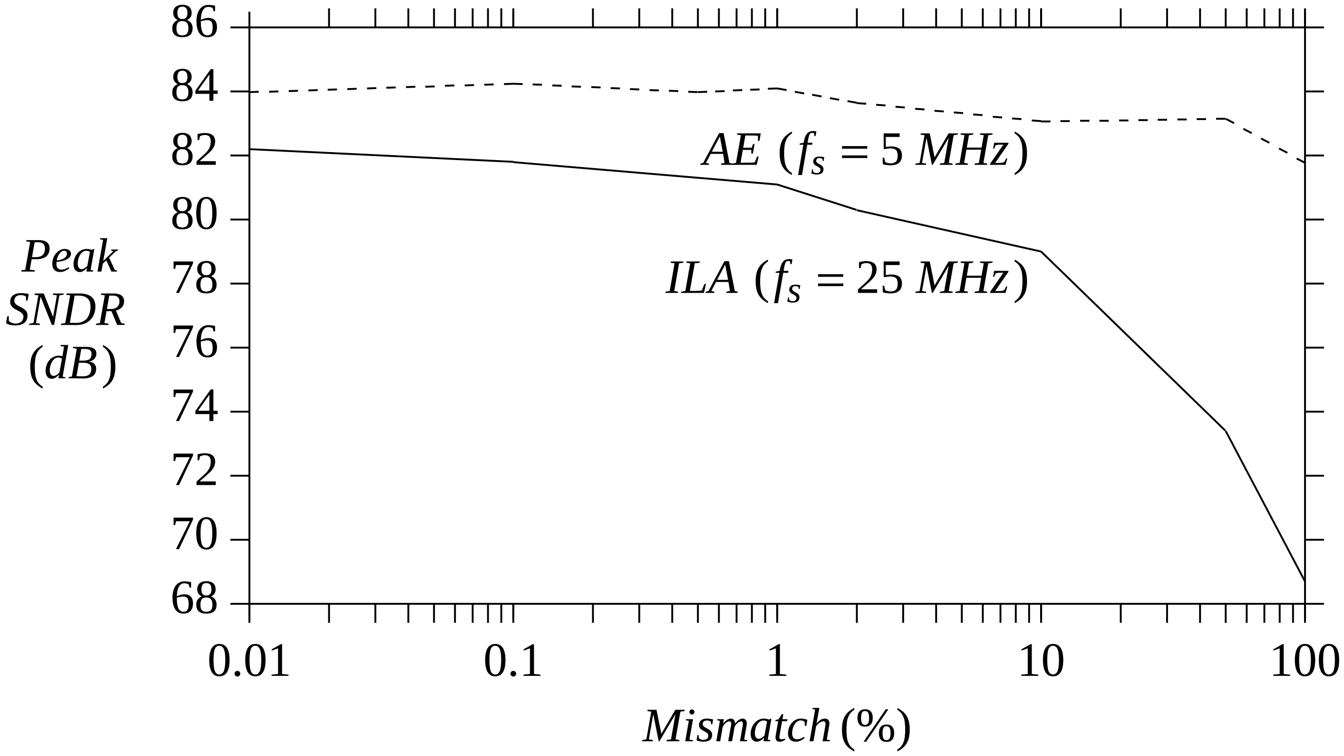


Fig. 10: SNDR vs. reference voltage mismatch.

Fig. 11: Die photograph.