An 80Mb/s Adaptive DFE Detector in 1μm CMOS*

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Intersymbol interference (ISI) and channel noise limit the recording density and the bit-error rate (BER) in hard-disk drives. To increase the recording density, sampling detectors are being used in the read channels of such drives, replacing peak detectors. In particular, partial-response maximum-likelihood (PRML) sampling detectors are now in production. However, recent work has shown that, in some cases, detectors using decision feedback equalizers (DFEs) perform better than PRML detectors [1],[2].

A DFE-based read channel uses adaptive forward and feedback equalizers to cancel precursor and postcursor ISI, respectively. Fixed right- and left-half-plane zeros have been used previously to reduce all ISI [3]. This paper describes a continuous-time forward equalizer (CTFE) with one adaptive right-half-plane zero that removes the precursor ISI and an adaptive RAM DFE that removes the postcursor ISI. Because the DFE cancels postcursor ISI noiselessly, the postcursor ISI cancellation does not degrade the signal-to-noise ratio. The prototype also includes a 7th-order linear-phase low-pass ladder filter to provide anti-aliasing and to suppress channel noise. The key contribution here is the implementation of this adaptive one-zero forward equalizer in conjunction with the low-pass filter and adaptive mixed-signal RAM-DFE on the same IC. Because two continuous-time outputs from the low-pass filter are combined to build the core of the adaptive forward equalizer, it is constructed with little hardware beyond that already required for the low-pass filter.

Figure 1 shows a block diagram of the prototype, which consists of a low-pass filter, a forward equalizer, and a DFE. The analog signal paths are indicated by thin lines and are fully differential. The output from the forward equalizer is fed to the DFE, which samples its input at the bit times *kT.*

The readback waveform from a step change in the magnetic field on a disk drive has the same shape as its own derivative in the region of significant precursor ISI. By subtracting a scaled derivative of the read signal from the read signal itself, the forward equalizer greatly reduces the precursor ISI at the sample times *kT.* Figure 2 shows a block diagram of the low-pass filter and forward equalizer. The filter produces two outputs: a low-pass output, x(t), and its derivative, x′(t). The forward equalizer adds an adaptively weighted version of the derivative to the low-pass output to cancel precursor ISI. Therefore, this forward equalizer has one adaptive zero. The forward equalizer is made adaptive by using two slicers, two digital multipliers, two 10b digital integrators, two 6b DACs, and two analog multipliers. The multiplier coefficients α_0 and α_1 are adapted each bit period using sign(x) and sign(x′) with a 3b error signal in the least-mean-squared (LMS) update equations.

The analog multipliers used in the forward equalizer are MOS versions of the Gilbert cell [4]. They multiply the analog coefficients from the two 6b DACs by the analog outputs from the low-pass filter and produce current outputs. These currents are summed and converted to a voltage to form the output of the forward equalizer. The low-pass filter in Figure 3 is a 7th-order 0.05° equiripple phase Gm-C filter with an adjustable cutoff frequency of 33-57MHz. A singly terminated ladder filter provides the low-pass output as well as its derivative. All the Gm cells are identical, except that a bold 2 in a cell indicates that two Gm cells are connected in parallel. The Gm-C filter uses the two-input transconductance cell shown in Figure 4. By adjusting the tail current of the n-channel differential pairs, each transconductor has a tuning range of 500μS to 1200μS. The output conductance of the transconductors is varied by adjusting the tail current of the p-channel pair MP1-2. The p-channel differential pair is connected to provide positive feedback and acts as a small-signal negative resistance to reduce output conductance. The bias voltages Gm-bias and Go-bias are connected off chip to allow evaluation of detector performance versus transconductance and output conductance.

To cancel postcursor ISI, the prototype also includes a 4-tap RAM-DFE shown in Figure 5 [5]. The RAM-DFE samples the output of the forward equalizer, adds a postcursor ISI cancellation value that is stored in the RAM and converted to analog form by a 6b DAC, and uses a nonuniform flash ADC to produce the binary decision and a 3b error signal. The RAM-DFE has the capability to cancel nonlinear as well as linear postcursor ISI [1]. The values stored in the RAM are adapted using the LMS algorithm with the 3b error signal. With a 4-tap RAM-DFE, simulations show that a one-zero CTFE performs as well as, and is simpler than, a 5-tap FIR forward equalizer.

A plot of bit-error rate (BER) versus input signal-to-noise ratio (SNR) is shown in Figure 6 for an 80Mb/s data rate. A Lorentzian channel model was used here. The data were gathered by adapting the equalizer and measuring the BER after the coefficients reached their steady-state values. The adaption was active during the BER measurements. For comparison, simulated BER performance of the equalizer is also plotted. The simulated results do not include error propagation effects because the BER is computed from a simulated minimum mean-square error. With $PW_{50} = 2T$, measured performance is within 0.8 dB of the simulated performance for channel SNRs ≤ 18dB. And with $PW_{50} = 2.5T$, measured performance is within 1.0dB of the simulated performance for channel SNRs ≤ 21dB. Allowing 0.2dB for error propagation [1], the losses from implementation are 0.6dB and 0.8dB, respectively. The DFE detector also performed well when the read signal was constructed from a measured disk-drive step response.

The die photo is shown in Figure 7. The IC was fabricated in a single-poly 1μm CMOS process. The active area of the IC is 11.2mm^2. Measured performance is summarized in Table 1.

[1] P. Bednarz, N. P. Sands, C. S. Modlin, S. C. Lin, I. Lee, and J. M. Cioffi, "Performance evaluation of an adaptive RAM-DFE read channel," *IEEE Transactions on Magnetics*, vol. 31, no. 2, pp. 1121-1127, March 1995.

[2] K. Han and R. Spencer, "Comparison of different detection techniques for digital magnetic recording channels," *IEEE Trans. on Magnetics,* vol. 31, no. 2, pp. 1128-1133, March 1995.

[3] R. G. Schneider, "An improved pulse-slimming method for magnetic recording," *IEEE Trans. on Mag.,* vol. Mag-11, no.5, Sept. 1975.

[4] B. Gilbert, "A precise four-quadrant multiplier with subnanosecond response," *IEEE Journal of Solid-State Circuits*, Dec. 1968, vol. SC-3, no.4, pp. 365-73.

[5] B. C. Rothenberg, J. E. C. Brown, P. J. Hurst and S. H. Lewis, "A mixed-signal RAM decision-feedback equalizer for disk drives," *1996 Symposium on VLSI Circuits Digest of Technical Papers,* pp. 180-181.

Figure Captions

Figure 1: Block diagram of the read channel IC. Analog signals are denoted by thin lines and digital signals by thick lines.

Figure 2: Lowpass filter and forward equalizer architecture. Analog signals are denoted by thin lines and digital signals by thick lines.

Figure 3: 7th-order 0.05° equiripple phase singly terminated Gm-C ladder filter. A bold 2 indicates two Gm cells in parallel.

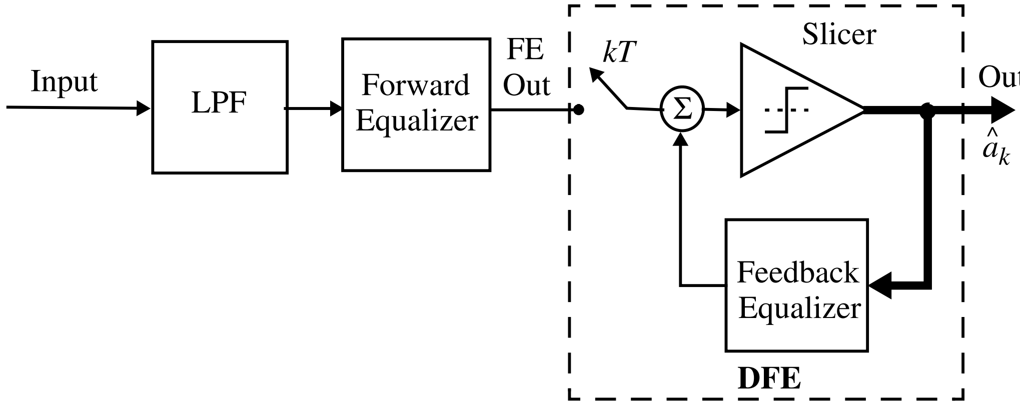
Figure 4: Two-input transconductance cell used in the lowpass filter.

Figure 5: RAM-DFE architecture.

Figure 6: BER performance of the read-channel IC @ 80Mb/s. Adaption enabled. Lorentzian channel.

Table 1: Performance summary at 80Mb/s. 5V supply, 25°C, and LPF -3dB freq. = 40MHz.

Figure 7: Die photo.



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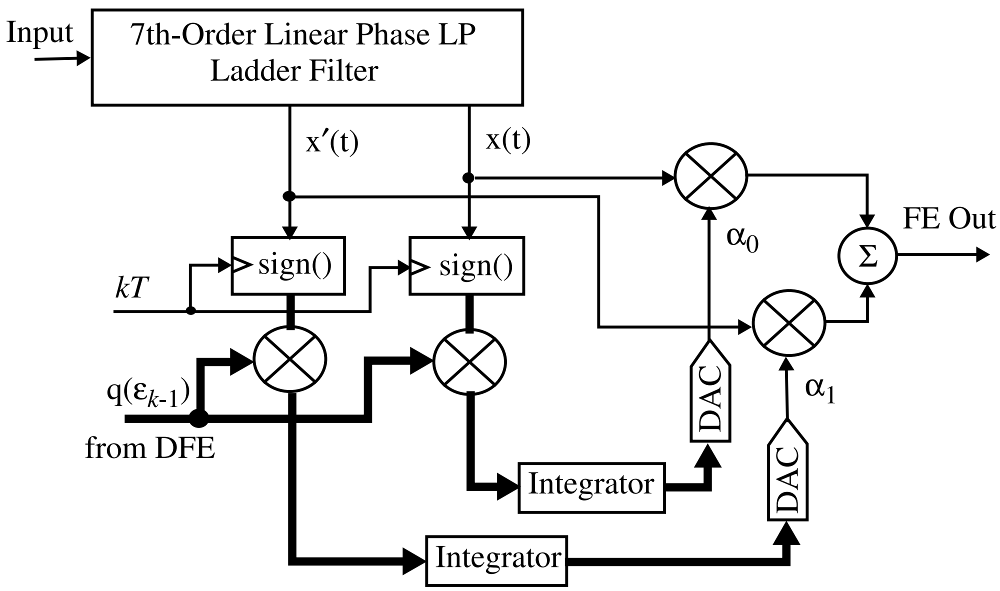

Figure 2: Lowpass filter and forward equalizer architecture. Analog signals are denoted by thin lines and digital signals by thick lines.

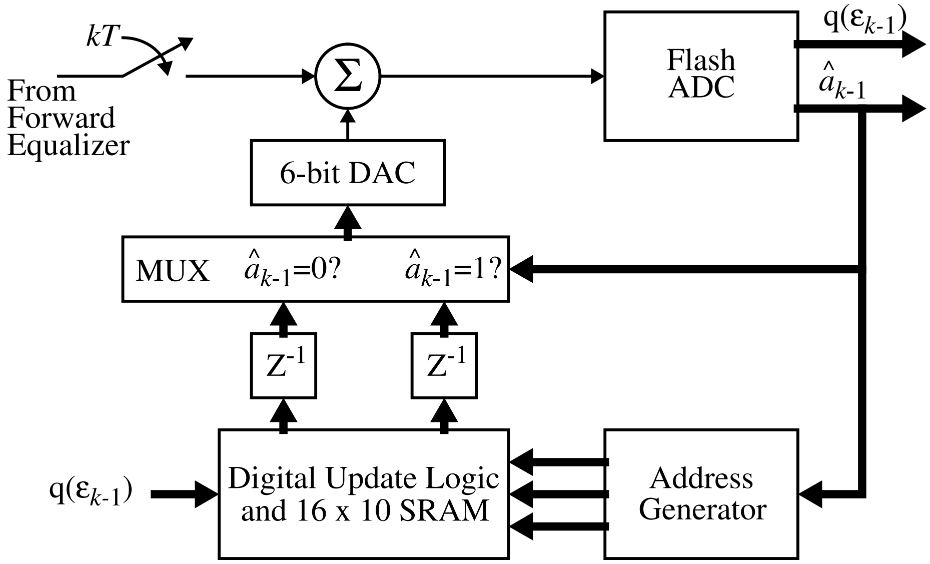

Figure 5: RAM-DFE architecture.

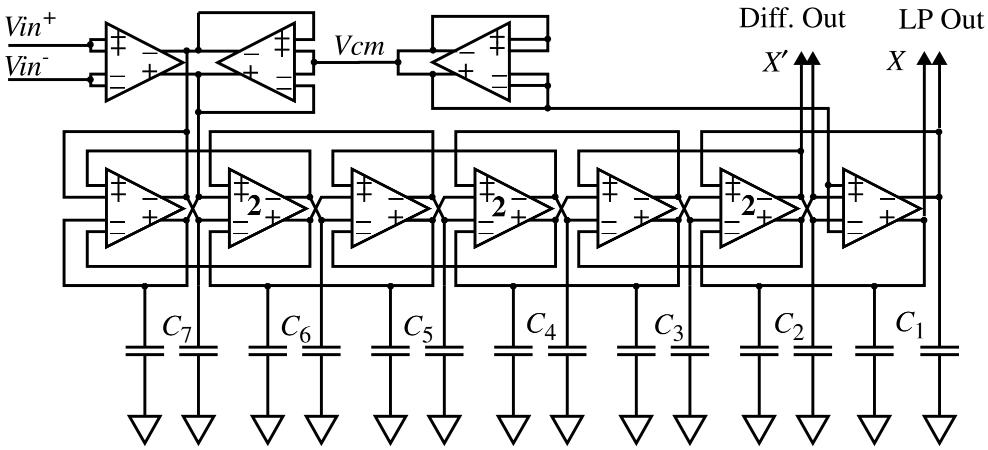

Figure 3: 7th-order 0.05° equiripple phase singly terminated Gm-C ladder filter. A bold 2 indicates two Gm cells in parallel.

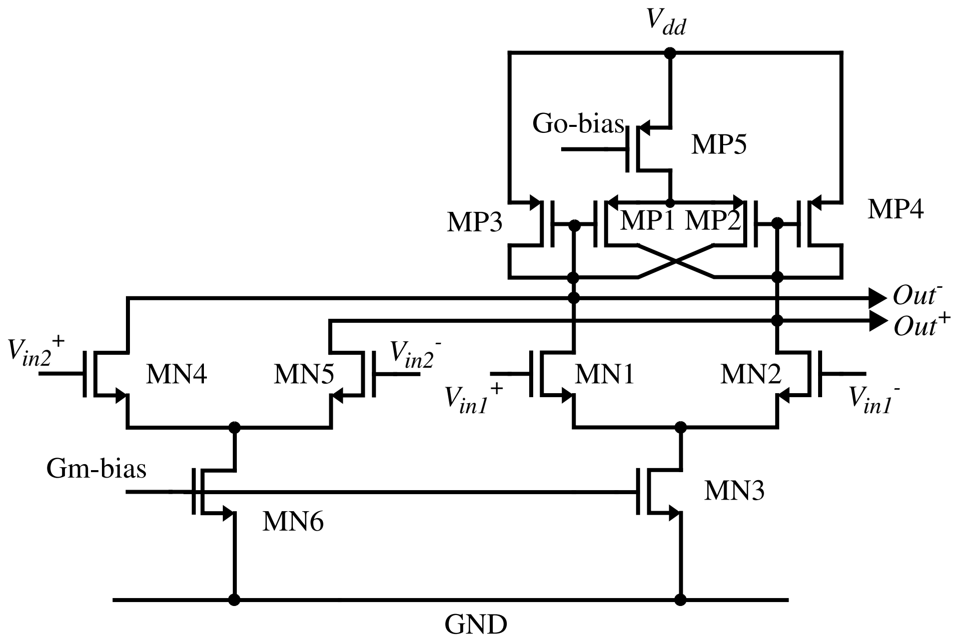

Figure 4: Two-input transconductance cell used in the lowpass filter.

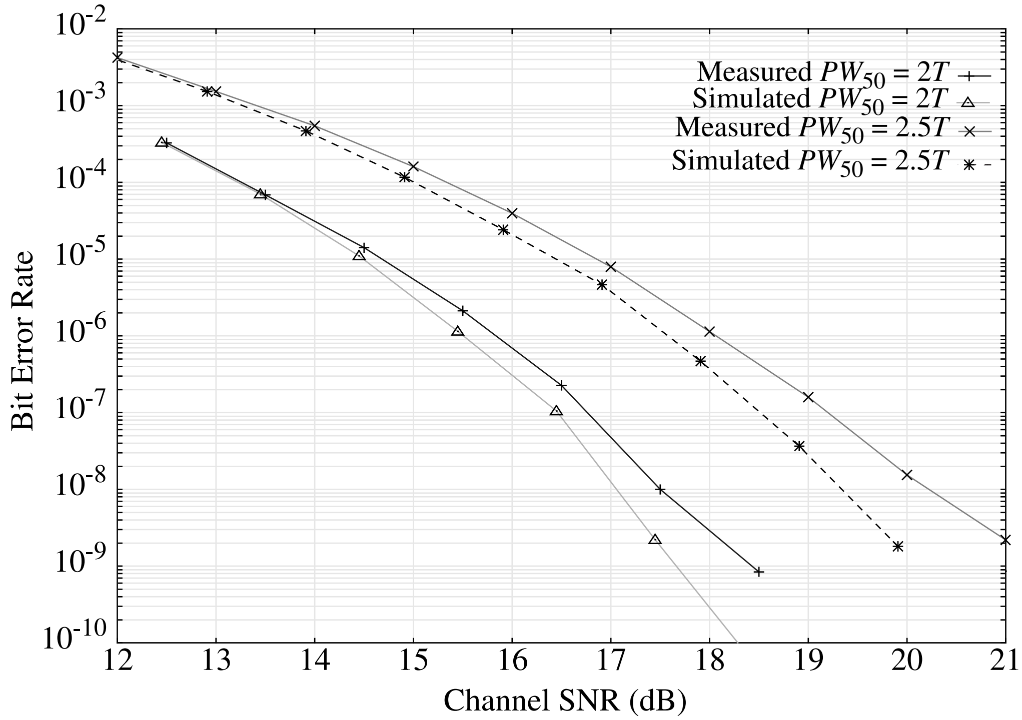

Figure 6: BER performance of the read-channel IC @ 80Mb/s. Adaption enabled. Lorentzian channel.

Process	1-µm CMOS
Total Active Area (RAM-DFE / LPF & CTFE)	$11.2mm^2$ ($4.5mm^2$ / $6.7mm^2$)
Total Power (RAM-DFE / LPF & CTFE)	630mW (350mW / 280mW)
Training Time	400 bit periods
RAM-DFE SRAM Size	16 x 10b
Full Scale Diff. Input Voltage	1Vpp
Forward Equalizer THD @ f_{in} = 10MHz	-37dB

Table 1: Performance summary at 80Mb/s. 5V supply, 25°C, and LPF -3dB freq. = 40MHz.

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