A Fully Differential Comparator Using a Switched-Capacitor Differencing Circuit with Common-Mode Rejection†

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Abstract

A fully differential comparator is described. It uses a switched-capacitor differencing circuit that provides common-mode rejection. The comparator has been tested by building a 3-bit flash analog-to-digital converter (ADC) in a 2-μm CMOS process. With a supply voltage of 3.3 V, a sampling rate of 25 MHz, and full-scale sinusoidal inputs up to 7 MHz, the signal-to-distortion ratio of the ADC when the input is single ended is about 1-2 dB less than when the input is differential. In a 2-μm CMOS process, the comparator occupies 0.25 mm^2 and dissipates 1.05 mW.

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I. Introduction

Fully differential circuit techniques have become common in many areas of analog circuit design. They are especially useful in rejecting common-mode noise in integrated circuits that do both analog and digital signal processing. In such circuits, comparators provide a link between the analog and digital domains. Fully differential comparators usually subtract a differential reference voltage from a differential input voltage (or vice versa). In CMOS technologies, the conventional approach used to generate such a difference is to sample the differential input onto a pair of sampling capacitors during one phase and switch the capacitors to the differential reference during the second phase of a two-phase nonoverlapping clock [1-9]. The output of this differencing circuit drives the preamplifier stage of a differential comparator. A key characteristic of this approach is that the output common-mode voltage is sensitive to differences in the common-mode components of the input and reference. These common-mode components are not necessarily equal or even constant. For example, the input common-mode voltage to the comparators in a fully differential flash analog-to-digital converter (ADC) may have a large time-varying component if a singled-ended signal and ground are connected to the ADC inputs. Changes in the common-mode output of the differencing circuit increase the required common-mode input range and common-mode rejection of the preamplifier that follows the differencing circuit. Therefore, the ability of comparators to reject such common-mode signals is sometimes important. This paper describes a fully differential comparator that uses a switched-capacitor differencing circuit to provide common-mode rejection.

This paper is organized as follows. Section II presents a switched-capacitor differencing circuit that provides common-mode rejection and acts as the input stage of a fully differential comparator. The prototype comparator is described in Section III. Section IV describes the experimental results.

II. Switched-Capacitor Differencing Circuit with Common-Mode Rejection

Fig. 1 shows a fully differential switched-capacitor differencing circuit that provides high common-mode rejection [10]. This configuration is adapted from a sample-and-hold amplifier described by Yen and Gray [11]. It uses a standard two-phase nonoverlapping clock. Capacitors C_{S1}-C_{S4} sample the references and inputs, and capacitors C_{L1} and C_{L2} represent the load, which is the input capacitance of the preamplifier. During ϕ_1, V_{i1} and V_{i2} are connected to C_{S2} and C_{S3}, and V_{r1} and V_{r2} are connected to C_{S4} and C_{S1}, respectively. During ϕ_2, the left sides of C_{S1} and C_{S4} are connected together as are the left sides of C_{S2} and C_{S3}.

This scheme forces the differential components of the input and reference to combine and appear in part on C_{L1} and C_{L2} during ϕ_2. The differential voltage across the left sides of C_{S2} and C_{S3} changes from V_{id} during ϕ_1 to zero during ϕ_2. This causes the differential output voltage to decrease by V_{id} attenuated not only by the load capacitors but also by the extra pair of sampling capacitors attached to the references. Similarly, the differential voltage across the left sides of C_{S1} and C_{S4} changes from $-V_{rd}$ during ϕ_1 to zero during ϕ_2. This causes the differential output to increase by V_{rd} attenuated by both the load capacitors and the sampling capacitors attached to the inputs.

From a common-mode standpoint, the left sides of C_{S2} and C_{S3} float while connected together during ϕ_2. Therefore, under ideal conditions during ϕ_2, the common-mode component of the input remains on C_{S2} and C_{S3}, and the common-mode component of the reference remains on C_{S1} and C_{S4}. As a result, there is no change in the common-mode output under ideal conditions even if the common-mode input and reference are unequal and/or time varying.

For simplicity, assume at first that:

1. $C_{S1} = C_{S2} = C_{S3} = C_{S4} = C_S$,
2. $C_{L1} = C_{L2} = C_L$, and
3. the switches are ideal.

Under these ideal conditions, the common-mode and differential outputs of the differencing circuit in Fig. 1 at the end of ϕ_2 are:

$$V_{oc} = V_{bias}, \text{ and} \tag{1}$$

$$V_{od} = -\frac{C_S}{2C_S+C_L}(V_{id} - V_{rd}), \tag{2}$$

where $V_{id} = V_{i1} - V_{i2}$ and $V_{rd} = V_{r1} - V_{r2}$. Equation 1 shows the key advantage of this circuit: with ideal switches and perfect matching, the samples of V_{oc} at the end of ϕ_2 are constant (equal to V_{bias}), independent of the samples of the input and reference at the end of ϕ_1. Therefore, the first preamplifier stage of a comparator using this switched-capacitor differencing circuit will have greatly relaxed specifications for its common-mode input range and common-mode gain. Under the same conditions, Equation 2 shows the key disadvantage of this circuit: the differential gain here is about half that of a conventional differencing circuit because four sampling capacitors are required instead of just two. However, the ratio of the differential to the common-mode gain of the differencing circuit in Fig. 1 is greater than that of a conventional differencing circuit (which has equal differential and common-mode gains).

Also, the preamplifier following Fig. 1 can be different than the one following a conventional differencing circuit. Because the allowed common-mode gain for the preamplifier is increased by using the differencing circuit in Fig. 1, a tail current source connected in a standard differential-pair configuration may not be required. Eliminating the tail current source would allow operation at a reduced supply voltage. If the supply voltage is constant, the $V_{gs} - V_t$ allocated to other transistors in the preamplifier can be increased, increasing the overall speed.

For simplicity, the differencing circuit was assumed to contain no capacitor mismatch at first. Under this condition, the attenuation of V_{id} in Equation (2) was identical to that of V_{rd}, and the common-mode-to-differential gain and differential-to-common-mode gain were zero. With mismatch, however, V_{id} and V_{rd} may be attenuated by different factors, changing the comparator threshold from its ideal value. Also, the cross-gain terms may be nonzero with mismatch. Therefore, changes in V_{id} will cause changes in V_{oc}, requiring that the preamplifier can tolerate this change in its common-mode input. On the other hand, nonzero common-mode-to-differential-mode gain in the differencing circuit does not cause a limitation if the switches are ideal because the common-mode input and reference are held on C_{S1}-C_{S4}; therefore, the change in the common-mode input during ϕ_2 is zero. Although the change in the common-mode input is nonzero in practice because of charge injection, clock feedthrough, and noise coupling onto the floating nodes, the change in the common-mode input can be much less than in a conventional differencing circuit in applications where the common-mode input and reference are unequal. For example, consider a fully differential two-step ADC that must operate on a single-ended input signal. If operational amplifiers (op amps) are used, Yen and Gray's technique allows conversion of a single-ended input to a differential signal in the input sample-and-hold amplifier. In many practical two-step ADCs, however, op amps are avoided to reduce power dissipation [1, 8, 12-14]. Then if the comparators use a conventional differencing circuit, the common-mode input changes by half the differential input from ϕ_1 to ϕ_2, which is as large as 1 V in many applications. In contrast, we estimate that the the common-mode voltages of the floating nodes on the left sides of the capacitors in Fig. 1 change by less than about 100 mV from ϕ_1 to ϕ_2 in practice. (HSPICE simulations of the prototype comparator described next show changes less than 2 mV.) Therefore, the differential output that would arise from capacitor mismatch and changes in the common-mode inputs is small under practical conditions even though the common-mode-to-differential gain is greater than zero. After accounting for the reduced differential gain, we estimate that the circuit in Fig. 1 increases the ratio of the differential to common-mode gain of the comparators by about 10-20 dB in practice, potentially allowing low-resolution differential ADCs to operate on single-ended inputs without op amps.

III. Prototype Comparator

Fig. 2 shows a block diagram of the comparator. It consists of the input switching network shown in Fig. 1 followed by two preamplifiers and then a latch. The preamplifiers are identical except that they are clocked 180° out of phase so that the entire structure can be pipelined [15]. The timing is controlled by standard two-phase nonoverlapping clocks with auxiliary phases used to reduce the magnitude of signal-dependent charge injection errors [16]. Fig. 3 shows simplified schematics for a preamplifier and the latch. Offset storage is provided by the C_1 capacitors in both circuits. Table 1 shows the corresponding capacitor values and transistor sizes. As suggested in Section II, the preamplifier does not use a tail current source, eliminating the associated local common-mode feedback (CMFB). However, negative feedback is provided around M_3 and M_4 through the C_2 capacitors. Ignoring parasitics other than gate capacitance, the feedback factor is $\frac{C_2}{C_2 + C_{gs3} + 2C_1}$ from a differential standpoint. From a common-mode standpoint, the feedback factor is $\frac{C_2}{C_2 + C_{gs3}}$. If the differential and common-mode loop gains are much greater than unity, the ratio of the differential to common-mode gain $\approx \frac{C_2 + C_{gs3} + 2C_1}{C_2 + C_{gs3}}$. To make this ratio greater than 1 for the preamplifier, $C_1 \gg C_2$ is chosen. Using the values in Table 1 and a gate oxide capacitance of 0.86 fF/μm^2, the resulting ratio of differential to common-mode gain ≈ 18 dB. This is important because the common-mode output of the differencing circuit will not be exactly constant in practice. For example, mismatch in the differencing circuit will cause differential-to-common-mode conversion, as described in Section II. Also, charge injection, clock feedthrough, and noise coupling onto the left sides of capacitor pairs $\{C_{S1}$ and $C_{S4}\}$ or $\{C_{S2}$ and $C_{S3}\}$ during ϕ_2 will cause changes in the common-mode output of the differencing circuit.

IV. Experimental Results

The comparator has been tested by building a 3-bit flash ADC in a 2-μm CMOS process. Fig. 4 shows the die photo. It is 2.2 mm by 2.2 mm and contains seven identical comparators. Each comparator occupies 0.25 mm^2.

Fig. 5 shows the linearity of the flash ADC at a conversion rate of 25 Msamples/s. In Fig. 5(a) differential nonlinearity (DNL) is plotted versus code, and in Fig. 5(b), integral nonlinearity (INL) versus code is plotted. The comparator offsets can be calculated from the linearity plots. The resulting standard deviation is 17 mV. Fig. 6 shows the common-mode rejection ratio (CMRR) of the flash ADC versus input frequency. Here CMRR is defined as the ratio of the common-mode input to the differential input for which the ADC outputs are equal in amplitude. As mentioned in Sections I and II, a potential application of the differencing circuit is in differential ADCs that operate on single-ended inputs. Fig. 7 shows plots of peak signal-to-distortion ratio (SDR) and signal-to-noise-and-distortion ratio (SNDR) of the flash

ADC versus input frequency for both differential and single-ended inputs. Note that the SNDR is limited by quantization noise because the resolution is only 3 bits. The single-ended performance is only about 1-2 dB worse than the differential performance over the entire range. Table 2 summarizes the comparator performance.

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TABLE AND FIGURE CAPTIONS

TABLE 1

Element sizes in Fig. 3.

Circuit	Element	Size
Preamp	M_1-M_2	60µm/2µm
Preamp	M_3-M_4	60µm/2µm
Preamp	C_1	600 fF
Preamp	C_2	100 fF
Latch	M_1-M_4	10µm/2µm
Latch	M_5-M_6	20µm/2µm
Latch	C_1	500 fF

TABLE 2

Comparator Performance Summary (25°C)

Technology	2-µm double-poly CMOS
Area	0.25 mm^2
Supply Voltage	3.3 V
Power Dissipation	1.05 mW
Sampling Rate	25 Msamples/s
Standard Deviation of Offset	17 mV

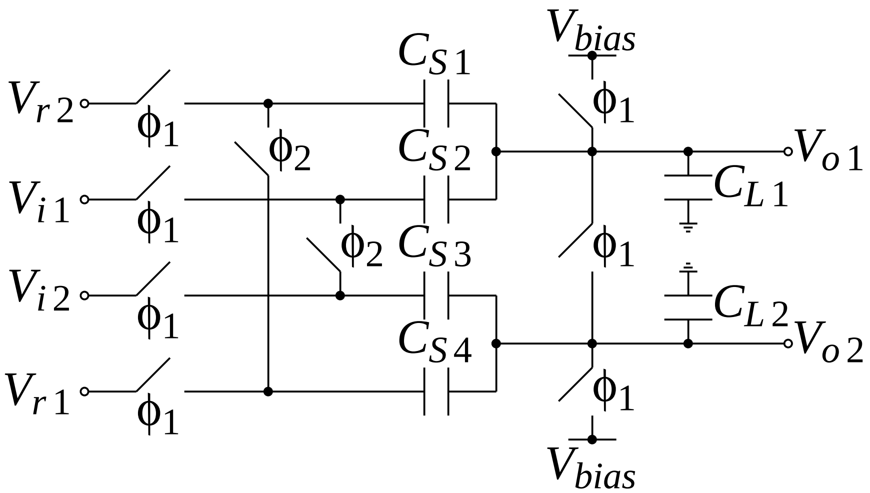

Fig. 1: Differencing circuit with common-mode rejection.

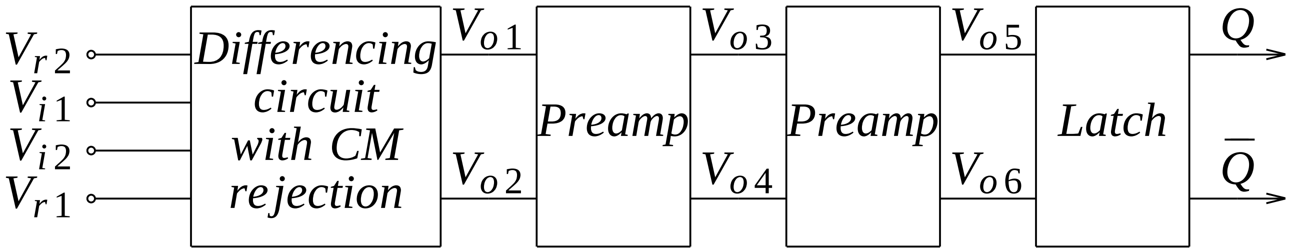

Fig. 2: Block diagram of comparator.

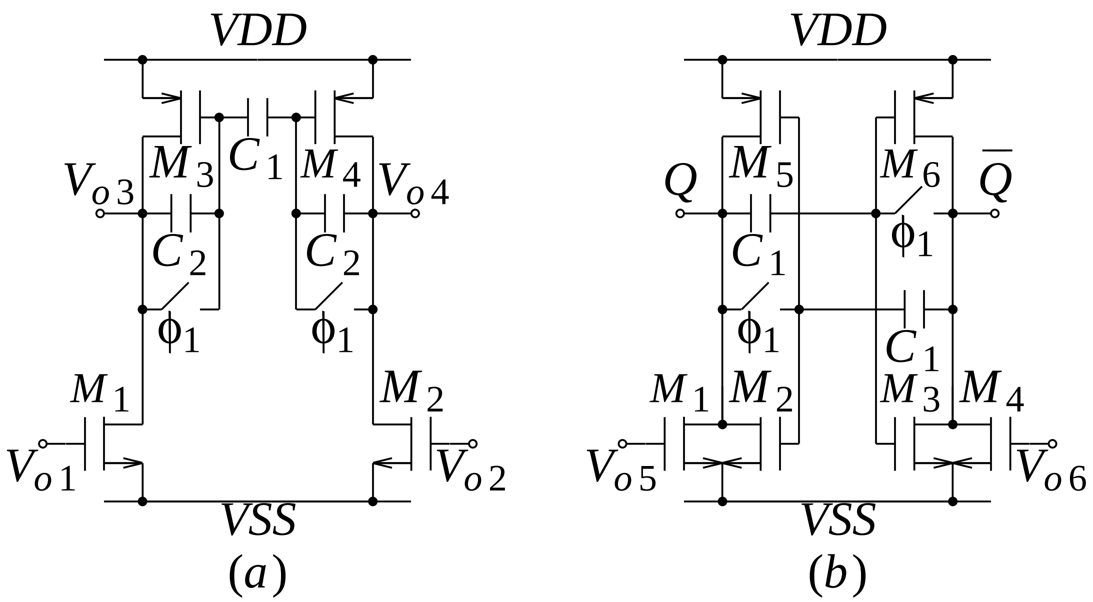

Fig. 3: Simplified schematics: (a) preamplifier and (b) latch.

Fig. 4: Die photo.

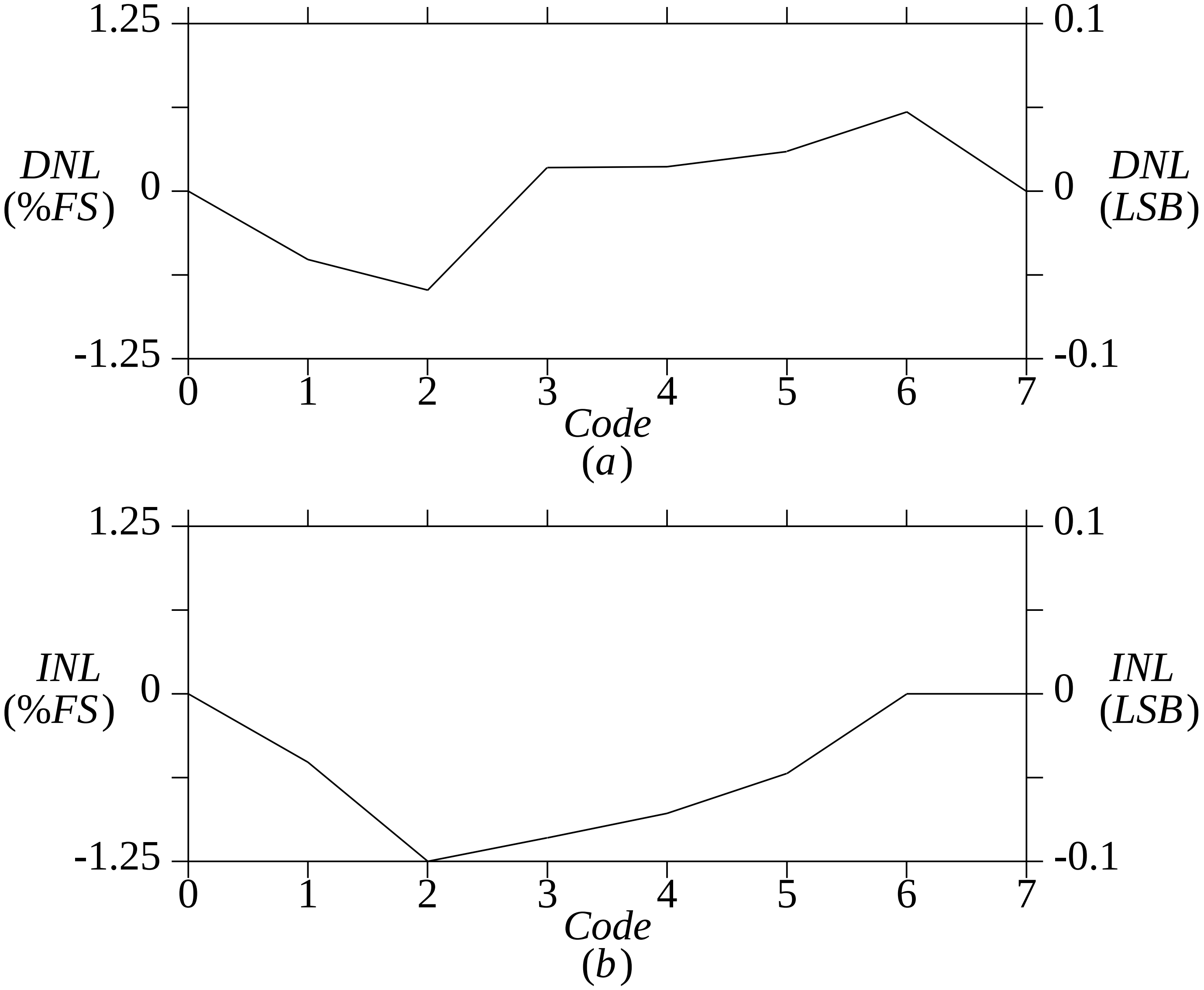

Fig. 5: Flash ADC nonlinearity versus code (25 Msamples/s): (a) DNL and (b) INL.

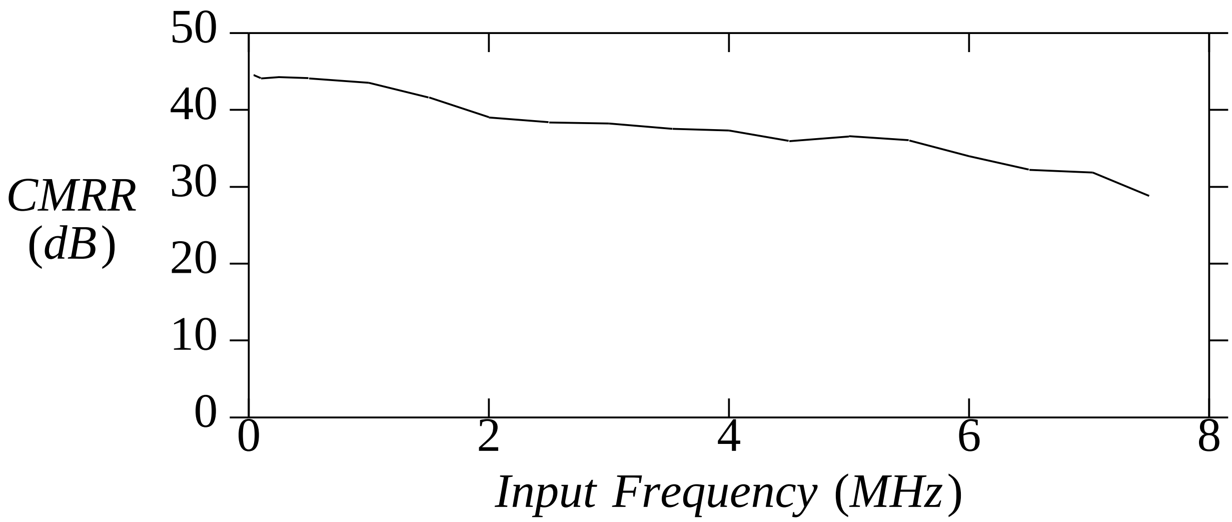

Fig. 6: ADC Common-Mode Rejection Ratio versus Input Frequency (25 Msamples/s)

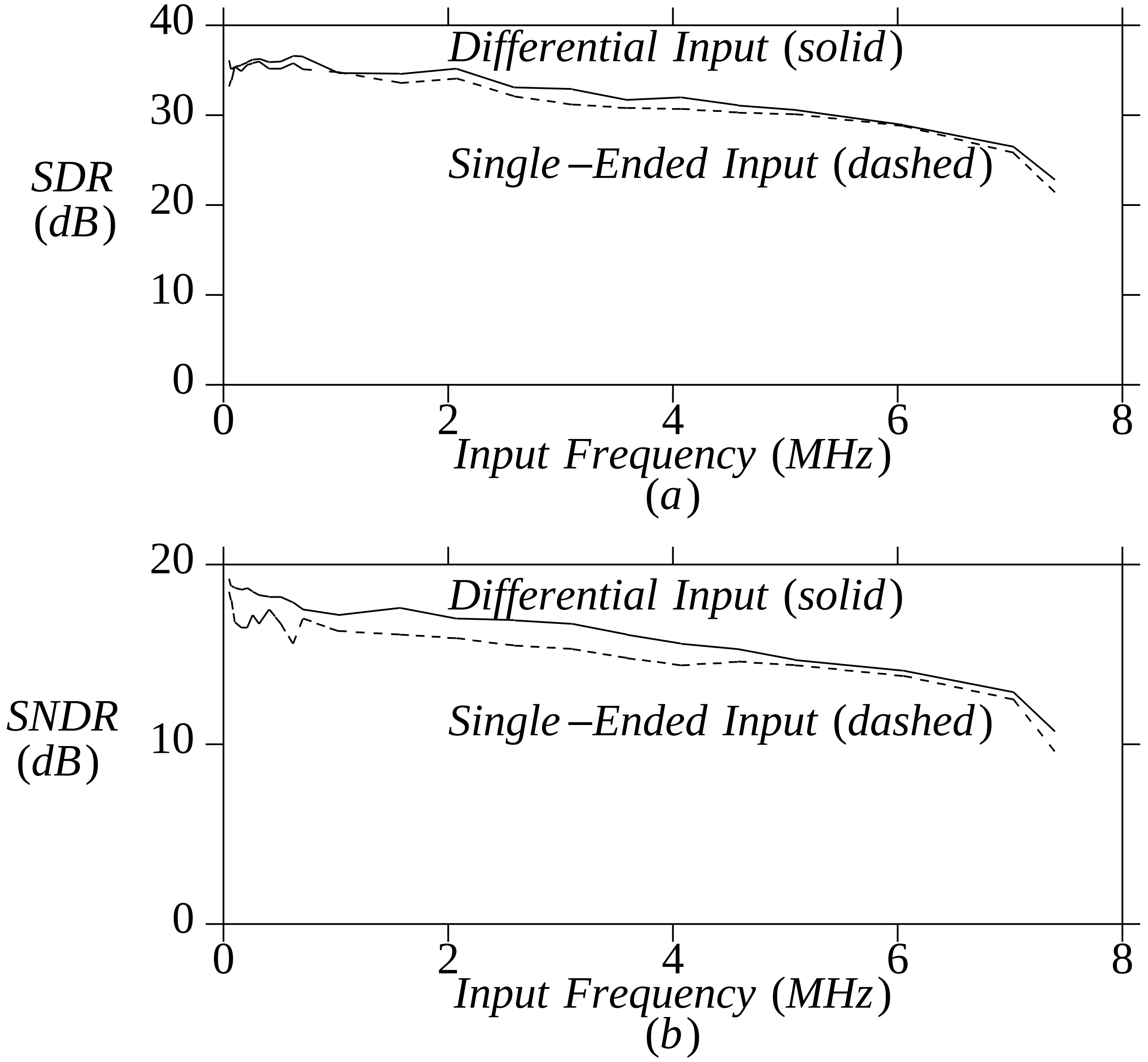

Fig. 7: ADC Performance versus Input Frequency for Differential and Single-Ended Inputs (25 Msamples/s): (a) Signal-to-Distortion Ratio (SDR) and (b) Signal-to-Noise-and-Distortion Ratio (SNDR)