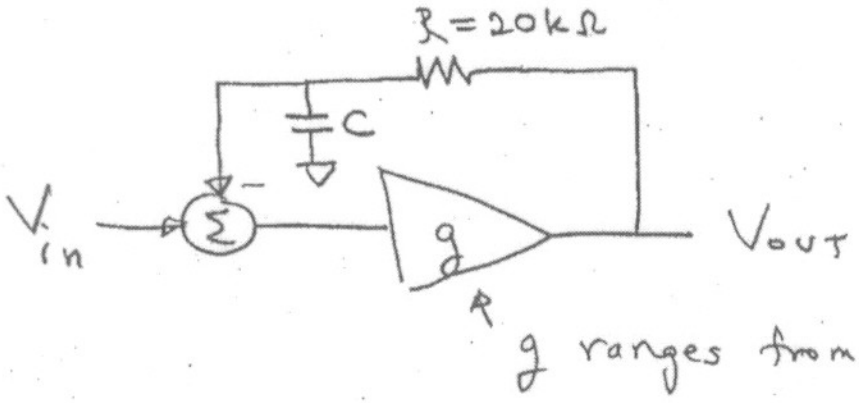
HW #2

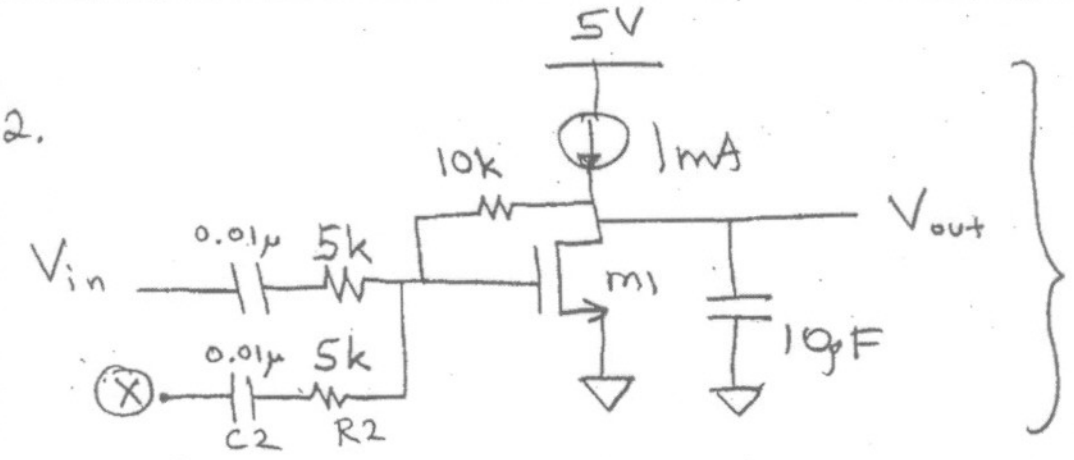
1. A gain stage with feedback to keep the output offset voltage low is shown below.



a) What value of C will give a pole magnitude $\leq 2\pi(30kHz)$ over the entire gain range?

b) What is the range of output offset voltage if the offset voltage at V_{in} is 0.1V?

2.



M1 : $W = 200\mu m$ $L = 0.5\mu m$

$AS = AD = 100(\mu m)^2$ $PS = PD = 201\mu m$

a) With ⓧ connected to V_{in}, use HSPICE to find the gain and upper f_{-3dB} for this circuit.

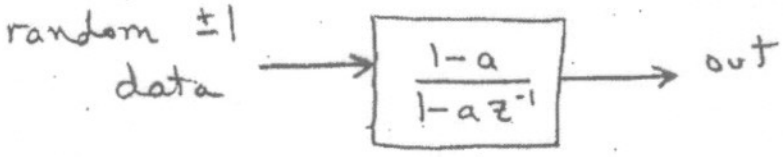
b) Remove R2 & C2 and repeat a). Why does f_{-3dB} change?

c) Simulate the circuit again, with ⓧ connected to ⏚. How does f_{-3dB} compare with a) & b)? Explain.

Use the mos models in the file:

~hurst/215/mos_models

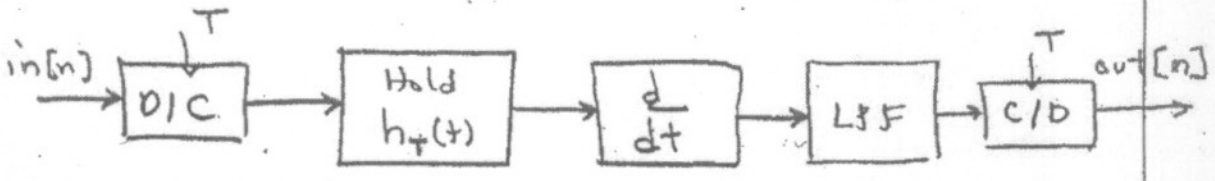
or on the 215 web page.

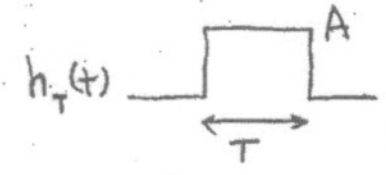
3. 

Let $a = 0.2$

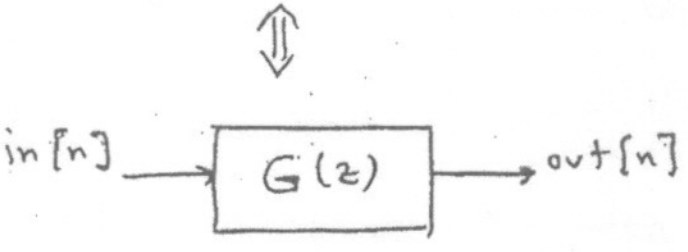
Simulate this equivalent discrete-time channel for a large number of bits (~ 1000) to find the range of high outputs and the range of low outputs.

4. Find the equivalent discrete-time channel $G(z)$ for the following:



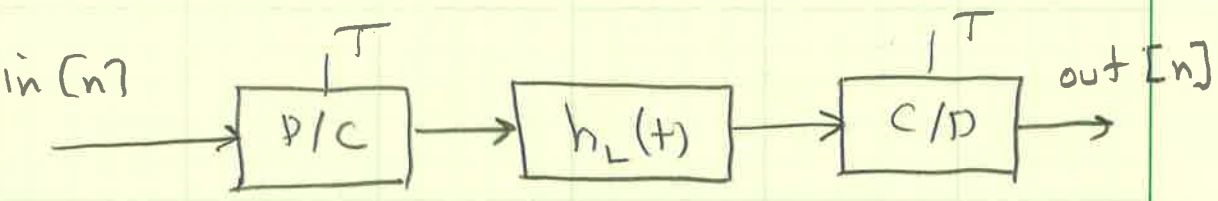


$$LPF(s) = \frac{1}{1+sT_1}$$

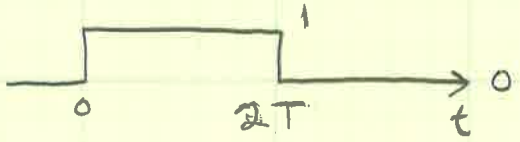


(hint: let $in[n] = \delta[n]$, then $out[n] = g[n]$.
$g[n] \leftrightarrow G(z)$.)

5. Find the equivalent discrete-time model $G(z)$ for the following:

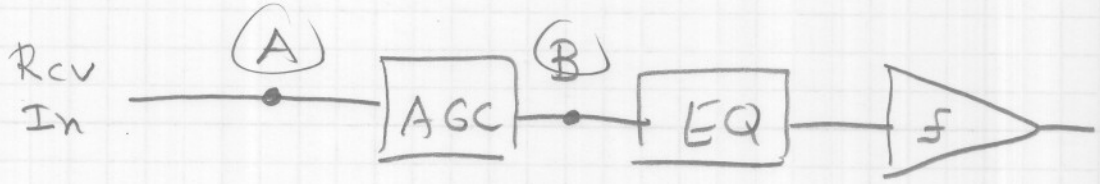


$h_L(t) \Rightarrow$



$$h_L(t) = \begin{cases} 1 & 0 \le t < 2T \\ 0 & \text{else} \end{cases}$$

6.



Assume the $\frac{\text{peak}}{\text{rms}}$ ratio of the RcvIn signal is 5 ($\approx$ 14 dB) and the range of RcvIn is 24 dB

$$(24\ \text{dB} = 20 \log \left[\frac{(\text{largest RcvIn})_{\text{rms}}}{(\text{smallest RcvIn})_{\text{rms}}} \right]).$$

If the SQNR required is $\geq$ 22 dB:

a) How many bits are needed if an ADC is placed at (A), before the AGC? Assume RcvIn $(\overset{\text{max}}{\text{peak}})$ = ADC full scale.

b) How many bits are needed if an ADC is placed at (B)? Assume the AGC is ideal, and the peak at (B) = ADC full scale for any RcvIn signal.