EEC 212
Problem Set 3

Professor Hurst

Read: Chapters 5 and 6

1

Design the folded-cascode op amp in Figure 1 for use in a feedback circuit with unity-gain feedback (i.e., as a voltage follower with its output connected to its inverting input). Design the op amp so that it has a gain-bandwidth product (GBW) (or unity-gain frequency f_u) of 10 MHz when $C_L = 5$ pF. Design for maximum output swing.

Use $V_{DD} = -V_{SS} = 2.5V$, $|V_{T0}(N)| = |V_{T0}(P)| = 0.8$V, $|V_{GS} - V_T| = 0.2$V for PMOS and NMOS transistors, $\mu_N C_{OX}/2 = 25\frac{\mu A}{V^2}$, and $\mu_P C_{OX}/2 = 10\frac{\mu A}{V^2}$. Assume the device capacitances in the op amp can be modeled by four capacitors: two capacitors from node 8 and 9 to ground, each with value $C_{n8} \approx 2(W/L)_1(10$ fF) and two capacitors from node 11 and 12 to ground, each with value $C_{n11} \approx (W/L)_9(10$ fF). Also, use M1=M2, M8=M9, M5=M6, M10=M11, and M12=M3=M4.

In addition to (W/L) values, calculate values for I_B, V_{B1} and V_{B2}. Estimate the phase margin for your design, assuming the op amp is in unity gain feedback as shown in Figure 3.

Assume that the op-amp gain rolls off at -6dB/octave up to (and somewhat beyond) the unity gain frequency. So the unity-gain frequency can be simply related the op-amp's DC gain and the dominant pole.

To estimate the phase margin, assume that C_{n8} and C_{n9} together introduce one pole approximately given by $-g_{m6}/C_{n8}$. Also, assume that C_{n11} and C_{n12} introduce poles at $p_{11} = -g_{m9}/C_{n11}$ and $p_{12} = -g_{m7}/C_{n12}$, respectively. However, because they operate on only 1/2 the signal path, assume that C_{n11} and C_{n12} also each introduce a left-half-plane zero that is twice the value of the corresponding pole.

2

Use the data from Table 2.4 in Problem Set 1, but use $\lambda_N = 0.04\text{V}^{-1}$ and $|\lambda_P| = 0.05\text{V}^{-1}$.

(a) For the simple op-amp in Figure 2 compute the small-signal gain v_{out}/v_{id} and output resistance. Assume all of the transistors are saturated and $V_{OUT}(DC) \approx 0$V. All transistors have $V_{BS} = 0$V (source connected to body; M1 and M2 are in N-wells). All transistors have L=0.5μm.

(b) Estimate the common-mode input range and output swing limits for this op-amp.

(c) If a C_{LOAD} =10pF is connected from V_{out} to ground, what is the slew rate?

(d) What is $Z_{in,d}$? (The differential input impedance of the op-amp).

(e) The op-amp is place in a feedback loop as shown in Figure 3. Calculate the closed-loop output resistance, and compare it to $1/G_m(op\ amp)$.

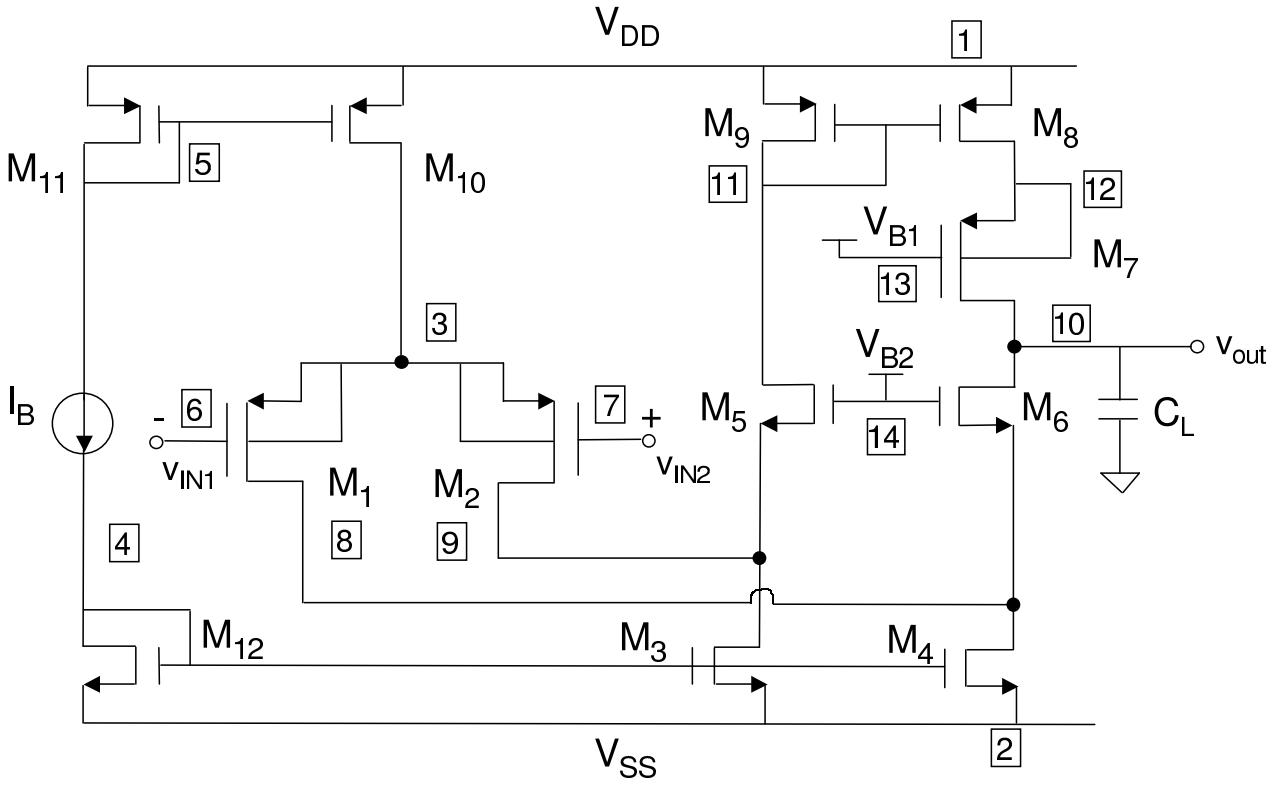

Figure 1: Folded-cascode op amp.

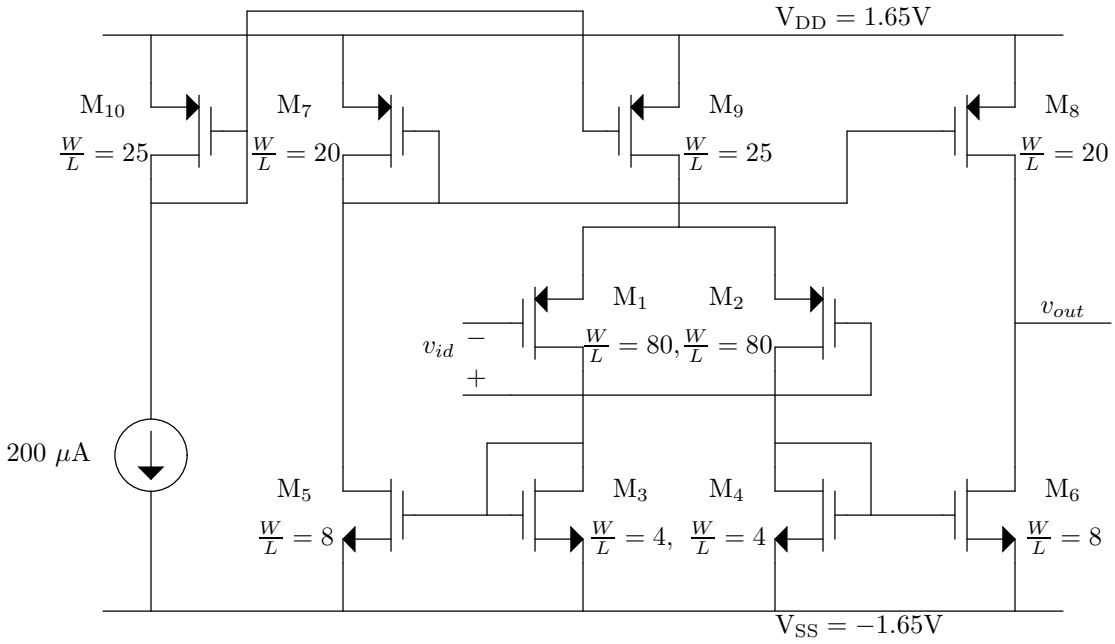

Figure 2: Amplifier

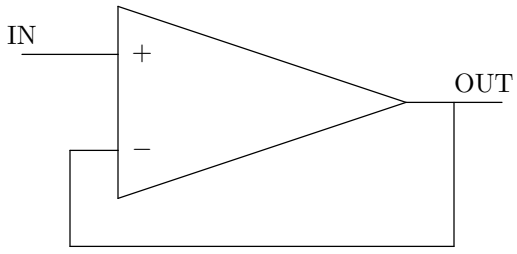

Figure 3: Amplifier in feedback loop