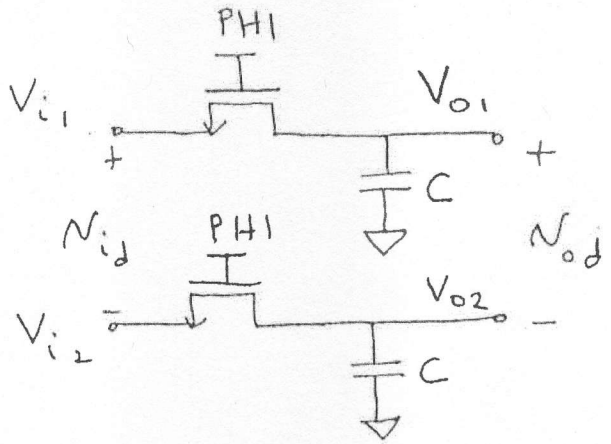
W 2022 Midterm Soln EEC 212

1. The circuit below is a differential Sample-and-Hold circuit. Each NMOS transistor acts as a switch, controlled by the clock PHI.



(4 pts) a) Assume that PHI is high (V_{PHI} = 5V) and each NMOS transistor is in the triode region, with V_{DS} = 0V. Find W/L to give an on-resistance R_{ON} of 40 kΩ for each transistor. Assume the two inputs are both 0 V for this calculation.

W / L = _____

$$R_{on} = \frac{1}{k_n' \frac{W}{L}(V_{GS} - V_T)}$$

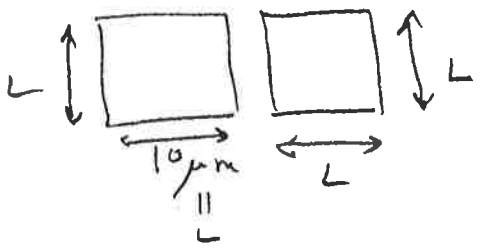
$$= \frac{1}{180\frac{\mu A}{V^2}\left(\frac{W}{L}\right)(5V - 1V)} = 40k\Omega$$

$$\Rightarrow \frac{W}{L} = 0.035$$

(1 con't)

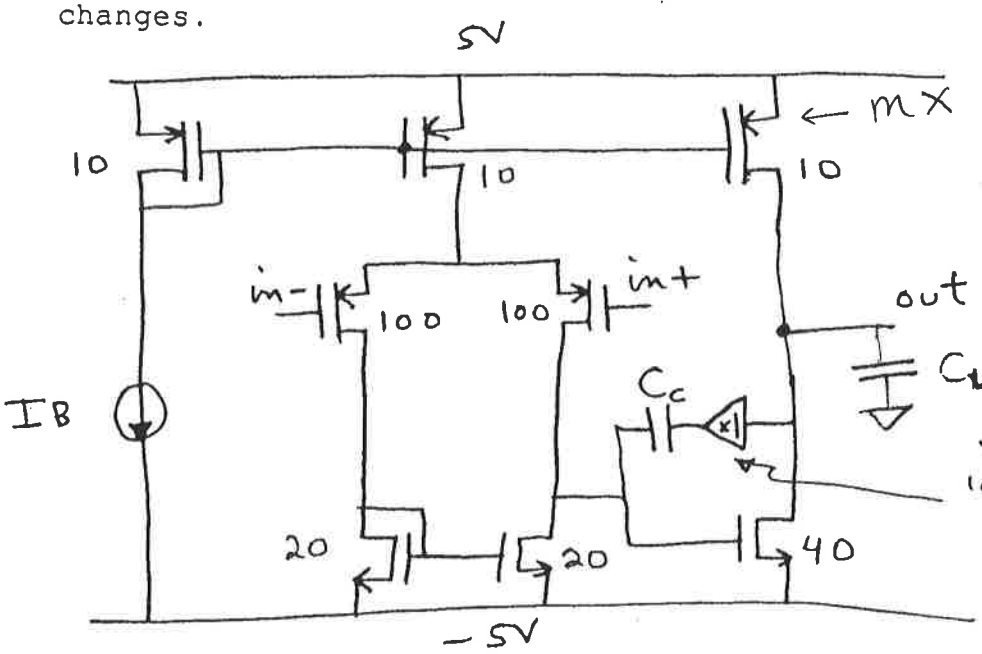
b) It is important that the capacitors and transistors are closely matched. You are allowed 200 $(\mu m)^2$ of total area for the top plates of the two capacitors. Sketch the layout of the top plates for the two capacitors. Give the dimensions of the capacitors on your drawing. (For this part, the most important thing is capacitor matching. Don't worry about the -3 dB frequency of the filter or the capacitor values.)

use max area, close together,



(could include common centroid)

2. A two-stage op amp is shown below. It was designed to have a bias current IB = 20 μA. However, due to a layout error, the op amp is operating with a bias current IB = 10 μA, which is half of the design value. For each parameter below, relate the value of the parameter when IB = 10 μA to the value of the parameter when IB = 20 μA. (That is, find the scale factor that relates the two values.)
Assume DC biasing places all the transistors in the saturation region for both values of IB, and further assume that all capacitances do not change when the bias current changes.



W/L values are next to transistors.

a) How does the low-frequency voltage gain, $a_v = v_{out}/v_{id}$, change?

$a_v(IB = 10\ \mu A) = v_{out}/v_{id} \approx$ 2 $\cdot a_v(IB = 20\ \mu A)$

$$a_v = g_{m_1} R_{o_1} g_{m_5} R_{o_2}$$

$$\propto \sqrt{I_B} \cdot \frac{1}{I_B} \cdot \sqrt{I_B} \cdot \frac{1}{I_B} = \frac{1}{I_B}$$

b) slew rate(IB = 10 μA) ≈ $\frac{1}{2}$ · slew rate(IB = 20 μA)

c) The output resistance of the op amp is R_{out}.

op amp R_{out}(IB = 10 μA) ≈ 2 · [op amp R_{out}(IB = 20 μA)]

$$R_{out} = r_{o_5} \| r_{o_4} \propto \frac{1}{I_B}$$

$$\propto \frac{1}{I_B} \quad \propto \frac{1}{I_B}$$

d) dominant pole: p_1(IB = 10 μA) ≈ $\frac{0.35}{(\frac{1}{2})^{\frac{3}{2}}}$ · p_1(IB = 20 μA)

$$p_1 = \frac{-1}{g_{m_5} R_{o_1} R_{o_2} C_c}$$

$$\propto \frac{-1}{\sqrt{I_B}\,\frac{1}{I_B}\,\frac{1}{I_B}} = -I_B^{\frac{3}{2}}$$

e) The non-dominant pole is p_2:

(3) $p_2(IB = 10\ \mu A) \approx$ 0.71 $\cdot\, p_2(IB = 20\ \mu A)$

$$p_2 \simeq -\frac{g_{m5}}{C_2} \propto -\sqrt{I_B}$$

(2) f) The upper limit of the op-amp output voltage swing is $\hat{V}_{out}^{+}$:

Circle one:

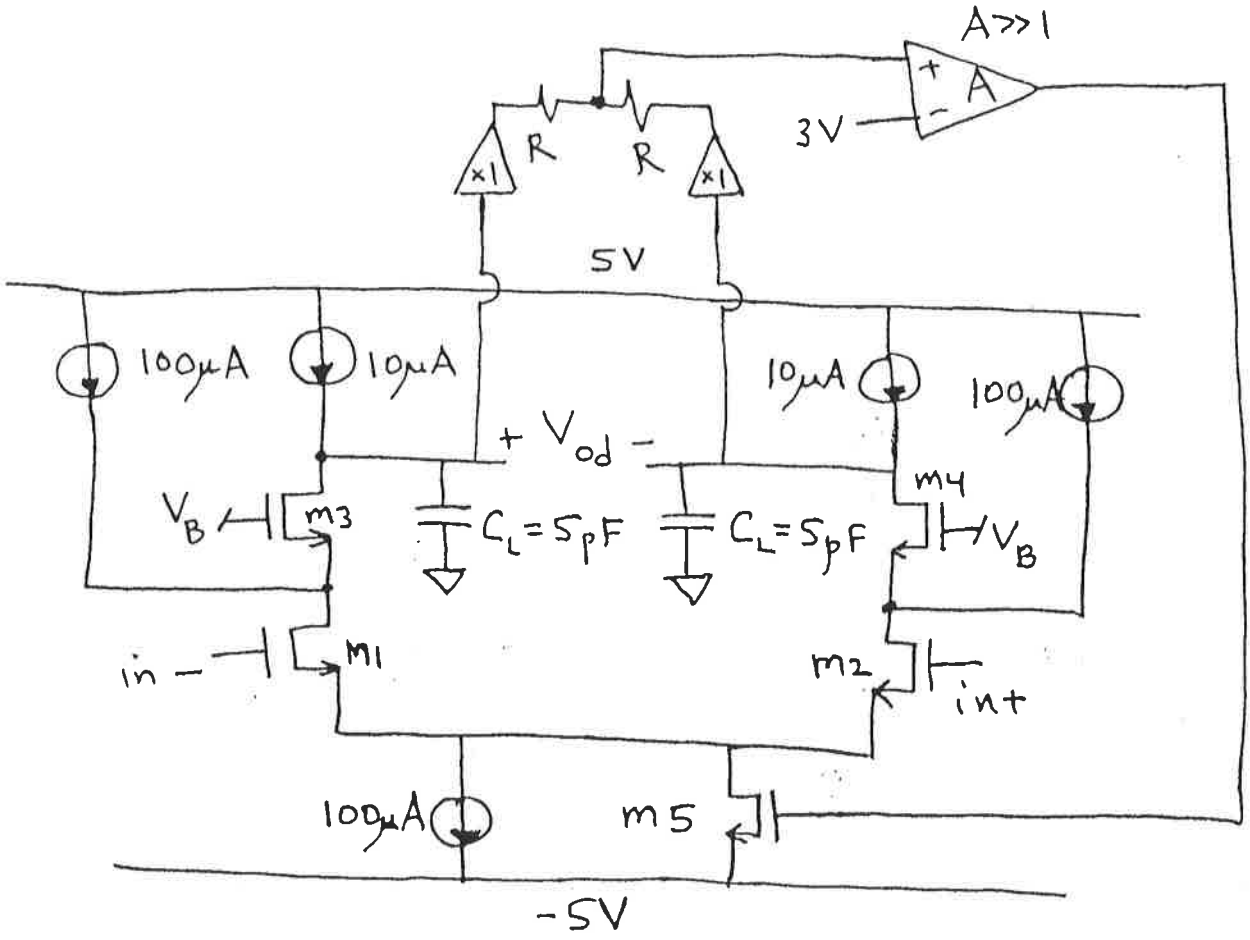
$\hat{V}_{out}^{+}(IB = 10\ \mu A)$ is LESS THAN, (GREATER THAN), SAME AS $\hat{V}_{out}^{+}(IB = 20\ \mu A)$

$$\hat{V}_{out}^{+} = 5V - \left|V_{DS_{SAT}(mX)}\right|$$

$$= 5V - \sqrt{\frac{2I_{D(mX)}}{k'_p(10)}}$$

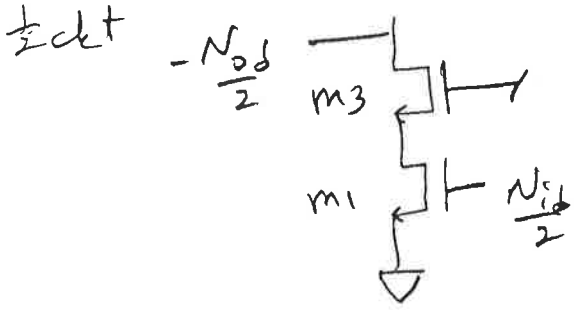
$I_B \uparrow \Rightarrow \quad \uparrow \Rightarrow \quad \hat{V}_{out}^{+} \downarrow$

3. A fully differential op amp with common-mode feedback is shown. Assume all transistors are saturated, and assume M1 = M2 = M3 = M4 = M5. All transistors have W/L = 50. Ignore all capacitances except C_L.



(2) a) What is the DC drain current in M5? $I_D(M5)$ = 120μA // 220μA − 100μA

b) What is the differential-mode gain? v_{od}/v_{id} = _____



$I_{b_1} = 110\mu A$

$I_{b_3} = 10\mu A$

$g_{m_1} = \sqrt{2\left(180\frac{\mu A}{V^2}\right)(50)110\mu} = 1410\frac{\mu A}{V}$

$g_{m_3} = 425\frac{\mu A}{V}$

$$\frac{N_{od}}{N_{id}} \simeq g_{m_1}\left(r_{o_3} \cdot g_{m_3} r_{o_1}\right) =$$

$$= \left(1410\frac{\mu A}{V}\right)\cdot\left(\frac{1}{0.02 \cdot 10\mu A}\right)\cdot\left(425\frac{\mu A}{V}\right)\cdot\left(\frac{1}{0.02\ 110\mu A}\right) = \underline{1.36M}$$

c) What is the slew rate? dV_{od}/dt = $\frac{44\,V}{\mu sec} = 44 \times 10^6 \frac{V}{sec}$

max $I_{out+} = 110\mu A$

flows thru two 5pf caps

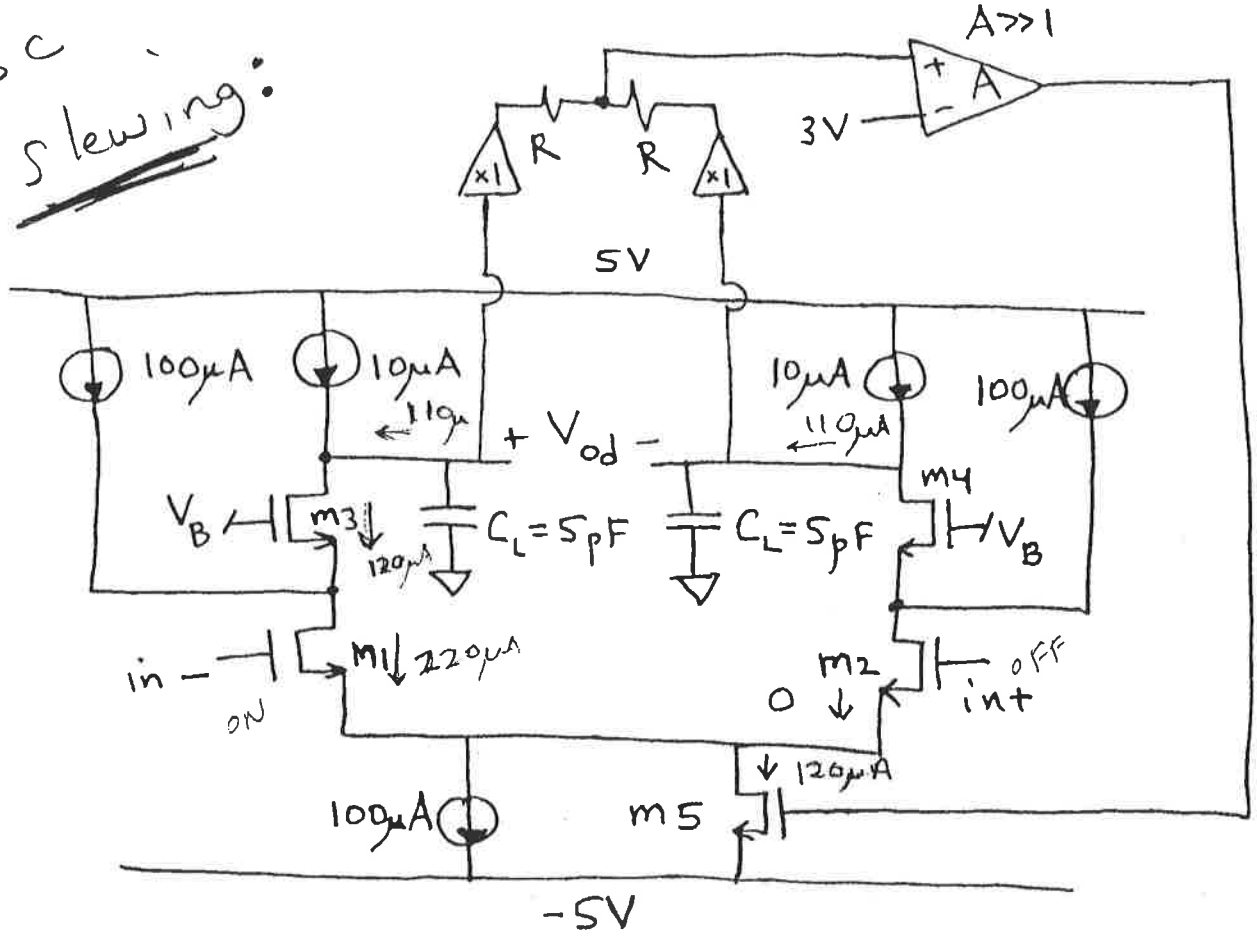
in series

$$\Rightarrow \frac{dV_{od}}{dt} = \frac{I}{C} = \frac{110\mu A}{2.5pF} = 44\ \frac{V}{\mu sec}$$

A fully differential op amp with common-mode feedback is shown. Assume all transistors are saturated, and assume M1 = M2 = M3 = M4 = M5. All transistors have W/L = 50. Ignore all capacitances except C_L.

#3c

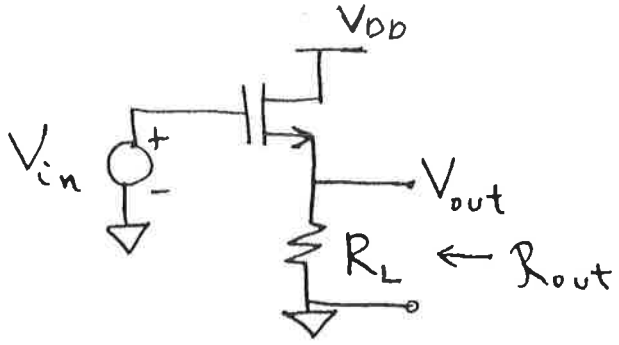
slewing:



a) What is the DC drain current in M5? $I_D(M5)$ = 120 μA

220μA - 100μA

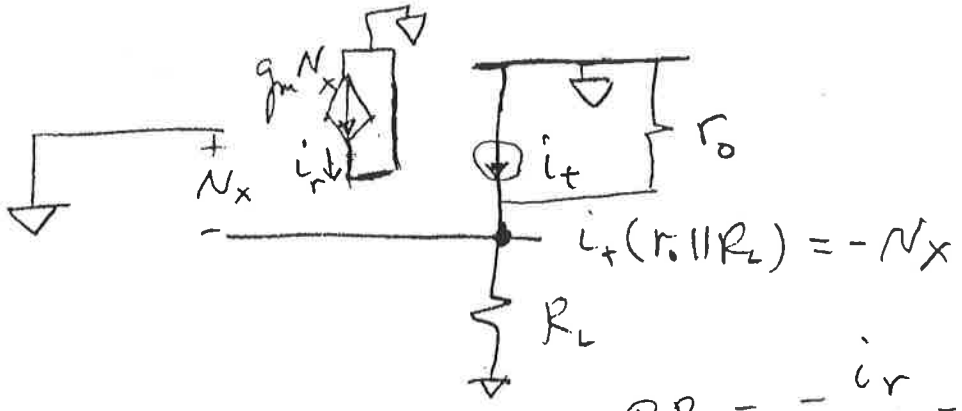
4. Use Blackman's impedance formula to compute the output resistance of the circuit below. Compute the return ratios with respect to the g_m controlled source of M1. Assume the transistor is saturated. Give the results in terms of R_L and transistor parameters that could be computed, such as g_m, r_o, etc. Ignore all capacitances in this problem.



a) What is R_{out} when $g_m(M1) = 0$? $R_L \| r_o$

$R_L \| r_o$

b) What is RR(g_m(M1) with output port open)? $g_m(r_o \| R_L)$



$$RR = -\frac{i_r}{i_t} = g_m(r_o \| R_L)$$

c) What is RR(g_m(M1) with output port shorted)? 0

short out → $V_{out} = V_X = 0$

→ no return current

d) Now applying Blackman's formula, what is R_{out} of this feedback circuit?

$$R_{out} = r_o \| R_L \cdot \frac{1}{1 + g_m(r_o \| R_L)}$$

$$\left(\simeq \frac{1}{g_m} \text{ if } g_m(r_o \| R_L) >> 1 \right)$$