

Qualifications Summary

Research scientist experienced in developing next generation networking solutions, having extensive exposure in designing embedded systems.

Experience Highlights

Research Experience

Associated with Laboratory of Embedded and Programmable Systems (<http://leps.ece.ucdavis.edu>), UC-Davis (September 2006 – Present) having researched on

- Programmable Architectures for Real-time Network Traffic Measurements (Active)
- Heavy Hitters Identification in IP-networks Using Network of Processors
- A Hardware Software Co-Design of LDPC Decoder

Associated with King Fahd University of Petroleum & Minerals (July 2002 – December 2005) having researched on

- Finite State Machine State Assignment for Area, Power Minimization and Increased Testability.

Industrial Experience

Hardware Design Engineer at Digitek-Mantero Networks, Pakistan – Maryland, USA (Jan-August, 2006)

- Design and development of next generation communication devices for Hughes Networks
- Up-gradation of OPENCORES' PCI core for internal project

Teaching Experience

Teaching Assistance experience at UC-Davis for

- Senior Digital Systems Design Course (Spring-08, Winter-09)
- First Level Digital Systems Design (Fall-07, Fall-08)
- Senior Design Projects (Spring – 09)

Development of FPGA CAD Laboratory in Computer Engineering Department, KFUPM (2003)

Selected Accomplishments

- UC-Davis OGS Fellowship, September 2006
- College of Computer Science (KFUPM) 'Special Contribution Award' for CAD Laboratory Development, 2003.
- King Fahad University (Saudi-Arabia) Fellowship for pursuing Masters in Computer Engineering, 2002.
- HSC merit Scholarship for securing 13th position in HSC-Examinations, 1996
- President of Pakistan Talent Farming Scholarship for securing 14th position in Presidential Talent Farming Competition, 1993.

Publications

- Faisal N. Khan, Lihua Yuan, Chen-Nee, Sohail Ghiasi, "A Programmable Architecture for Scalable and Real-time Network Traffic Measurements", ANCS-08, November 6-7, San Jose, CA.
- Aiman El-Maleh, Sadiq M. Sait and Faisal N. Khan, Finite State Machine State Assignment for Area and Power Minimization, ISCAS-2006 (Paper Number 2695)

- “A VLSI Implementation of Fully Pipelined Baseline JPEG Encoder”, IEEE conference on ‘Technology Extravaganza’, 11th August 2000, NEDUET (IEEE Record No. 8204).

Areas of Specialization

- Extensive exposure in FPGA based designs, Embedded Systems, Verilog, C/C++ and Assembly languages (8088/8051).
- Highly experienced in working with networking protocols and designing measurement equipment on Xilinx platforms.
- Experienced in multiprocessor designing and programming.
- Experienced in Partial Dynamic Reconfiguration of FPGA Logic.

Education

- Ph.D in Electrical and Computer Engineering, UC-Davis. (Expected – Fall-'10; GPA: 3.53)
- M.Sc in Computer Engineering, KFUPM, Dhahran, KSA. GPA: 3.72. (Sept 2002 – June 2005)
- Bachelors in Computer Systems Engineering; NEDUET, Karachi. Graduated with honors, (1997-2001)