A Guide for Using Modelsim

EEC 180 • UC Davis • B. Baas

EEC 180 uses Quartus II Prime and ModelSim. This document describes steps to use the ModelSim simulator.

Place one verilog module inside each file with the name *modulename*.v

Edit verilog modules in a separate editor.

To make examples easier to read, the top-level module name is assumed to be "top" in this document.

In some cases, the time stamp of the corresponding discussion in the video is given along the right edge.

To have copies handy, consider downloading ModelSim documentation: Help > PDF documentation > [select document]

1. Setup

As instructed in the *Recommended file organization* web page and video, create a folder for your project as well as the following subfolders:

- hdl/ Hardware verilog files
- simulation/ ModelSim-related files
- synthesis/ Quartus-related files
- testbench/ Testbench verilog files

Run SystemBuilder to make a quartus project. Place all files in the synthesis/ subfolder except for the top-level module file which should be placed in hdl/

2. Running Modelsim

1. Run ModelSim from the start menu or a desktop shortcut
2. Modelsim will automatically open to the last project you worked on. Skip step #4 if you do not want to start a new project.
3. Simulate > Runtime Options… > Defaults tab > Default radix: binary
    a. This makes waveforms appear in binary format in your waveform viewer by default.
4. File > New > Project… [5:35]
    a. Enter Project Name: top
    b. Browse: navigate to simulation/ subfolder.
    c. Default Library Name: normally leave default "work"
    d. click Reference Library Mapping
    e. click Ok

f. Popup window: Add items to the Project [6:00]
   i. click Add Existing File (for hardware verilog)
   ii. Browse… navigate to hdl/ subfolder, click or shift-click to select all .v files
   Click Open
   iii. **Always** click Reference from current location
   iv. click Ok

g. Add Existing File (for testbench verilog). Follow the same instructions given in section 3.f except navigate to the testbenches/ subfolder instead. [7:10]

h. Close

i. You should now see all files in the window

5. To add more *.v files later
   a. right click in left window > Add to project > Existing file…
6. Compile > **Compile All**
7. If Modelsim reports a compile error in the window at the bottom, double click on the red line reporting the error to see details
8. Simulate > **Start simulation** > popup window [8:10]
   a. Open "+" by project name "work"
   b. Click on testbench top_tb
   c. Ok
9. If you do not see the waveform sub-window: View > check Wave
10. In left window: click "sim" tab on bottom, click top level testbench in left window, drag to waveform viewer—it puts all signals onto the waveform viewer
11. Simulate > Run > **Run -All** (there is also a small "run all" button)
12. The right window has several tabs on the bottom: Wave and testbench Verilog top_tb.v
    Click the Wave tab.
13. Type "f" to Zoom Full. Or right click in the waveform window and choose a zoom option.
14. Right click on the signal names in the waveform window to choose an appropriate Radix to make the signals easy to understand.
15. Output from $write and $display commands will appear in the bottom window

- If you do not see the waveforms of signals you expect (if you add signals to waveform that are not logged, or sometimes if a module is changed)
   a. Simulate > Restart… (there is also a small "Restart" button)
   b. Check all
   c. Ok
   d. Simulate > Run > **Run -All**

- When you make changes in a source Verilog file (in a separate editor), sometimes the system will give you a popup window saying, “Warning! File modified outside of source editor.” If you get this, click “Reload” [10:50]
    a. Click the Project tab on the bottom of the left window
    b. You should see a “?” Status for top_tb.v [11:09]
    c. Compile > **Compile Out of Date**
    d. Compile > **Compile All**
    e. Status should now be a green checkmark
    f. Simulate > Run > **Run -All**

Todo:

- How can all signals in the entire hierarchy be logged for waveform viewing automatically?

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2020/04/17 Written