UNIVERSITY OF CALIFORNIA, DAVIS
Department of Electrical and Computer Engineering

EEC180A DIGITAL SYSTEMS I Winter 2015

LAB 5: STATIC HAZARDS, LATCHES AND FLIP-FLOPS

Hardware Required

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>74LS00</td>
<td>Quad 2-Input NAND Gates</td>
</tr>
<tr>
<td>2</td>
<td>74LS04</td>
<td>Hex Inverters</td>
</tr>
<tr>
<td>1</td>
<td>74LS10</td>
<td>Triple 3-Input NAND Gates</td>
</tr>
<tr>
<td>2</td>
<td>74LS02</td>
<td>Quad 2-Input NOR Gates</td>
</tr>
<tr>
<td>2</td>
<td>74LS74</td>
<td>Dual D positive edge Flip Flop</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>LED's and current-limiting resistors</td>
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Pre-Lab

- Read Unit 8 (Hazards), Unit 11.1 – 11.4, and Unit 11.8 in the Roth textbook

- Analyze the function $Y = SEL \& A + SEL' \& B$ using a Karnaugh map. Determine whether this function has a static 0-hazard or a static 1-hazard. Using the K-map, derive an equation which implements the same function but eliminates the static hazard. Using only parts available in the Hardware Required list (above), redesign the circuit shown in Fig. 1 to eliminate the static hazard. Be prepared to build this circuit in the lab.

- For the circuit of Fig. 2, construct a transition table summarizing the operation of the circuit. This table will show all possible “current” values for $A$, $B$, $X$, and $Y$, and also the resulting “next” values for $X$ and $Y$.

- For the circuit of Fig. 3, construct a transition table summarizing the operation of the circuit. This table will show all possible “current” values for $S$, $R$, $Q$, and $Q'$, and also the resulting “next” values for $Q$ and $Q'$.

- Do a paper design for the Combinational Logic block of Fig. 5.

Part I. Static Hazards

In the first part of the lab, you will implement a circuit with a static hazard. A static hazard is a condition where a change in a single input produces a momentary output change where no output change should occur. Static hazards are classified as either static 1-hazards, when the output momentarily goes to 0 when it should remain 1, or static 0-hazards, when the output momentarily goes to 1 when it should remain 0.

- Build the circuit shown in Fig. 1 using five inverters in series instead of the one shown in the figure in order to introduce extra delay into the circuit. The circuit implements the function $Y = SEL \& A + SEL' \& B$
Figure 1. Circuit with a static hazard

- Connect the SEL input to a 0 to +5V square wave from your clock generator circuit which you built in Lab 2. Try various input combinations for A and B and adjust the Time/Div setting of the oscilloscope until you can observe the hazard on the Y output. If you cannot see the hazard clearly, connect SEL to the other scope channel and trigger the scope off of that channel. Viewing both channels, you should be able to see the spikes clearly.

- Show the hazard on the scope to your TA and have him/her sign your verification sheet.

- Change the number of inverters before Gate 2 from five to three. 
  Q1: Do you see any difference? If so, what is the difference?
  Q2: What would happen if you add more than five inverters of delay into the circuit?
  Q3: Why might it not be a good idea to use an even number of inverters of delay?

- Redesign the circuit to eliminate the hazard. You must determine how to do this and have your design ready before coming to lab. Build the new circuit (using 5 inverters before Gate 2) and check if it still has the hazard.
  Q4: What are the other ways to eliminate static hazards?

Part II. Latches and Flip-Flops

1. Cross-Coupled NAND Latch

   - Analyze the circuit shown in Fig. 2 by constructing a transition table (explained in the textbook in Unit 11.2) summarizing the operation of the circuit, and construct a transition table before coming to lab. This table will show all inputs and outputs at a given time t and the resulting outputs a short time later.
2. Cross-Coupled Set-Reset NOR Latch

- Analyze the circuit shown in Fig. 3 by constructing a transition table (explained in the textbook in Unit 11.2) summarizing the operation of the circuit, and construct a transition table before coming to lab. This table will show all inputs and outputs at a given time $t$ and the resulting outputs a short time later.

![Figure 3. Cross-Coupled NOR Latch](image)

- Build the circuit shown in Fig. 3 and test it with different values for $S$ and $R$ and compare it to the transition table you created in your pre-lab.

- Demonstrate your circuit to your TA and have him/her sign your verification sheet.

3. Bounceless Switch

- Build a "bounceless" switch as shown in Fig. 4. Check for switch bounce by looking at the $X$ output on the oscilloscope when the switch is toggled. Save your debounced switch circuit for later parts of the lab.

- Note: A single-pole double-throw (SPDT) switch to drive A or B to ground may not be available. If that is the case, just use a grounded wire to drive A and B to ground to produce the same effect.

**Q5**: Explain why the circuit in Fig. 4 is called a “bounceless” or “debounced” switch.

![Figure 4. Debounced Switch](image)
4. **Positive-Edge-Triggered D Flip-Flop (D-FF) using the 74LS74A**

- Design the block labeled “Combinational Logic” and implement the entire circuit of Fig. 5. The combinational logic must generate a binary value of “1” (one) to drive the input of the first D-Flip Flop (D_a) only when \( Q_a = Q_b = Q_c = Q_d = 0 \)

Note that each 74LS74A Flip-Flop has a complementary output \( Q' \) in addition to \( Q \), that may be used to simplify your design.

- Connect an LED to each complementary output (\( Q' \)) using current-limiting resistors and connect your 1 Hz clock to the CLK input. Observe how the binary “1” injected by your Combinational Logic is transferred to the Q of each FF with each clock cycle.

- Now disconnect your clock and connect instead the “bounceless” switch of Fig. 4. Test your design again using your switch.

- Demonstrate your circuit to your TA and have him/her sign your verification sheet.

![Figure 5. Flip-Flop Ring](image)

**Lab Report**

In your report, answer **ALL** the questions in all parts of this handout. Be as complete and precise as possible. In addition, turn in your graded pre-lab and TA verification sheet.

**Grading**

<table>
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<tr>
<th>Component</th>
<th>Points</th>
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<tbody>
<tr>
<td>Prelab</td>
<td>20</td>
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<tr>
<td>Lab checkoff</td>
<td>50</td>
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<tr>
<td>Hazard shown on scope</td>
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<td>NOR/NAND S-R latch operation</td>
<td>(15)</td>
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<tr>
<td>D flip-flop Ring using debounced switch</td>
<td>(20)</td>
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<tr>
<td>Lab report</td>
<td>30</td>
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<tr>
<td>Answer all questions (Q1-Q5)</td>
<td>(20)</td>
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<tr>
<td>Meeting overall report guidelines</td>
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