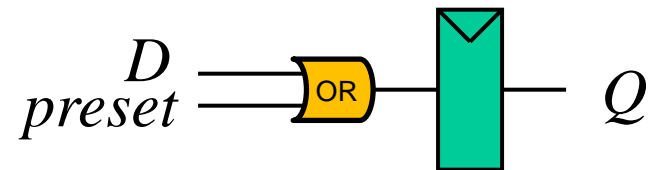
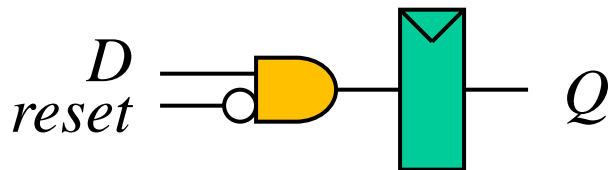


EEC 18
FLIP-FLOP SYNCHRONOUS
AND ASYNCHRONOUS
RESET AND PRESET

Single-bit Memories with Special *Reset* and *Preset* Inputs

- Sometimes it is convenient or necessary to have flip-flops with special inputs like *reset* and *preset*
- **Synchronous** *reset* and *preset* take effect only on the active edge of the clock (for a flip-flop)
- For robust design, normally use only synchronous *reset* and *preset* instead of asynchronous reset
- If a flip-flop with a built-in synchronous *reset* and/or *preset* is not available, they can be added to a plain D flip-flop with a circuit like the ones below



Asynchronous *Reset* and *Preset*

- An **asynchronous** *reset* or *preset* will take effect any time the input signal is asserted—even after a very short “glitch” in the middle of a clock period
- Such glitches are commonly generated from combinational logic, and capacitive coupling or inductive coupling of wires
- In normal usage, do not use flip-flops with asynchronous inputs
- However they are needed in specialized cases such as:
 - clock generation
 - asynchronous interface logic

