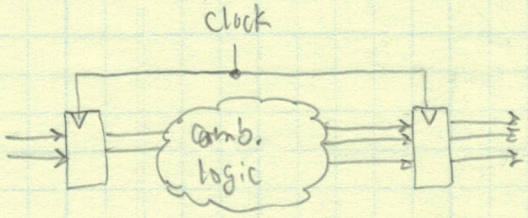
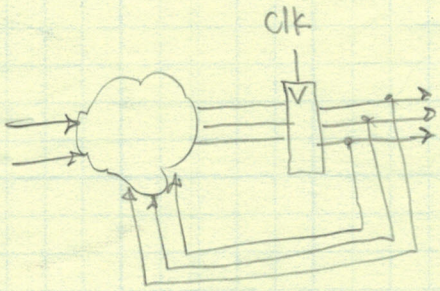
Critical Timing Relationships

If these are violated, the circuit will definitely fail under some circumstances.

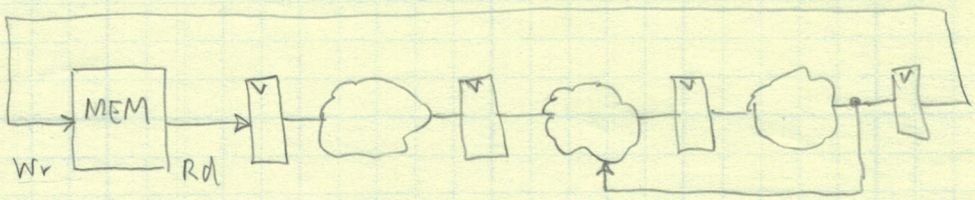
Fundamental block of every clocked digital system:



- FSM control, datapath, anything
- could also use latches, but we use FFs



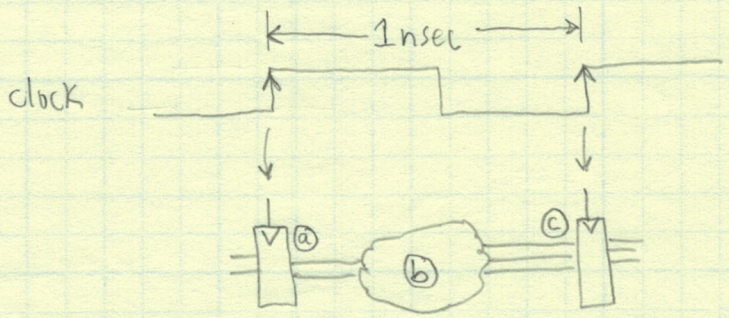
- could be the same register for both sides



Requirement #1: Logic is not too slow (clock not too fast)

Ex: 1 GHz clock

clock period = $1/\text{freq} = 1/10^9\ \text{Hz} = 10^{-9}\ \text{sec} = 1\ \text{nsec}$



- There is one clock period for data to get from one register to the next one.

a) clock edge → Q output — $t_{clk\text{-}to\text{-}q}$

b) time for the slowest path through the comb. logic — $t_{logic_{max}}$

c) time to arrive before the active clock edge — t_{setup}

∴ time circuit requires ≤ time allowed, for correct operation

$$t_{clk\text{-}to\text{-}q} + t_{logic_{max}} + t_{setup} \leq t_{cycle}$$

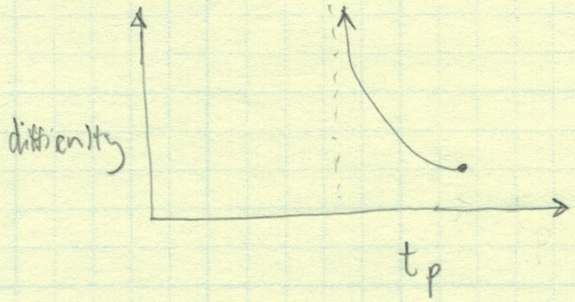
$$\leq 1/\text{freq}$$

What if the requirement is violated?

A) Design time

- speed up logic

but...



B) After chip is built.

- only t_{cycle} is available

slow f_{clk} → longer t_{cycle}

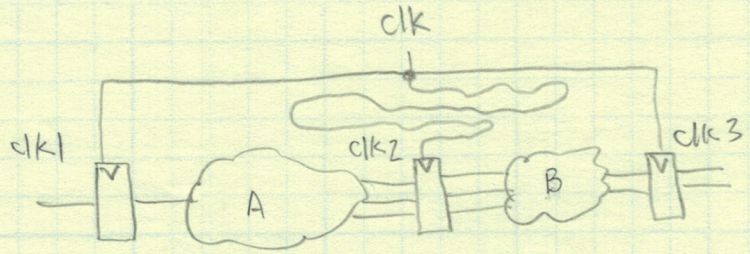
i) product - maybe ok

1.9 GHz proc instead of 2.0 GHz ✓

59 frames per second vs. 60 fps ✗

ii) research - probably fine

Equation assumes clocks are perfectly aligned.



What if clk2 is 0.1 ns late compared to clk1 and clk3 ?

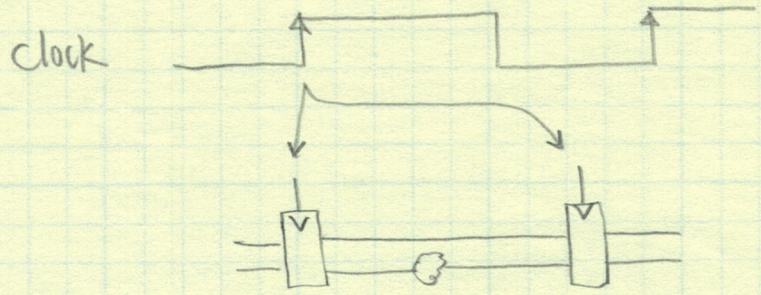
$$t_{cycle_A} = 1.0ns + 0.1ns = 1.1ns$$

$$t_{cycle_B} = 1.0ns - 0.1ns = 0.9ns$$

$\therefore$ For a simple analysis,

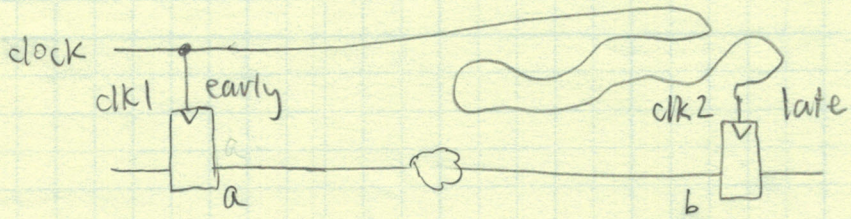
$$t_{cycle_{avail}} = \frac{1}{freq_{clk}} - \left| t_{clk\text{-}skew_{worst\ case}} \right|$$

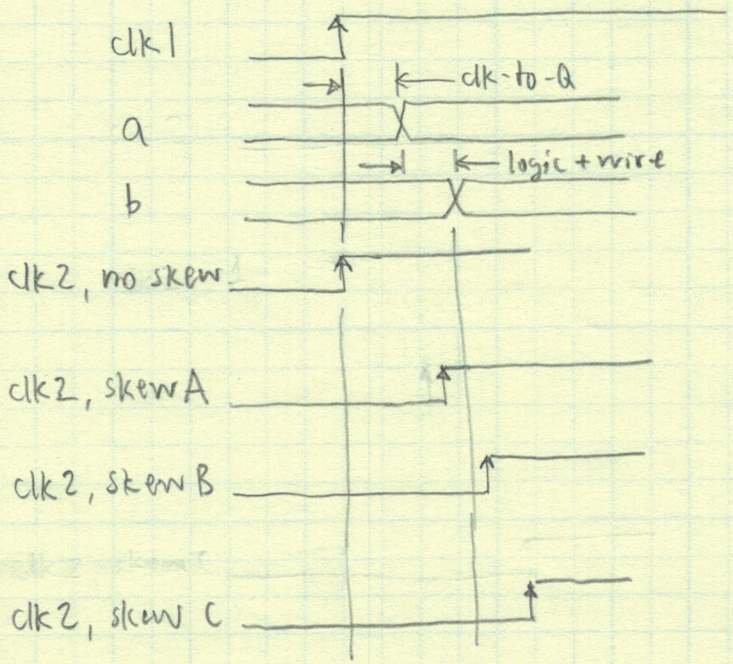
Requirement #2 : Logic is not too fast



Enabled by clock skew which is the difference in arrival times between clock signals

This failure occurs when the second downstream clock is late w.r.t. to the first upstream clock.



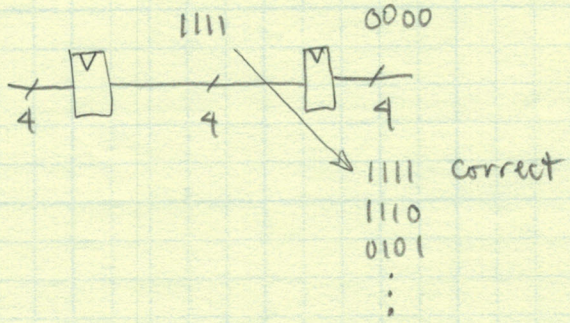


Hold time violation

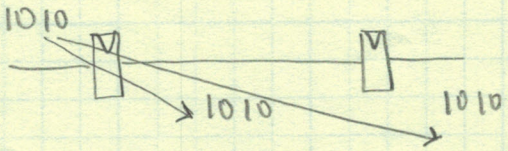
Fail, possible race through, setup time violation

Fail, race through

- Timing violations make function fail or unreliable



- Race through in worst case



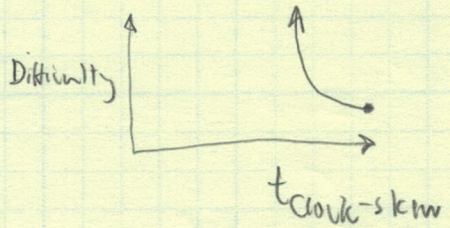
$$t_{clk\text{-}to\text{-}Q} + t_{logic\ min} > t_{clk\text{-}skew} + t_{hold}$$

for correct operation

What if the requirement is violated?

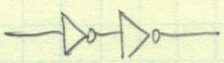
A) Design time

- lower clock skew



- increase $t_{logic\ min}$

Very easy!

Add slow circuits 

B) After chip is built

- no terms are a function of f_{clock} "

- no fixes possible!

∴ Hold time violations are very dangerous!