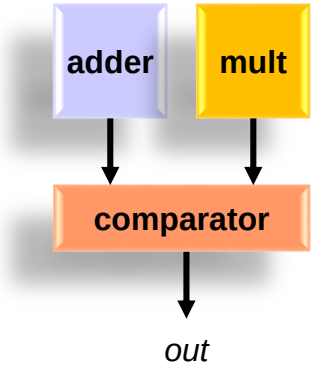
7 BASIC DIAGRAMS

Basic Diagrams

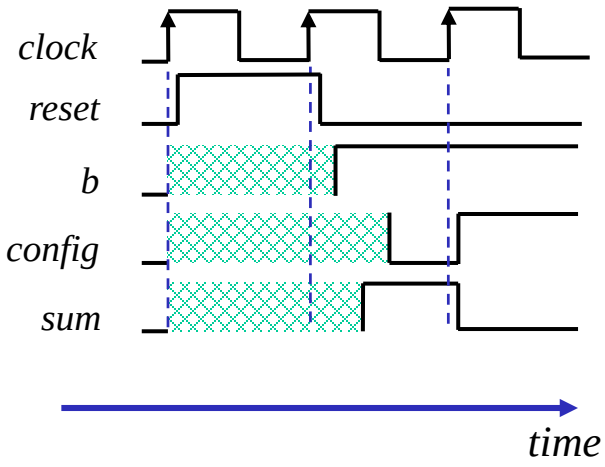
1. Block diagram
   - Just like it says; diagram of blocks (and inter-connections)

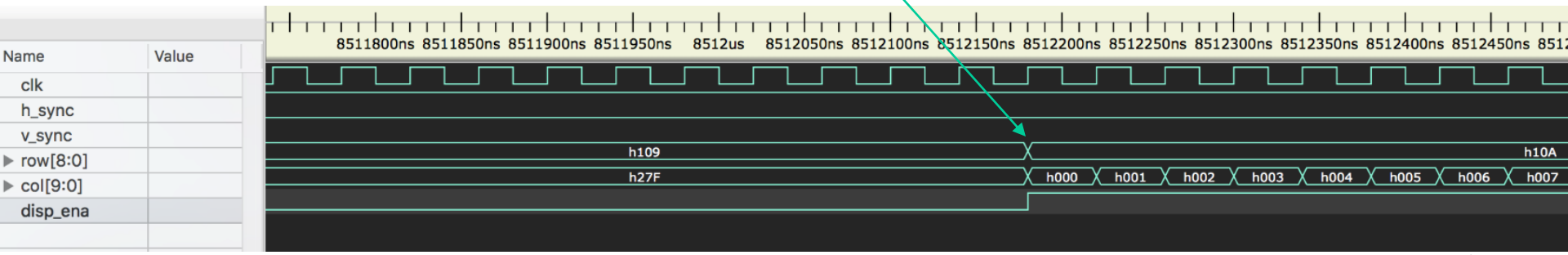


2. Circuit diagram
   - Although it may not require details to the transistor level or gate level (e.g., NAND or NOR), it should have more circuit-type details if applicable
   - Having said that, in some cases it may be the same as a block diagram

Basic Diagrams

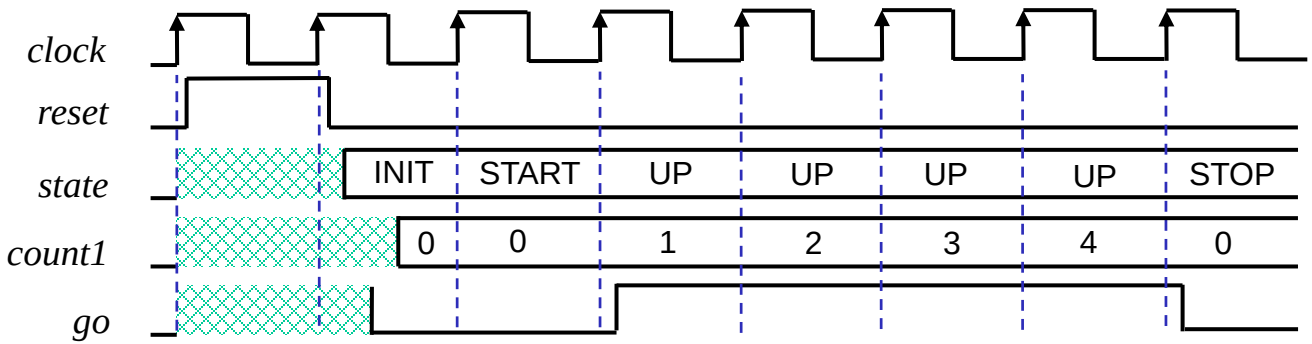
3. Timing diagram
   - Logic level (voltage) versus time
   - As a rule, the *clock* is at the top. Draw a small arrow on each active edge. Draw a light vertical line aligned with each active clock edge.
   - Several common waveform features:
     - Simple single-bit signal 0/1 values
     - Multi-bit bus
     - Transition location or region where a signal, or signal(s) within a bus, changes value





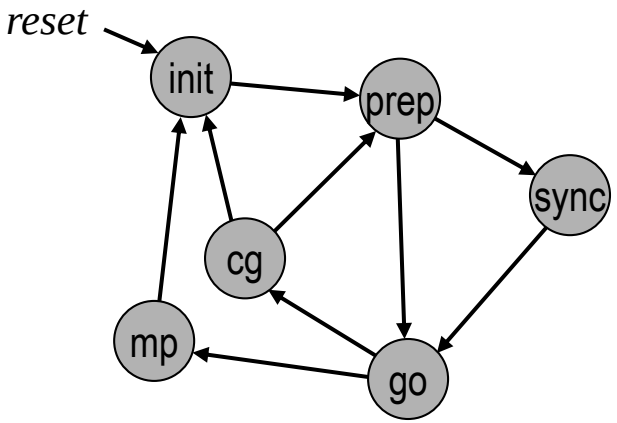
Basic Diagrams

3. Timing Diagram continued
   - Draw transitions of signals that come from a register a very short time after the active edge of the clock, not at the same time as the clock edge—this is for increased clarity however it also explicitly shows the "*clock-to-Q* delay"
   - Timing diagrams may also show higher-level events such as state and counter values

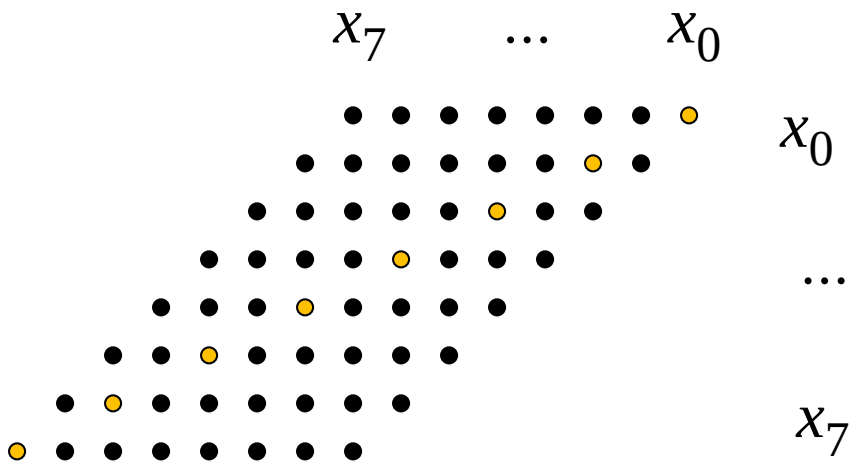


Basic Diagrams

4. State Diagram

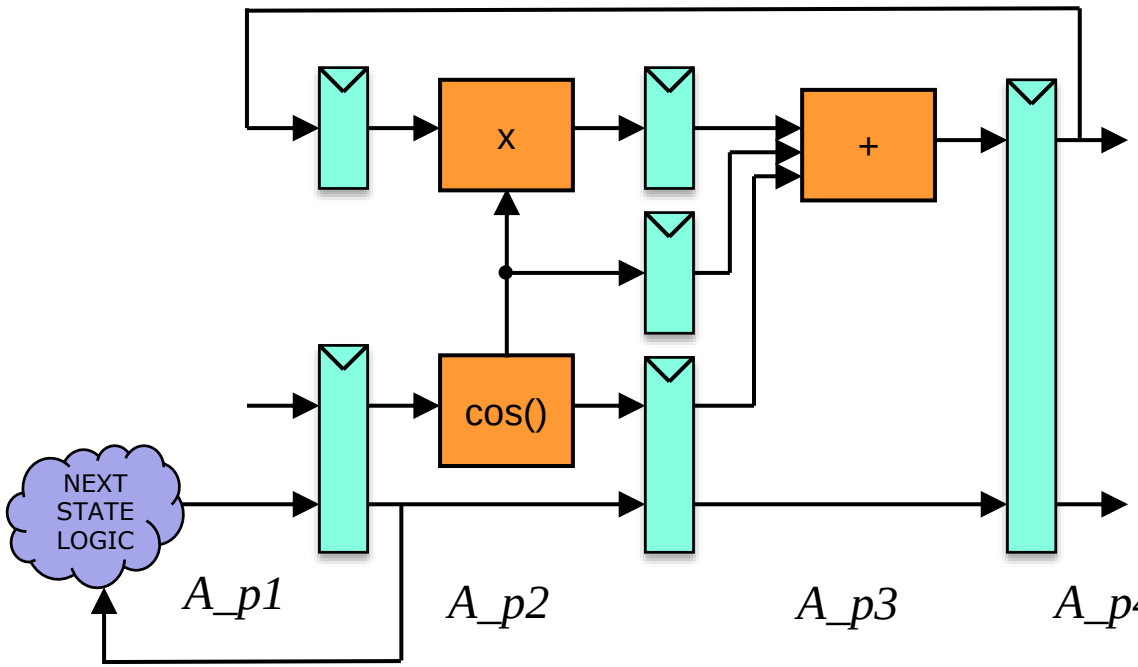


5. Arithmetic Dot Diagrams



Basic Diagrams

6. Pipelined Block Diagram
   - All registers are aligned with others in the same pipeline stage
   - "Reverse-flowing" signals are generally not pipelined
   - It is often advisable to include a pipeline-stage notation in each signal's name



Counter or Finite State Machine

Basic Diagrams

7. Pipeline Diagram
   - Useful for designing deeply-pipelined digital processors