

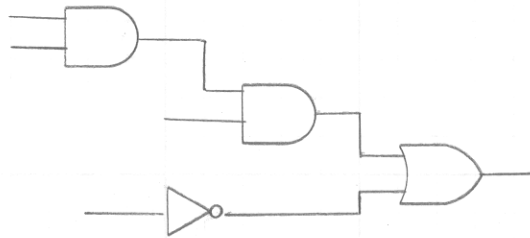
7.1 Multi-Level Gate Circuits

Level of a circuit \equiv maximum number of gates in series between input and output

Sum-of-Products : 2 level circuit (AND-OR)

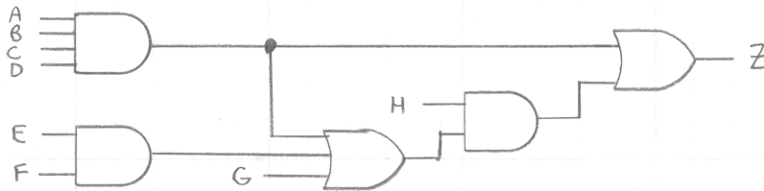
Product-of-Sums : 2 level circuit (OR-AND)

Ex:



3 level circuit

Ex: $Z = (ABCD + EF + G)H + ABCD$



4 level circuit

Why does level matter?

1. Multi-level may have fewer gates
2. Limited number of inputs per gate (i.e., limited fanin).
3. Limited number of loads (gates) connected to the output of a gate (limited fanout).
4. Delay: a change in the input variable value takes time to induce a change in the output value (propagation delay). A circuit can't run faster than its slowest path.

Ex: Suppose each gate has a propagation delay of 100ps. The slowest delay for the circuit for Z above takes 400ps.

7.2 NAND and NOR Gates

A logic gate (or gates) is/are functionally complete if they are able to generate any Boolean function.

Operators for minterm expansions are functionally complete (AND, OR, NOT)
 Operators for maxterm expansions are functionally complete (OR, AND, NOT)

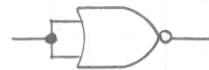
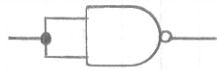
AND is not functionally complete ($A \cdot A \not\Rightarrow A'$)
 OR " " " " ($A + A \not\Rightarrow A'$) } can't generate inverse.

NOT (inverter) is not functionally complete - can't generate two input operations.

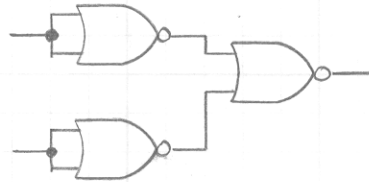
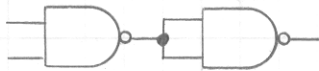
NAND } are functionally complete.
 NOR }

Difficult to prove directly, but easier to say that we can generate any function by its minterm/maxterm expansion using AND, OR, NOT, and then implement these using NAND / NOR:

NOT:

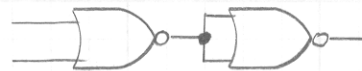
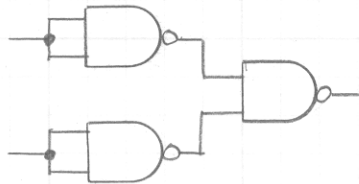


AND:



(De Morgan)

OR:

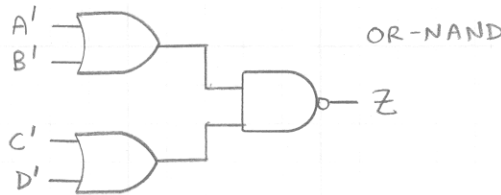
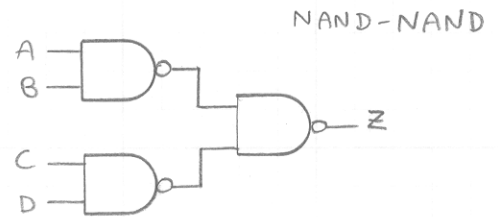
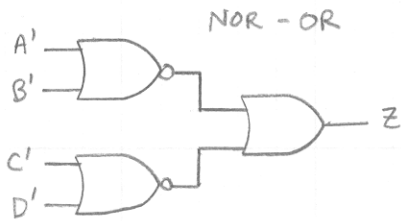
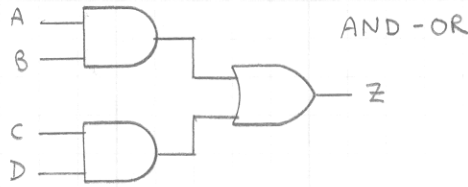


(De Morgan)

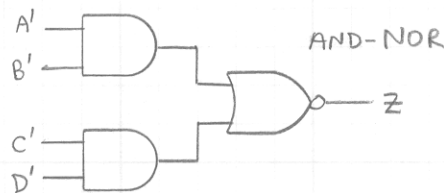
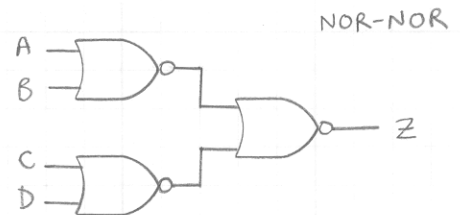
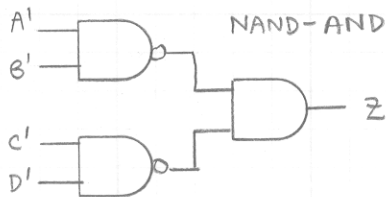
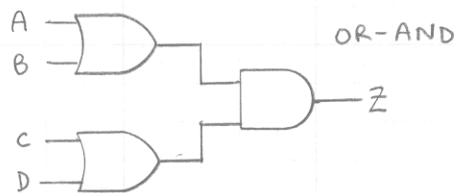
∴ NAND / NOR are functionally complete.

Moving Between Different Types of Two Level Circuits

Starting with Sum-of-Products:



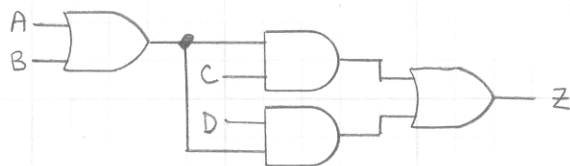
Starting with Product-of-Sums:



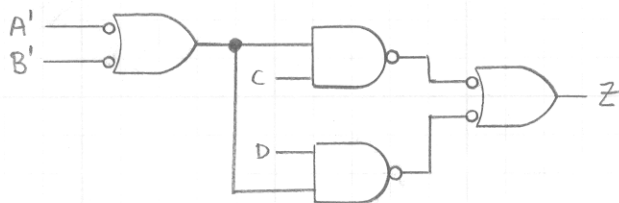
13-782 500 SHEETS, FILLER 5 SQUARE
 42-381 50 SHEETS, FILLER 5 SQUARE
 42-382 100 SHEETS, FILLER 5 SQUARE
 42-383 100 SHEETS, FILLER 5 SQUARE
 42-384 100 SHEETS, FILLER 5 SQUARE
 42-385 100 SHEETS, FILLER 5 SQUARE
 42-386 100 SHEETS, FILLER 5 SQUARE
 42-387 100 SHEETS, FILLER 5 SQUARE
 42-388 100 SHEETS, FILLER 5 SQUARE
 42-389 100 SHEETS, FILLER 5 SQUARE
 42-390 100 SHEETS, FILLER 5 SQUARE
 42-391 100 SHEETS, FILLER 5 SQUARE
 42-392 100 SHEETS, FILLER 5 SQUARE
 42-393 100 SHEETS, FILLER 5 SQUARE
 42-394 100 SHEETS, FILLER 5 SQUARE
 42-395 100 SHEETS, FILLER 5 SQUARE
 42-396 100 SHEETS, FILLER 5 SQUARE
 42-397 100 SHEETS, FILLER 5 SQUARE
 42-398 100 SHEETS, FILLER 5 SQUARE
 42-399 100 SHEETS, FILLER 5 SQUARE
 42-400 100 SHEETS, FILLER 5 SQUARE
 Made in U. S. A.



Ex: Multi-level NAND



OR-AND-OR form



Convert using DeMorgan's Law and $X'' = X$ identity

Ex: Find minimum 3 level NOR circuit that implements

$$f = a'b' + abd + acd$$

cd \ db	00	01	11	10
00	1	0	0	0
01	1	0	1	0
11	1	0	1	1
10	1	0	0	0

f

cd \ db	00	01	11	10
00	0	1	1	1
01	0	1	0	1
11	0	1	0	0
10	0	1	1	1

f'

Want NOR-NOR-NOR circuit,

1) Find AND-OR-AND circuit \rightarrow find OR-AND circuit then factor using $(X+Y)(X+Z) = X+YZ$

To find OR-AND (Product-of-Sums), use K-map for f':

$$f' = a'b + ad' + ab'c'$$

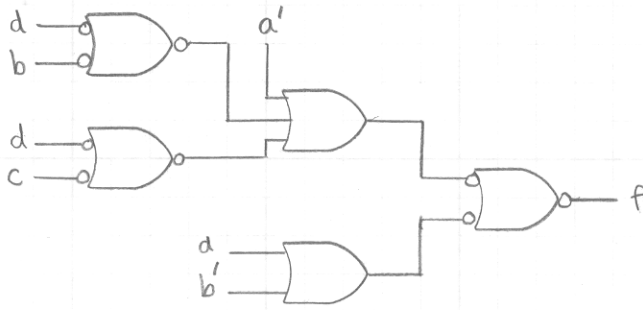
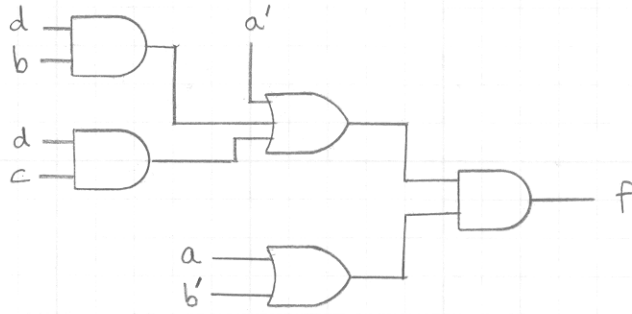
$$f = f'' = (a+b')(a'+d)(a'+\underbrace{b+c})$$

$\underbrace{\hspace{1cm}}_{X=a'} \quad \underbrace{\hspace{1cm}}_{y=d} \quad \underbrace{\hspace{1cm}}_{z=b+c}$

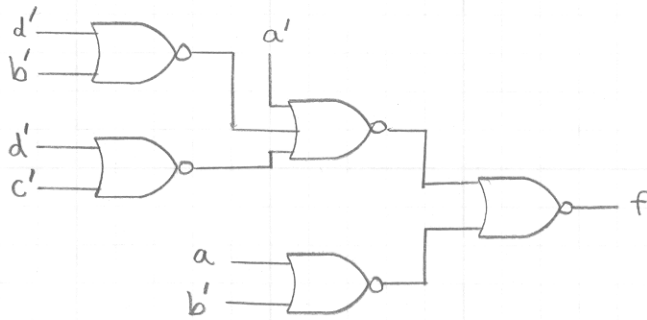
$$f = (a+b')(a'+d(b+c)) \quad 4 \text{ levels}$$

$$= (a+b')(a'+db+dc) \quad 3 \text{ levels}$$





Replace AND with NOR
equivalents (De Morgan's
Laws)



13-782 500 SHEETS, FILLER, 5 SQUARE
42-381 50 SHEETS EYE-EASE, 5 SQUARE
42-382 100 SHEETS EYE-EASE, 5 SQUARE
42-383 200 SHEETS EYE-EASE, 5 SQUARE
42-392 100 RECYCLED WHITE, 5 SQUARE
42-399 200 RECYCLED WHITE, 5 SQUARE
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