

**11.1 Introduction**

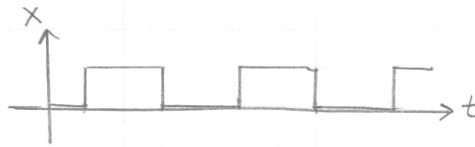
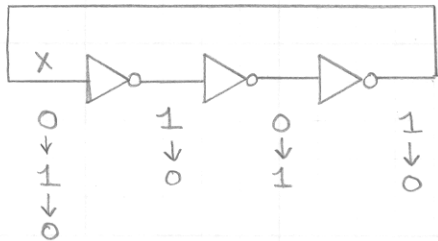
Sequential circuits: output depends on present and past values of inputs (circuit "remembers")

Latches and flip-flops are common memory devices used in sequential circuits

Memory is implemented using feedback with combinational gates:

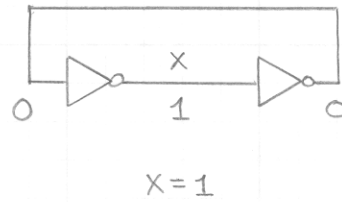
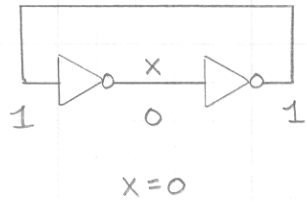
Odd number of inverters (Lab 2)

Analyze by assuming value on a node and propagating values to other nodes:



Even number of inverters

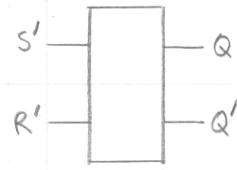
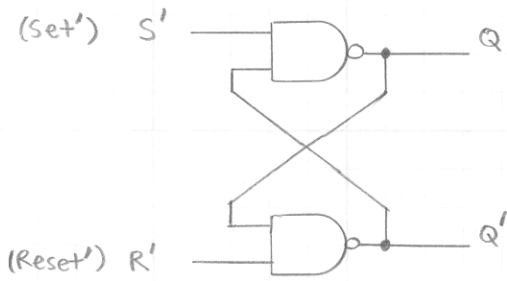
Two stable states:



Circuit "remembers" previous value (once  $X=0$ ,  $X$  stays 0 until some external action changes it)

**11.2 Set-Reset Latch**

SR Latch (NAND Latch)

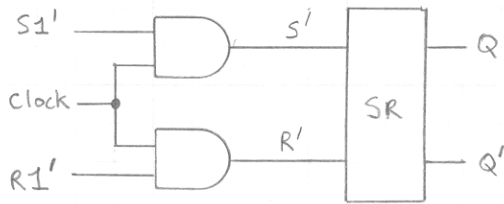


13-782 500 SHEETS FILLER 5 SQUARE  
 42-381 50 SHEETS EYE-EASE 5 SQUARE  
 42-382 100 SHEETS EYE-EASE 5 SQUARE  
 42-383 100 SHEETS EYE-EASE 5 SQUARE  
 42-389 100 RECYCLED PAPER 5 SQUARE  
 42-390 100 RECYCLED PAPER 5 SQUARE  
 42-399 200 RECYCLED WHITE 5 SQUARE  
 Made in U.S.A.

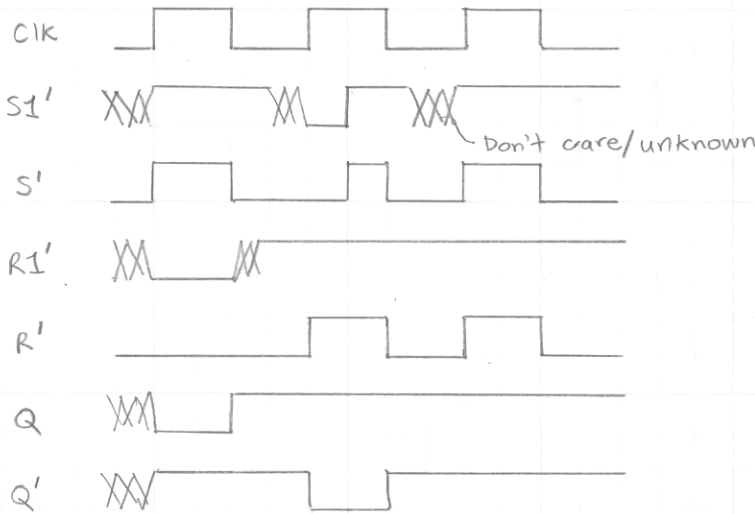


S'	R'	Q	New Q
0	0	0	1 (Q'=0)
0	0	1	1 (Q'=0)
0	1	0	1 } set
0	1	1	1 } set
1	0	0	0 } reset
1	0	1	0 } reset
1	1	0	0 } no change (remember)
1	1	1	1 } no change (remember)

Clocked SR Latch



Clock (CLK) ≡ a periodic waveform used to control sequential circuit timing

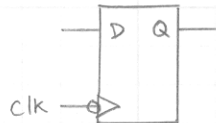


11.4 Edge Triggered D Flip-Flop

D Flip-Flop: has two inputs, D (data) and CLK (clock). Output only changes in response to transitions on CLK



Rising Edge Triggered

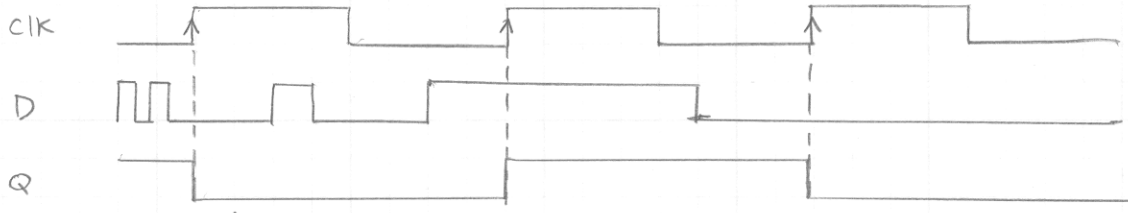


Falling Edge Triggered

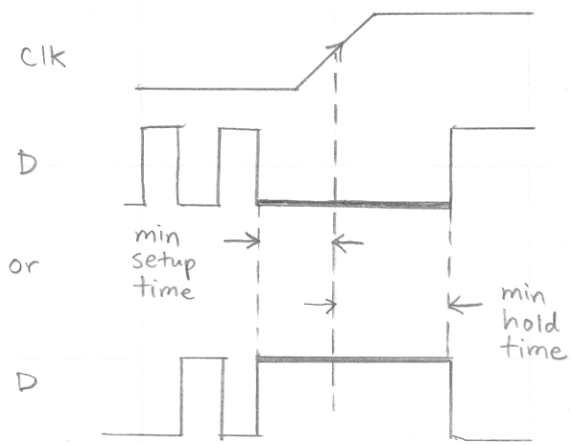
D	Q	New Q
0	0	0
0	1	0
1	0	1
1	1	1

Truth Table





Zoom in on positive edge



Setup Time : input must not change before clock edge

Hold Time : input must not change after clock edge

Setup and hold time constraints must be met for proper circuit operation.

13-762 500 SHEETS, FILLER, 5 SQUARE  
 42-361 50 SHEETS, EYE-EASE, 5 SQUARE  
 42-362 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-363 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-364 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-365 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-366 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-367 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-368 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-369 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-370 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-371 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-372 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-373 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-374 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-375 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-376 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-377 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-378 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-379 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-380 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-381 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-382 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-383 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-384 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-385 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-386 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-387 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-388 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-389 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-390 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-391 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-392 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-393 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-394 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-395 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-396 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-397 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-398 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-399 100 SHEETS, EYE-EASE, 5 SQUARE  
 42-400 100 SHEETS, EYE-EASE, 5 SQUARE  
 Made in U.S.A.

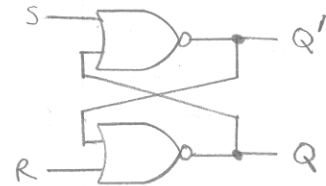
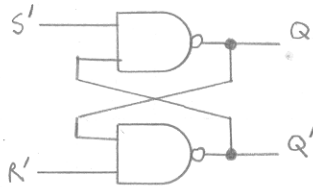
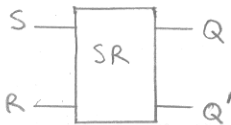


Latches and Flip-Flops Review

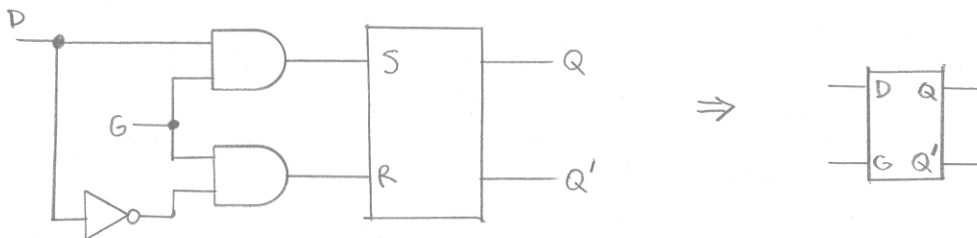
Flip-flop: Memory element whose output changes on the active edge of a special input (clk)

Latch: Memory element whose output changes on the active level of a special input (e.g., gated latch) or at any time (e.g., SR latch)

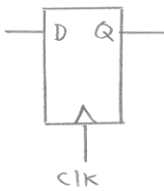
SR Latches



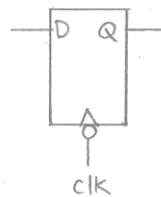
Gated Latches (Transparent Latches)



D Flip-Flop



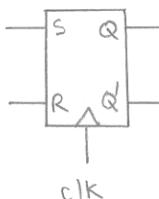
a) positive edge-triggered



b) negative edge-triggered

Must meet setup and hold time requirements for correct operation

SR Flip-Flop



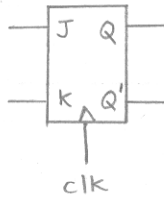
S	R	Q <sup>+</sup>
0	0	memory (Q <sup>+</sup> = Q)
0	1	reset (Q <sup>+</sup> = 0)
1	0	set (Q <sup>+</sup> = 1)
1	1	invalid

Q<sup>+</sup> ≡ next Q state

22-141 50 SHEETS  
22-142 100 SHEETS  
22-144 200 SHEETS

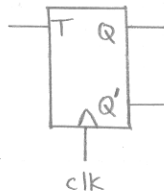


JK Flip-Flop



J	K	Q+
0	0	memory ( $Q^+ = Q$ )
0	1	reset ( $Q^+ = 0$ )
1	0	set ( $Q^+ = 1$ )
1	1	toggle Q ( $Q^+ = Q'$ ), i.e. $0 \rightarrow 1$ or $1 \rightarrow 0$ )

T Flip-Flop



T	Q+
0	memory ( $Q^+ = Q$ )
1	toggle Q ( $Q^+ = Q'$ )

22-141 50 SHEETS  
22-142 100 SHEETS  
22-144 200 SHEETS



Other Inputs

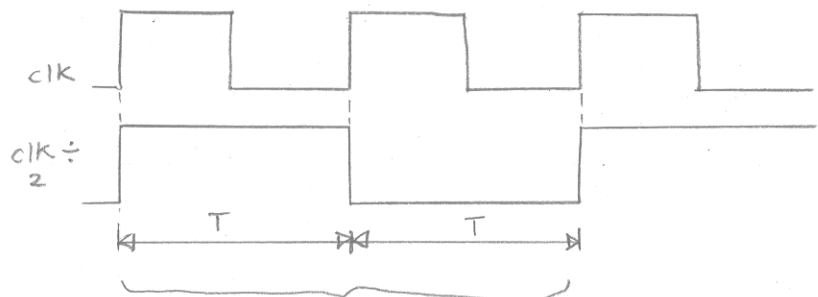
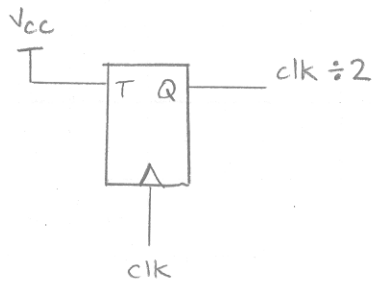
Asynchronous: without regard to the clock signal

Synchronous: effective only on an active clock edge

Ex: Four combinations to initialize value stored in a flip-flop:

	Clear (reset)	Set
Asynchronous	X	X
Synchronous	X	X

Ex: Flip-flops can be used to divide a clock (generate a clock at a lower frequency):



Old period = T, New period = 2T

We can cascade multiple T flip-flops to produce  $clk \div 4$ ,  $clk \div 8$ , etc. Lab 6 uses clock division on the Altera board.