EEC 18

Nov. 30

State Table:

P.S.		N.S. X=0	N.S. X=1	output z X=0	output z X=1
begin	S_0	S_1 ✓	S_4	0	0
"0"	S_1	S_1 ✓	S_2	0	0
"01"	S_2	S_5	S_3	0	0
"011"	S_3	S_5	S_4	1	0
"1"	S_4	S_5	S_4	0	0
"10"	S_5	S_1 ✓	S_2	0	1

Num of FFs: minimal = $\lceil \log_2(6) \rceil$

= 3 FFs

Guideline I.

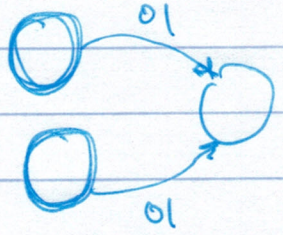
N.S.

✓ (S_0, S_1, S_5) S_1 for X=0

✓ (S_2, S_3, S_4) S_5 X=0

✓ (S_0, S_3, S_4) S_4 X=1

✓ (S_1, S_5) S_2 X=1



Guideline II

× N.S. of $S_0 = (S_1, S_4)$

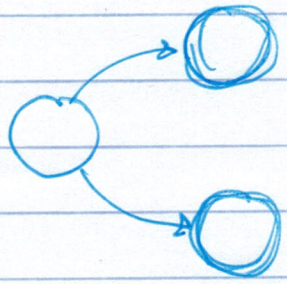
✓ $S_1 = (S_1, S_2)$

× $S_2 = (S_5, S_3)$

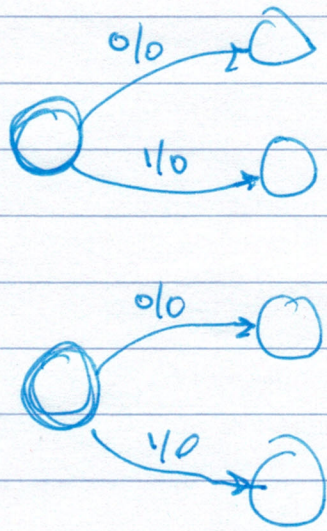
✓ $S_3 = (S_5, S_4)$

✓ $S_4 = (S_5, S_4)$

✓ $S_5 = (S_1, S_2)$



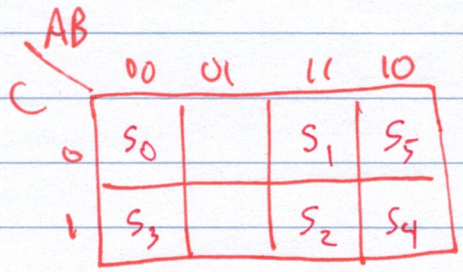
Guideline III

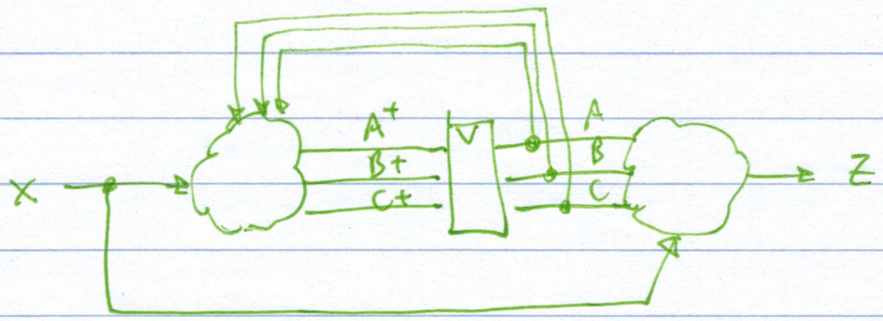


$(S_0, S_1, S_2, S_4) \rightarrow Z=0 \quad X=0,1$

$(S_0, S_1, S_2, S_4, S_5) \rightarrow Z=0 \quad X=0$

$(S_0, S_1, S_2, S_3, S_4) \rightarrow Z=0 \quad X=1$

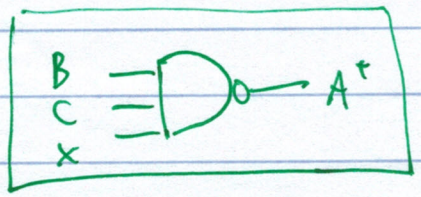




	P.S. ABC	N.S. $A^+B^+C^+$ X=0	N.S. $A^+B^+C^+$ X=1	output Z X=0	output Z X=1
S_0	000	110	101	0	0
S_3	001	100	101	1	0
X	010	xxx	xxx	x	x
X	011	xxx	xxx	x	x
S_5	100	110	111	0	1
S_4	101	100	101	0	0
S_1	110	110	111	0	0
S_2	111	100	001	0	0

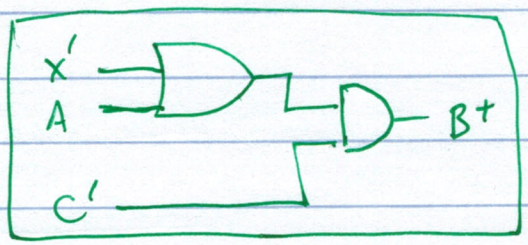
$A^{+\prime} = BCx$

$A^{+} = \overline{(B \cdot C \cdot x)}$

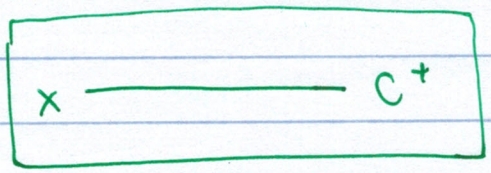


$B^{+} = C'x' + AC'$

$= C'(x' + A)$

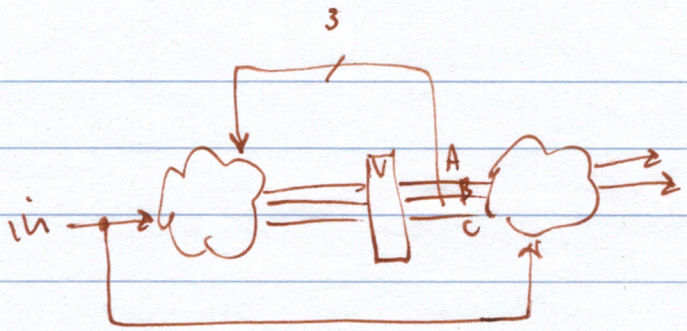


$C^{+} = x$



$Z = AB'C'x + A'Cx$

Unit 16

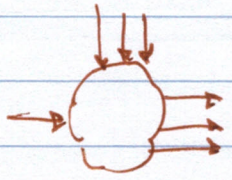


Use a ROM for FSM logic

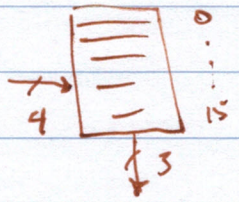
- more area than gates
+ highly flexible

Example above:

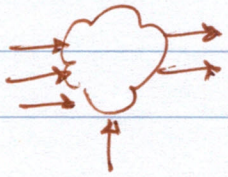
- N.S. logic



4 inputs → 16-word × 3-bit ROM



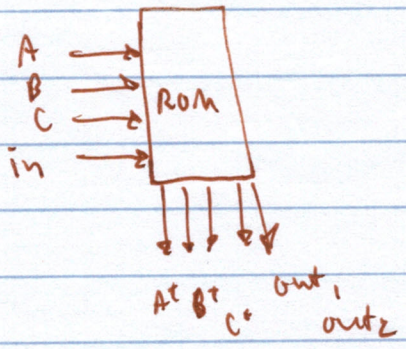
- output logic

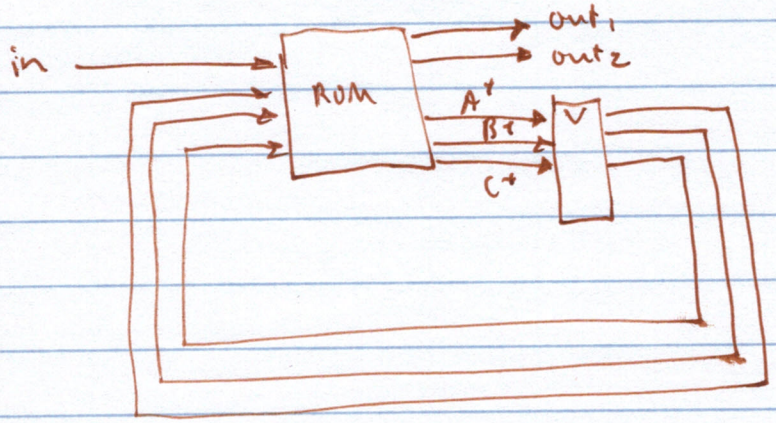


4 inputs → 16-word × 2-bit ROM

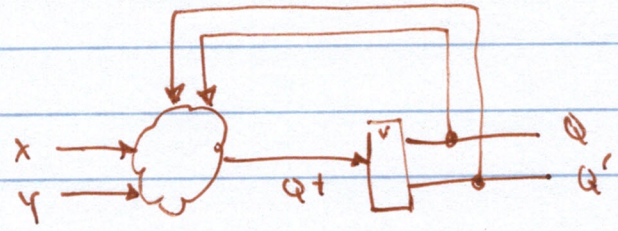
Notice both have inputs: A, B, C, in

→ merge two ROMs

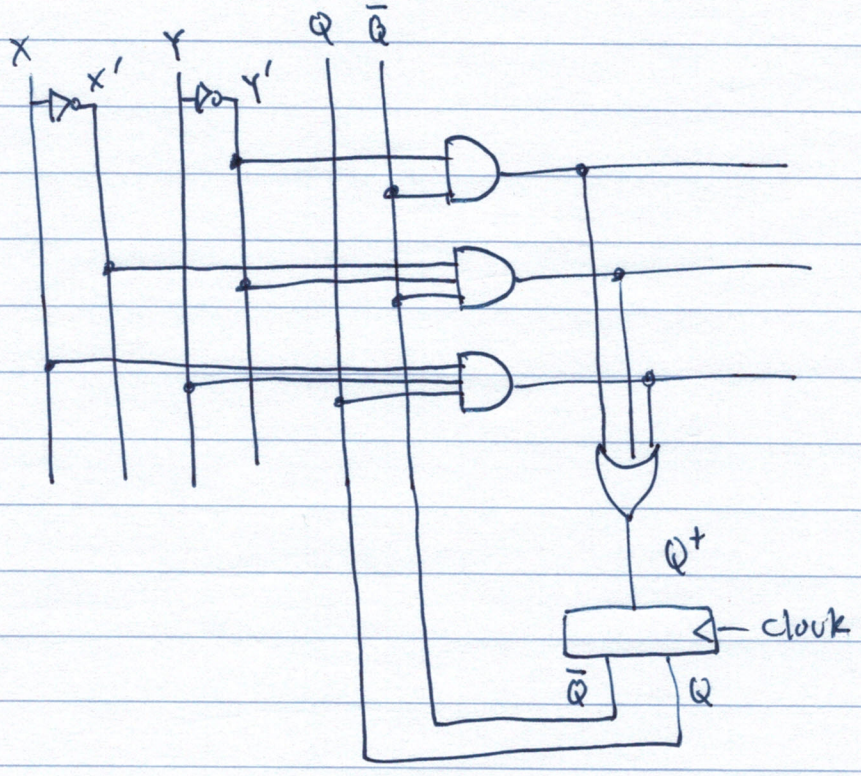




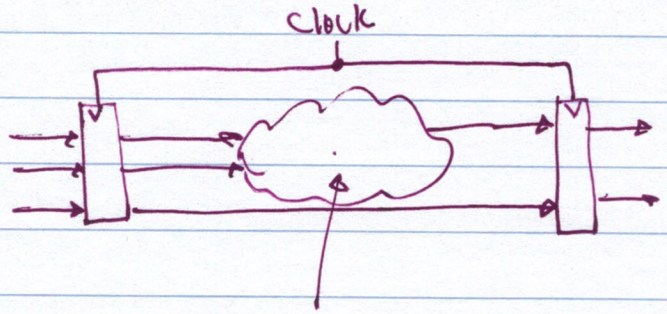
PLA



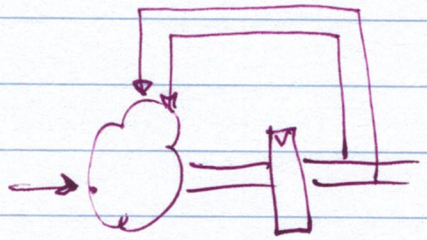
$$Q^+ = Y'Q' + X'Y'Q' + XYQ$$



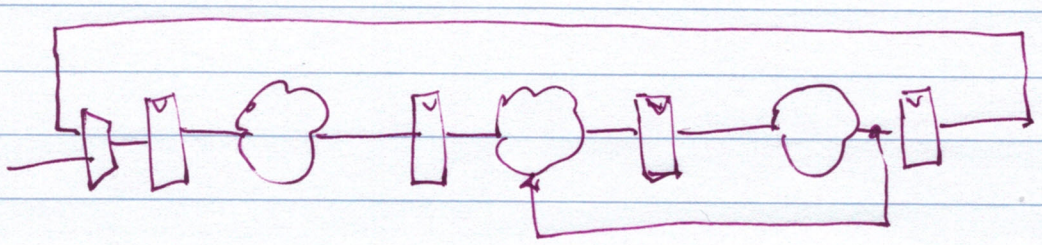
Critical Timing Relationships



datapath, FSM logic, anything



One reg is both upstream and downstream

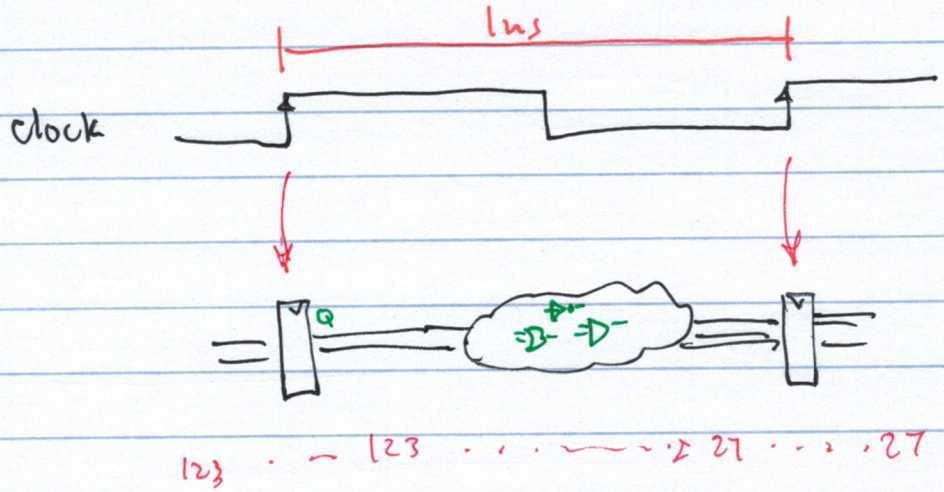


Requirement #1 - Logic may not be too slow
Clock not too fast

Ex. 1 GHz clock $= 10^9$ Hz

clock period $= 1/10^9$ Hz

$= 10^{-9}$ sec $=$ 1 nsec



- One clk period for data to move from one register to the next one

a) clk edge → Q output $t_{clk\text{-}to\text{-}q}$

b) time for slowest path thru comb. logic $t_{logic_{max}}$

c) before clk edge t_{setup}

∴ time circuit requires ≤ time allowed, for correct operation

$$t_{clk\text{-}to\text{-}Q} + t_{logic_{max}} + t_{setup} \leq t_{cycle}$$

$$\leq 1/freq$$