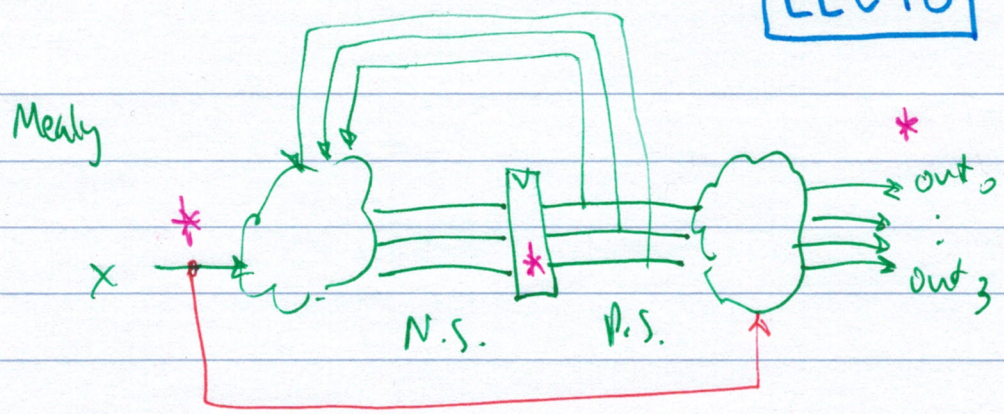
Nov. 23



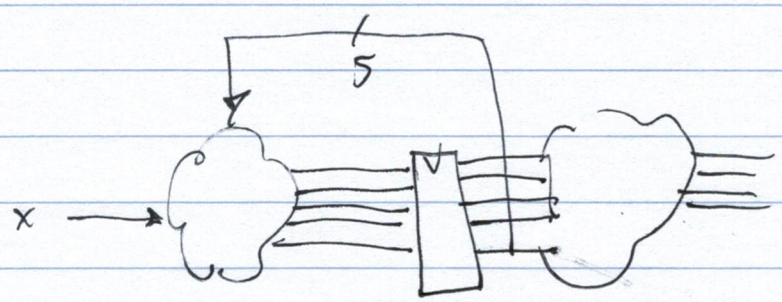
One-hot, Moore

- 9 states → 5 FFs

	P.S. $Q_4\ Q_3\ Q_2\ Q_1\ Q_0$	N.S. $X=0$	N.S. $X=1$
S_0	0 0 0 0 1	00010	01000
S_1	0 0 0 1 0	00100	01000
S_2	0 0 1 0 0	01000	01000
S_3	0 1 0 0 0	10000	01000
S_4	1 0 0 0 0	00001	01000

=

N.S. logic: 6 inputs! 64-box K-map!



N.S. logic

- When does Q_0^+ need to be "1"? S_4 AND $X=0$
- When in S_4? $Q_4 \cdot \bar{Q}_3 \cdot \bar{Q}_2 \cdot \bar{Q}_1 \cdot \bar{Q}_0$

Q_4

$$Q_0^+ = Q_4 \cdot \bar{X}$$

$$Q_1^+ = Q_0 \cdot \bar{X}$$

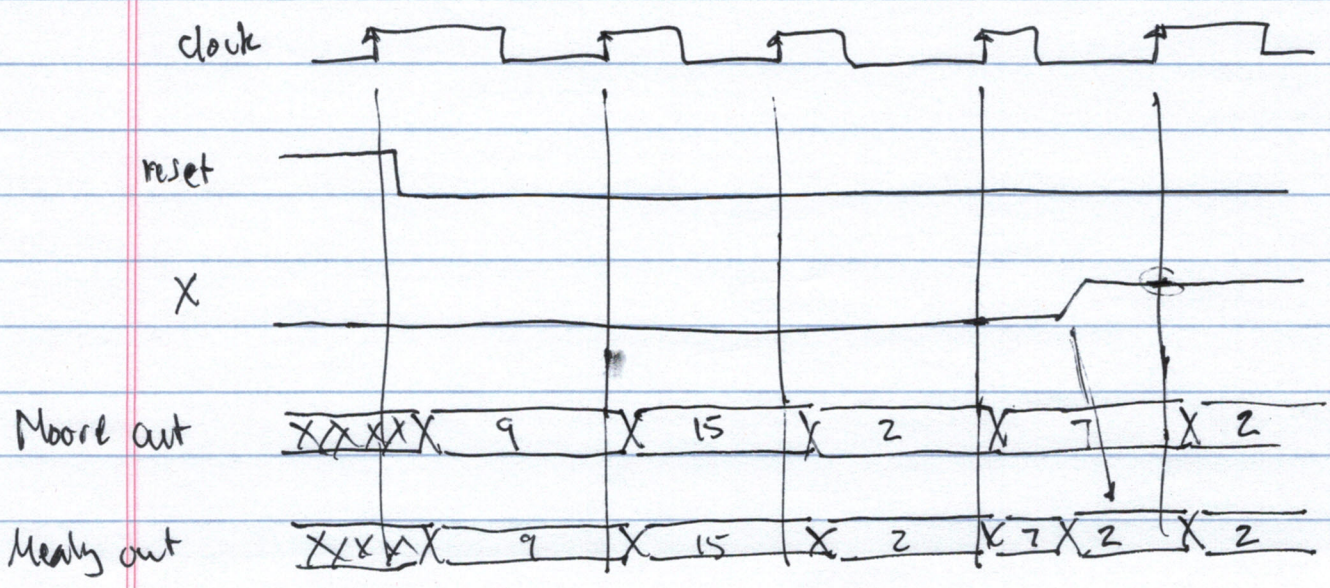
$$Q_2^+ = Q_1 \cdot \bar{X}$$

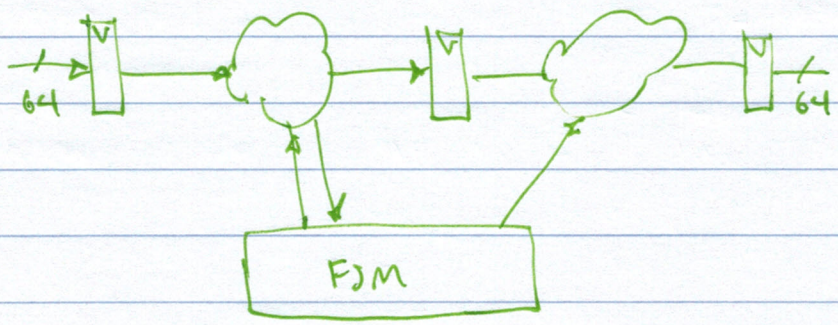
$$Q_3^+ = Q_2 \cdot \bar{X} + X$$

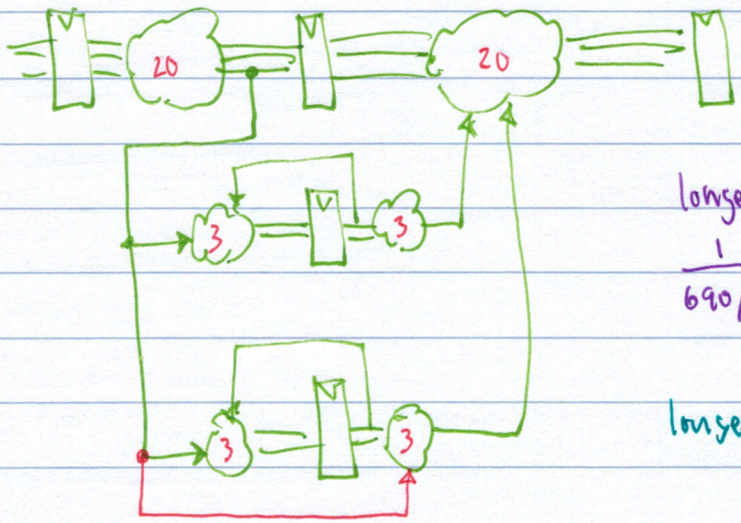
$$Q_3^+ = Q_2 + X$$

$$Q_4^+ = Q_3 \cdot \bar{X}$$

Compare Moore + Mealy







assume gate delay = 20 ps

Moore

longest path = 23 gate delays

$\frac{1}{690\,ps}$ = $f = 2.17$ GHz

Mealy

longest path = 43

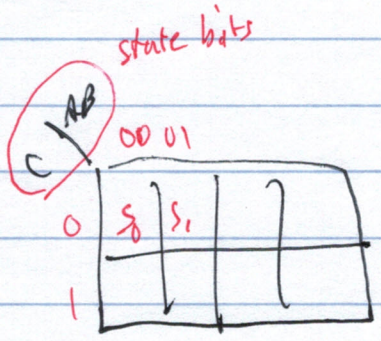
$f = 1.16$ GHz

Logic depth - longest delay between registers

~50 gate delays	long
~15-20	fast
~10	special processors designs

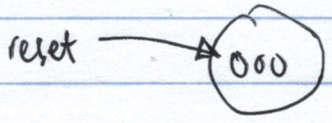
Guidelines for Efficient State Assignments

Idea: Use Kmap to assign states

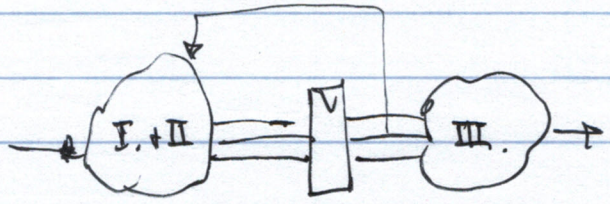


000 → 010

Often assign reset state to 000

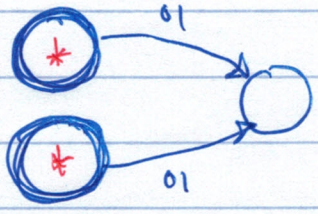


- One-hot : use preset also



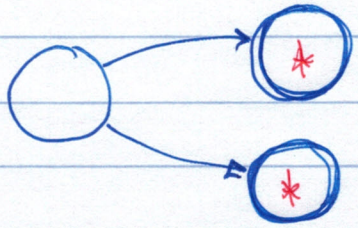
Guideline I.

Different P.S.
Same input → Same next state
} Group P.S.



Guideline II.

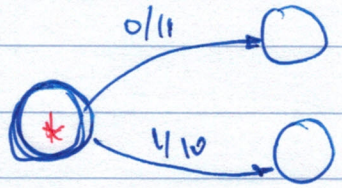
Different N.S. of one P.S.

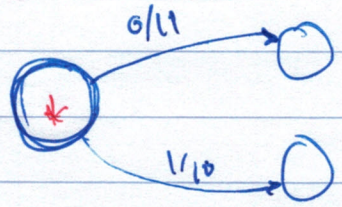


Guideline III

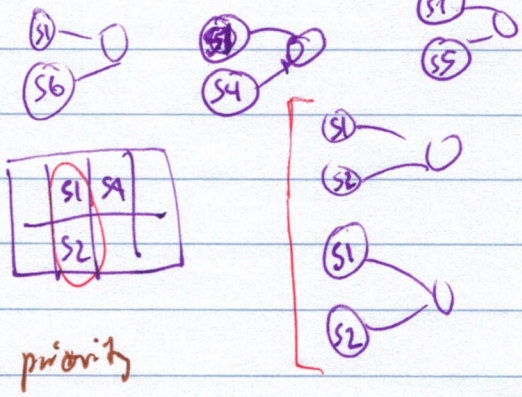
Different P.S.

Same outputs for all input combinations



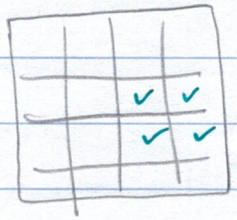


- No min soln guarantee
- Work best w/ D, JK



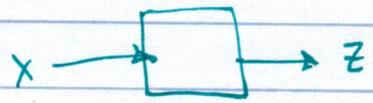
Guidelines of guidelines

- I. + II 2 or more times → high priority
- 3 or 4 states → group of 4 on K-map



- III lower priority
- I preference over II
- Favor N.S. vs. output depending on complexity

16.5 Sequence det., Mealy



$z = 1$ iff $X = \ldots 0110$

$X = \ldots 101$

$X = 0\,|\,0\,1\,|\,1\,0\,1$

$z = 0\,0\,0\,|\,0\,|\,1$

Q: What needs to be remembered?