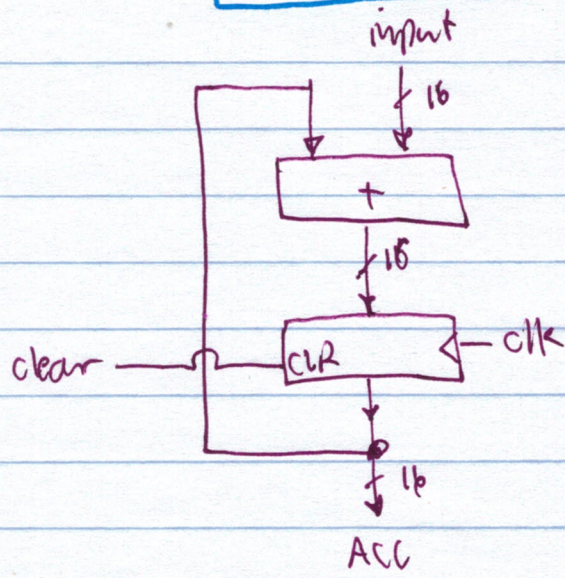
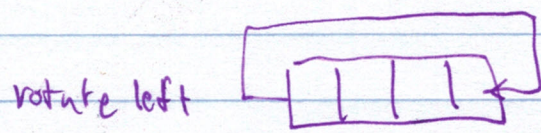
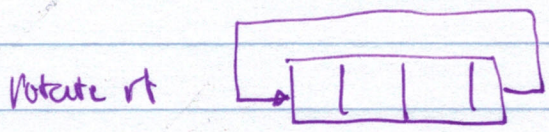
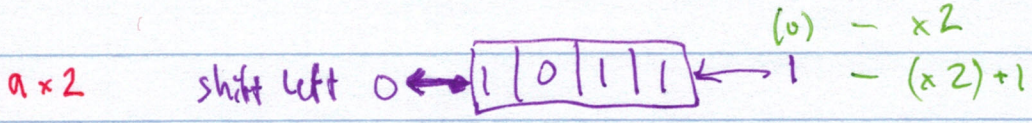
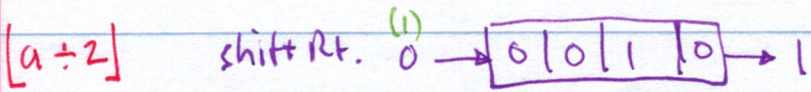
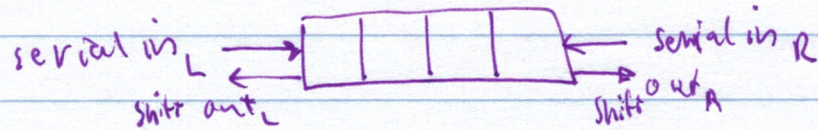


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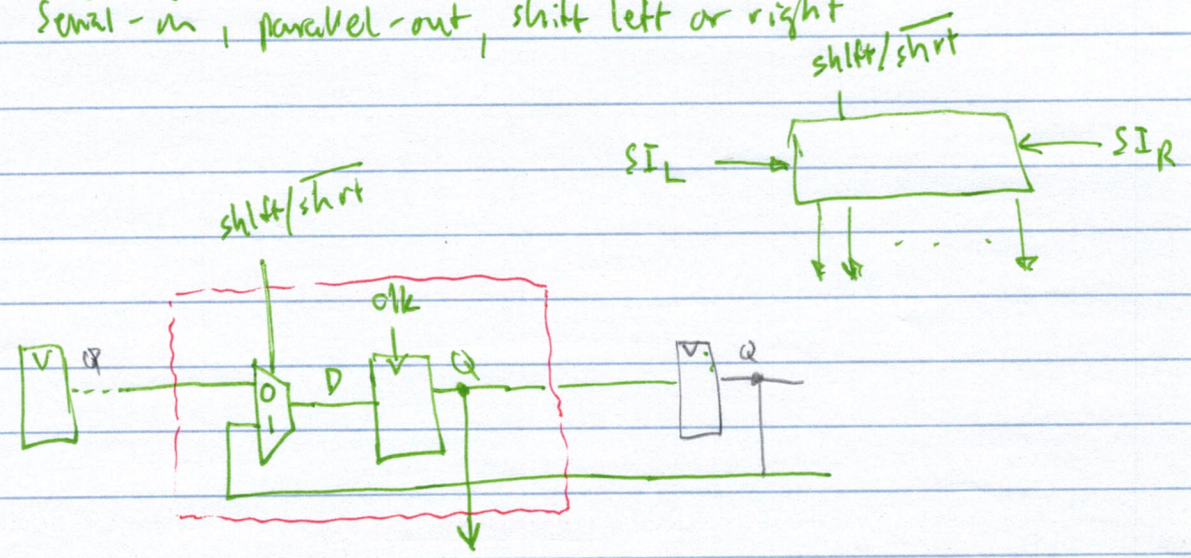
Shift Registers



- Updates on clock edge (FFs)
- Why would transp. latches be bad?

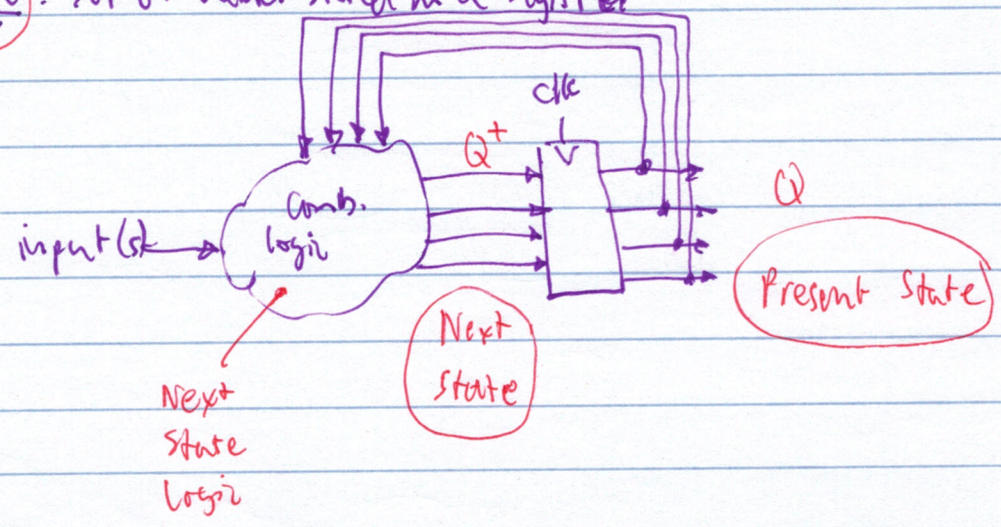
		Inputs	
		Serial	Parallel
Output	Serial	✓	✓
	Parallel	✓	✓

Ex: Serial-in, parallel-out, shift left or right



Binary Counters

state: set of values stored in a register

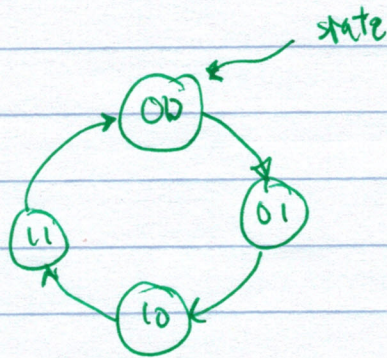


Ex: 2-bit counter

Sequence: 00, 01, 10, 11, 00, ...

$$\begin{array}{r} 11 \\ + 01 \\ \hline 00 \end{array}$$

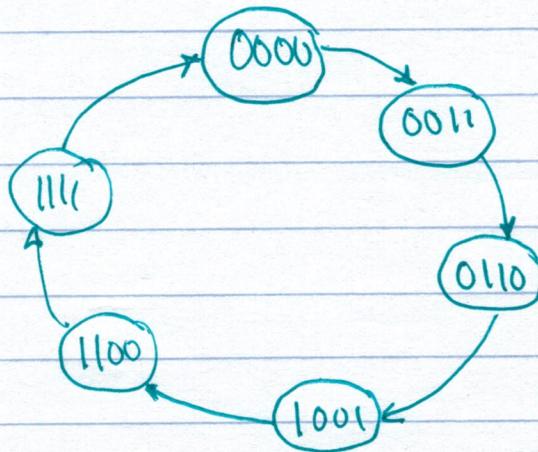
State Graph



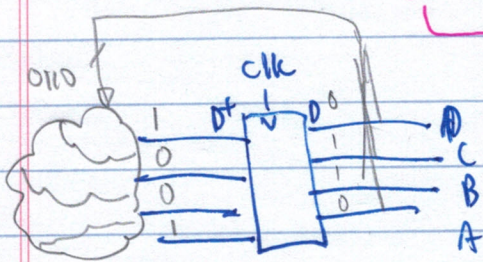
To design:

- 1) State graph or state sequence
- 2) For each P.S., write a corresponding N.S.
- 3) Determine the needed PF inputs
- 4) Design N.S. logic

Ex. 4-bit counter, incr. by 3, at 15 \rightarrow 0



Present state				Next state											
D	C	B	A	D ⁺	C ⁺	B ⁺	A ⁺	D _D	C _D	B _D	A _D	D _T	C _T	B _T	A _T
0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1
0	0	1	1	0	1	1	0	0	1	1	0	0	1	0	1
0	1	1	0	1	0	0	1	1	0	0	1	1	1	1	1
1	0	0	1	1	1	0	0	1	1	0	0	0	1	0	1
1	1	0	0	1	1	1	1	1	1	1	1	0	0	1	1
1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1



1) D_D

DC	00	01	11	10
0	0	x	0	x
01	x	x	x	1
10	1	x	0	x
11	x	1	x	x

$$D_D = \bar{B}D + B\bar{A}$$

$$D_D = \bar{B}D + \bar{A}C$$

- 2) D_C
- 3) D_B
- 4) D_A

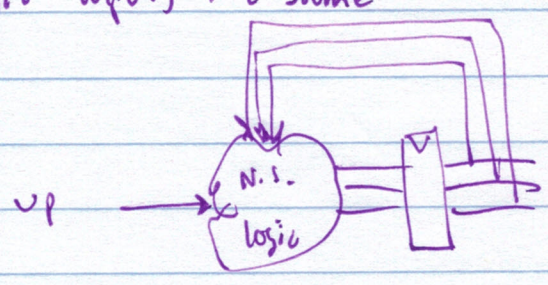
If we have additional inputs!

- count up / down
- reset

1) With multiple next states next to each other

P.S.	N.S. up = 1	N.S. up = 0
00	01	11
01	10	00
10	11	01
11	00	10

2) Consider all N.S. logic - inputs the same



up	P.S.	N.S.
0	00	11
0	01	00
0	10	01
0	11	10
1	00	01
	01	10
	10	11
	11	00

Reset input

- 1) Treat as any input
- 2) Use special FF inputs : reset set

- watch active high/low
- easiest method, if available

Ex: 2-bit counter, T FFs

$\bar{u}/dn = 0$
N.S.

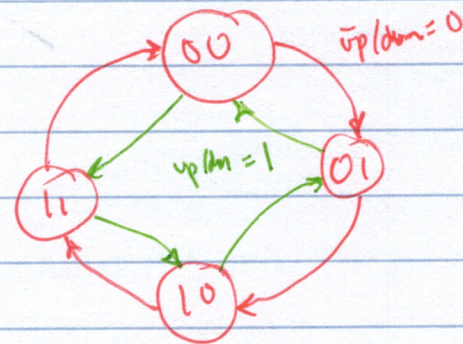
$\bar{u}/dn = 1$
N.S.

A) Method 1

Q ₁ P.S.Q ₀	Q ₁ ⁺	Q ₀ ⁺	Q ₁ ⁺	Q ₀ ⁺
00	0 ⁰	1 ¹	1 ¹	1 ¹
01	1 ¹	0 ⁰	0 ⁰	0 ⁰
10	1 ⁰	1 ¹	0 ¹	1 ¹
11	0 ¹	0 ¹	1 ⁰	0 ¹

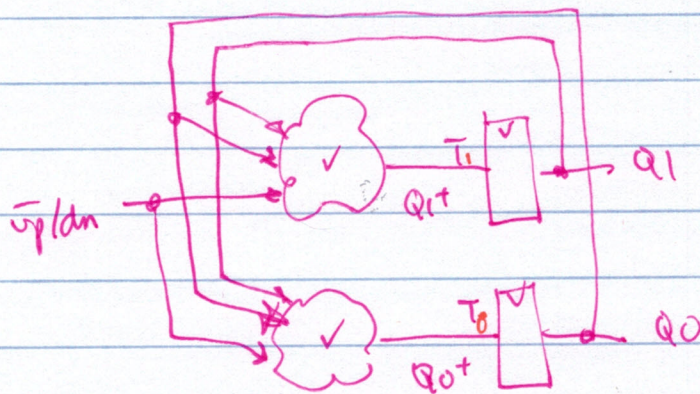
\bar{u}/dn

	0	1
00	0	1
01	1	0
11	1	0
10	0	1



T_0

1	1
1	1
1	1
1	1

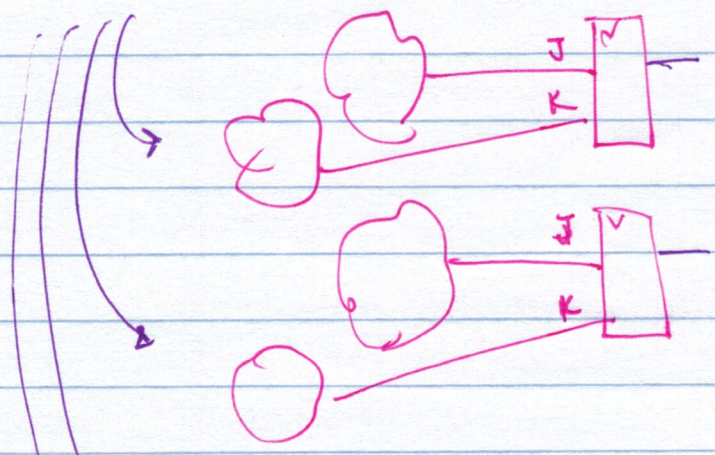


$$T_{Q1} = Q_0 \oplus \bar{u}/dn$$

$$T_{Q0} = 1$$

Next State Logic

SR, JK



D, T ✓

