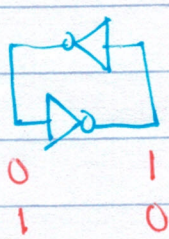
EEC 18

NOV. 4

Clock - periodic

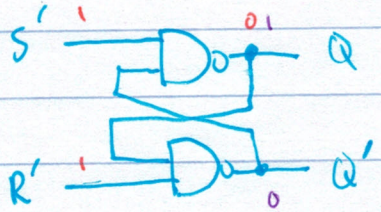
Memories

* I. Single-bit
II. Array

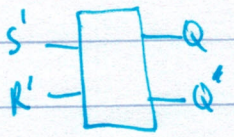


A) Clockless latches

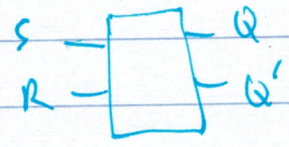
1) SR NAND latch

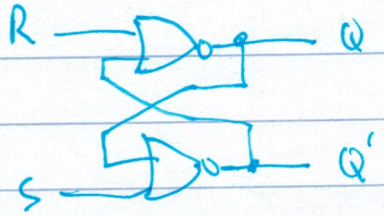


S'	R'	Q	New Q		
0	0	0	1		Invalid
0	0	1	1		
0	1	0	1		Set
0	1	1	1		
1	0	0	0	Q'=1	Reset
1	0	1	0	Q'=1	
1	1	0	0	Q'=1	Memory
1	1	1	1	Q'=0	



2) SR NOR latch

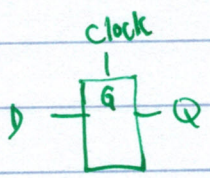


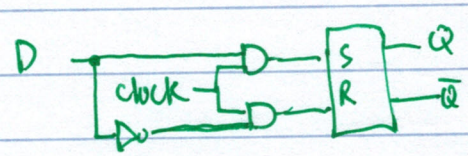


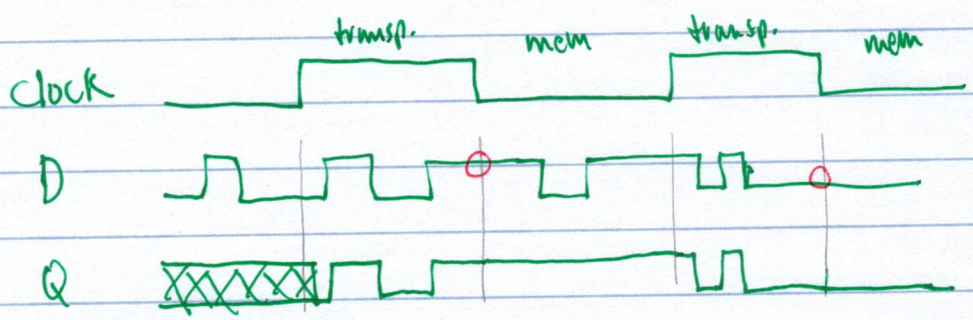
S	R	Q_{new}	
0	0	Q_{old}	Memory
0	1	0	Reset
1	0	1	Set
1	1	0, D	Invalid

B) Transparent / Gated Latches
Level-Sensitive Latches

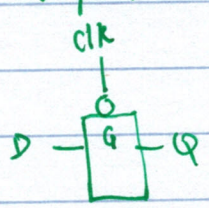
1) D Transparent-High Latch

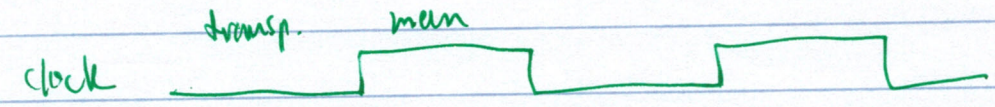




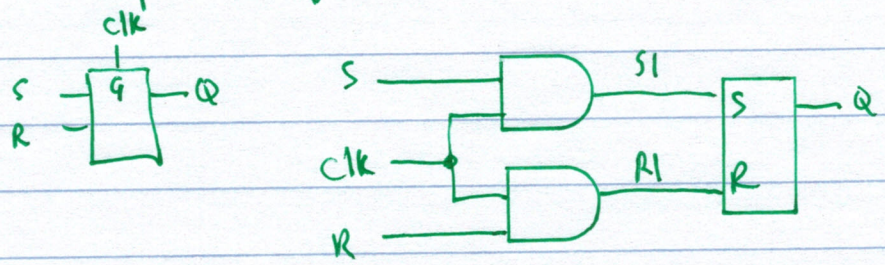


2) D Transparent-low Latch



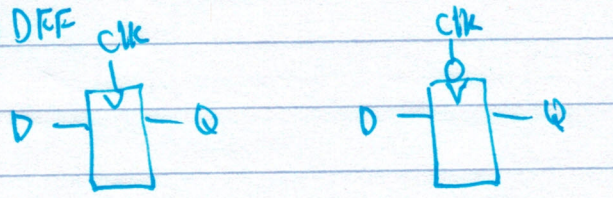


3) SR Transparent-High Latch



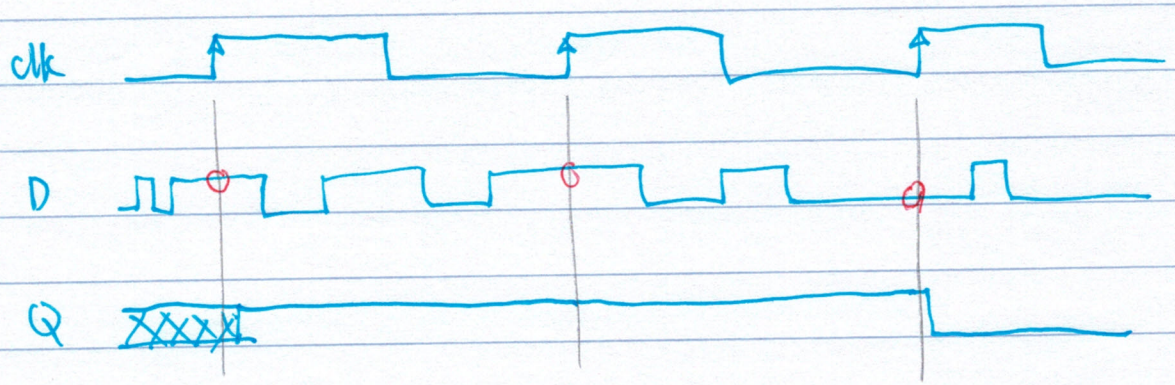
c) Edge-Triggered Flip Flops (FFs)

1) DFF

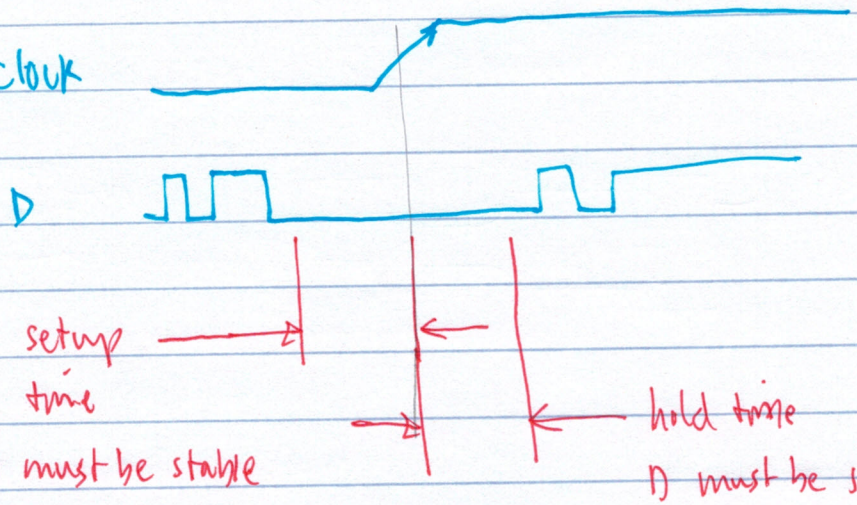


rising-edge falling-edge

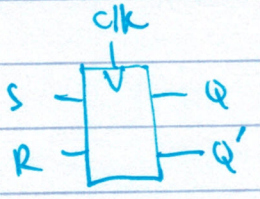
D	Q	Q new
0	0	0
0	1	0
1	0	1
1	1	1



Zoom in

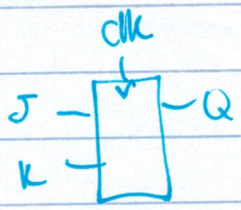


2) SR FF



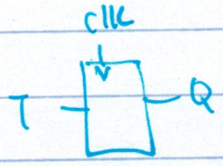
S	R	Q^+ = Qnew	
0	0	Mem	$Q^+ = Q$
0	1	0	Reset
1	0	1	Set
1	1	-	Invalid

3) JK FF



J	K	Q^+	
0	0	$Q^+ = Q$	Mem
0	1	0	Reset
1	0	1	set
1	1	$Q^+ = \bar{Q}$	toggle

4) T FF - Toggle



T	Q^+	
0	$Q^+ = Q$	Mem
1	$Q^+ = \bar{Q}$	Toggle

Other inputs:

- Reset (clear)
- Set (preset)

- Synchrous - effective only on clock edge
- Asynchronous - effective anytime

	R	S
async	✓	✓
sync	✓	✓

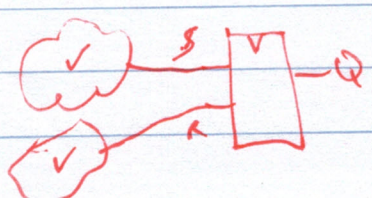
- active high
- active low

all 8 combinations ok

For design

Q	Q^+	D	S	R		J	K	T
0	0	0	0	X	no reset	0	X	0
0	1	1	1	0		1	X	1
1	0	0	0	1		X	1	1
1	1	1	X	0	no set	X	0	0

p-347

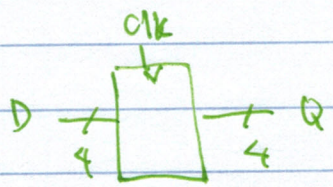


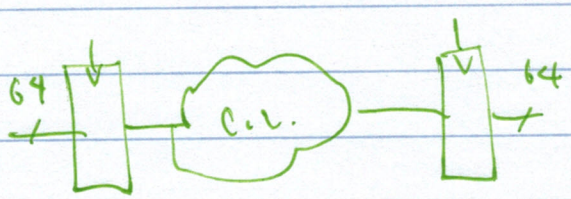
For analysis

D FF	$Q^+ = D$		
D-CE	$Q^+ = D \cdot CE + Q \cdot \overline{CE}$	Clock enable	p.401
T	$Q^+ = Q \oplus T$		p.336
SR	$Q^+ = S + \overline{R} \cdot Q$		
JK	$Q^+ = J \cdot \overline{Q} + \overline{K} \cdot Q$		

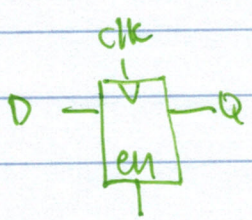
Unit 12

A register is set of FFs w/ a common clock signal



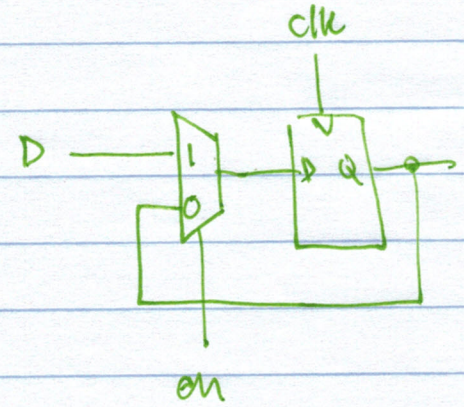


Enablable registers/FFs



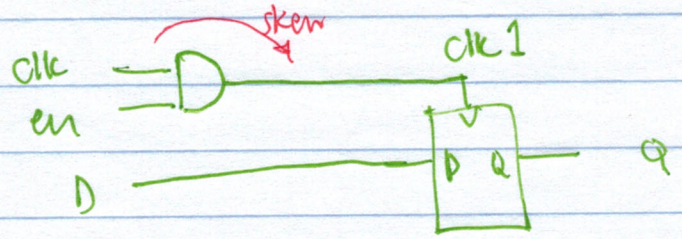
D	en	clk	Q^+	
X	0	↑	Q	hold, mem
0	1	↑	0	
1	1	↑	1	

i)



good way to build it

ii)

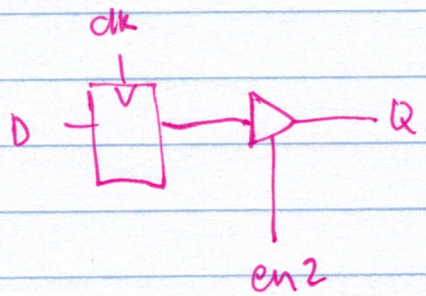


bad circuit

- susceptible to glitching on en when clk = 1

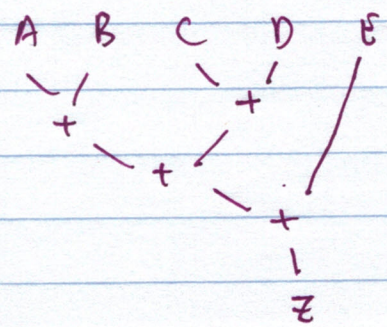
iii) Custom circuit

Regs w/ Tri-state outputs



Accumulators

Ex. $Z = A+B+C+D+E$



\+ fast

\- Large circuit

\- Inflexible

ACC = 0 clear

ACC = ACC + A

ACC = ACC + B

ACC = ACC + E

Picture cash register

a · b'