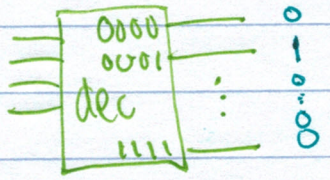
EEC 18

Oct. 28

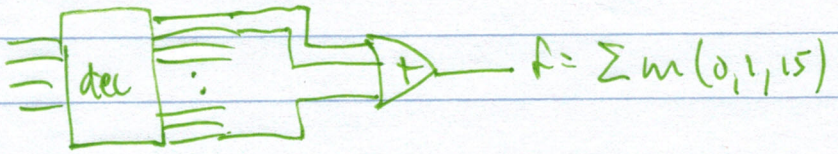
N binary → 2^N combinations

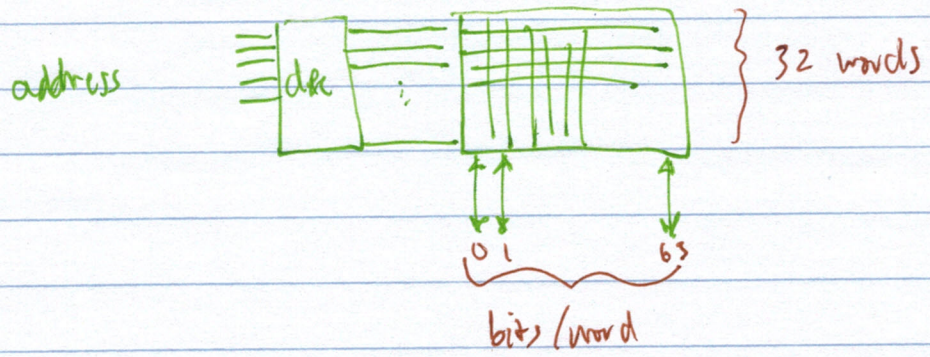
Decoders



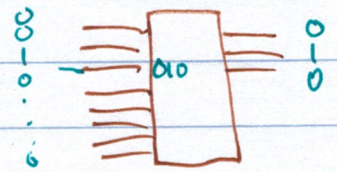
only one output high at a time

N 2^N



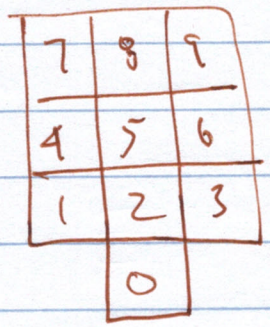


Encoder

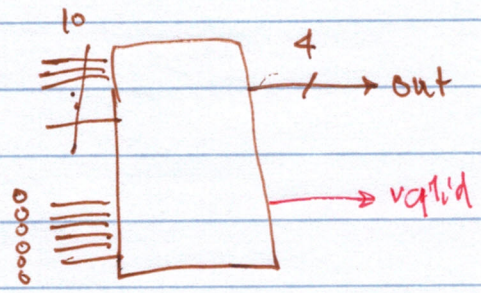


8 (2^N) 3 (N)

Ex:



min encoding requires 4 bits



(2^N) (N)

Possibility #1 - only valid when one input is high

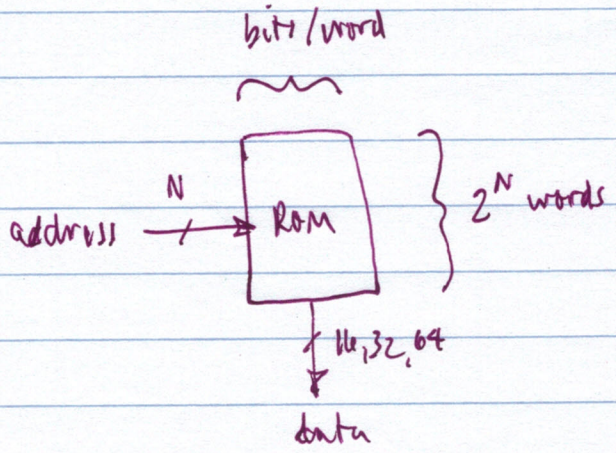
	k_0	k_1	k_2	k_3	...	k_9	out	valid
none high (1)	0	0	0	0	...	0	XXXX or 0000	0
single bit (10) high	1	0	0	0	...	0	0000	1
	0	1	0	0	...	0	0001	1
	0	0	1	0	...	0	0010	1
	0	0	0	0		1	1001	1
multiple bits high (1013)	1	1	0	0	...	0	XXXX	0
	0	1	0	1		1	XXXX	0

valid = 0

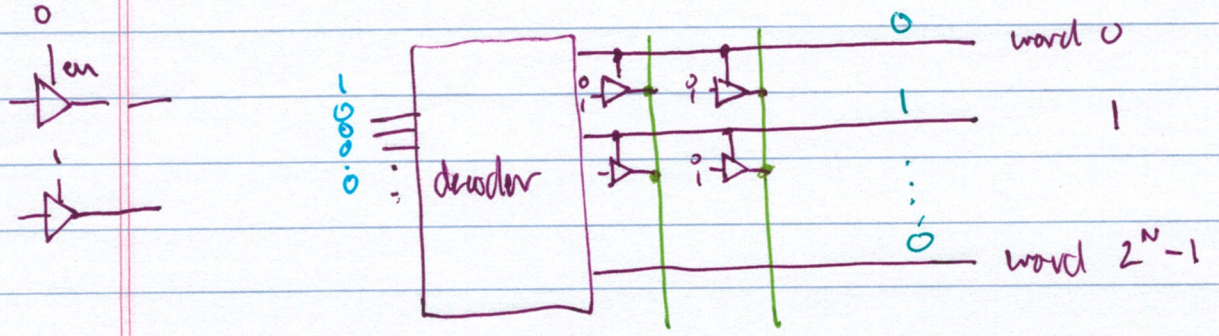
Possibility #2 - highest # input wins - Priority Encoder

	k_0	k_1	k_2	k_3	...	k_q	out	valid
none or single bit high (11)	same as above						same as above	
	0	0	0	0	. .	1		
(1013)	X	1	0	0	0 0 0 0 0 0		0001	1
	X	X	1	0	0 0 0 0 0 0		0010	1
	X	X	X	1	0 0 0 0 0 0		0011	1
					= = = = = =		= =	
	X	X	X	X	X X X X X	1	1001	1

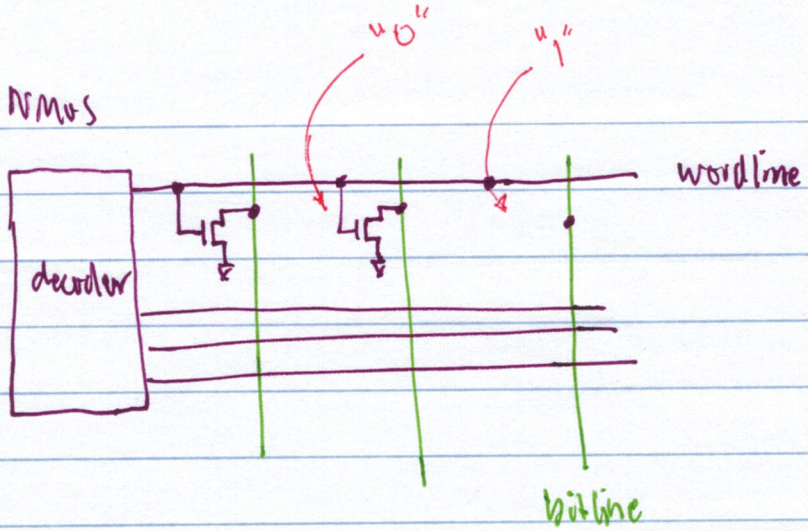
Read Only Memory (ROM)



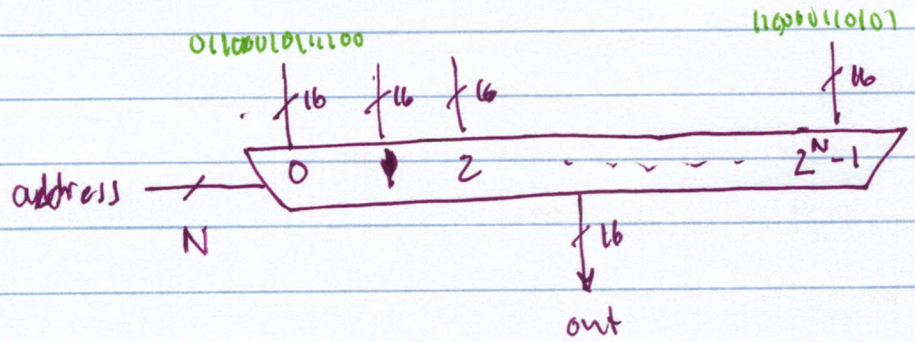
a) tri-state buffers



b) using NMOS

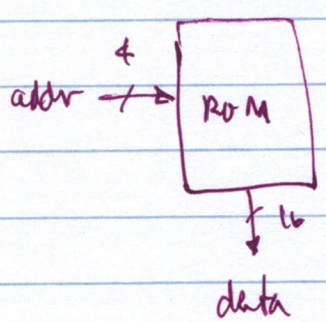


c)



A Truth Table is the way to specify the contents of a ROM

a b c d	data [0:15]
0 0 0 0	1110001010 - 011
=	=



Key Concept

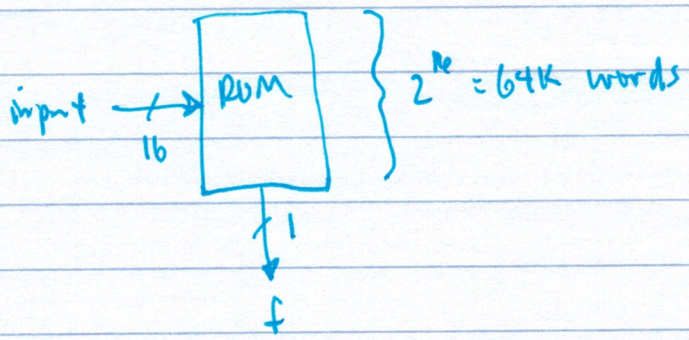
Use a ROM to implement combinational logic
- "brute force"

Ex: f is high when 16-bit input is a factor of 4.

T.T.

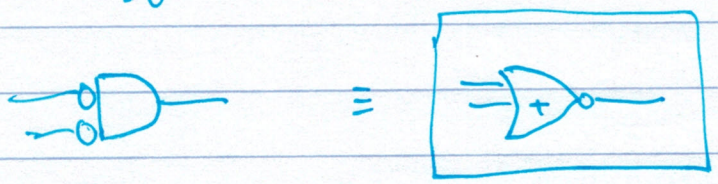
input [0:15]	f
0000 . . 000	1
0000 . . . 001	0
	0
	0
	1
	⋮

a) ROM



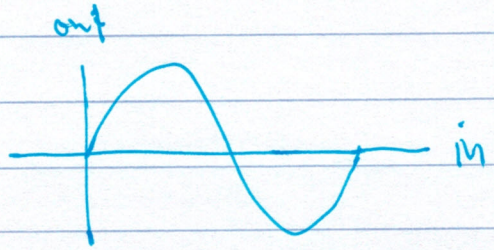
b) Logic

f = 1 when input [1] & input [0] = 0
= 0



Ex: sin or cos table
- high randomness

ROM may be better than logic

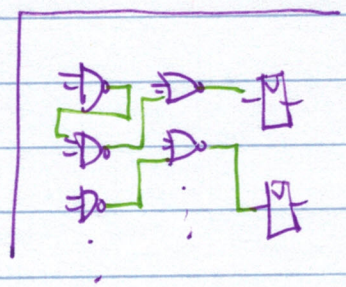


Types of ROMs

1) Permanent - at time of manufacture
2) One-time programmable - fuse PROM
3) Erasable ROM, using UV light EPROM
4) Electrically-erasable PROM EEPROM - Flash

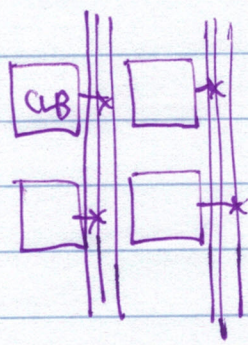
Field-Programmable Gate Array

Gate Array



FPGA

1) User programs
   a) small logic blocks (CLB) Comb. logic block
   b) connections between blocks

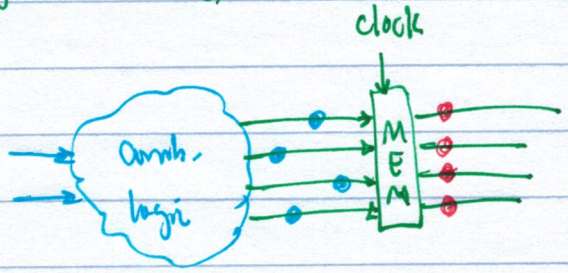


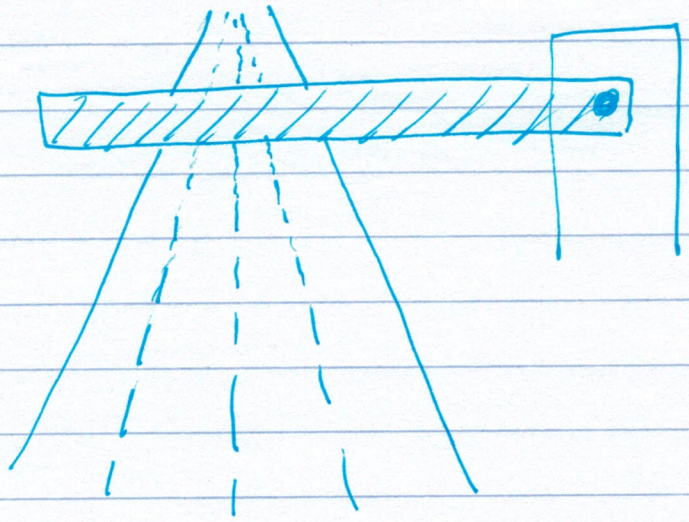
2) Using HDL - Verilog or VHDL

3) Xilinx and Intel (Altera)

4) domains of 100

Clock signal - special signal that paces the flow of data inside digital machines





"Single-bit" memories

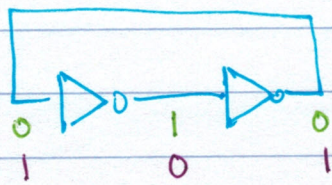
1) Clockless latches

2) Transparent latches or level-sensitive latches
clock input labeled "G"

3) Edge-Triggered Flip-Flops

vs. Array Memories
- Address

Memory must be by:



two states → remember 1 bit