EEC 018 Lab Tips and Common Errors

Overall Tips:

1. The device is MAX10 10M50DAF484C7G
2. The project name is same as top level BDF file name
3. All design files (i.e your schematic BDF files) are included in project.
    a. On the top left small window, click on “Files” to check whether files are included
4. Import assignments before programming to DE-10 board
5. Modelsim setup:
    a. Tools -> Options -> EDA Tool Options -> Path: “C:\IntelFPGA\17.0\modelsim_ase\win32aloem”
    b. This path should be changed to your own installation path for your personal machine.

Common Errors:

1. **Project Hierarchy is empty**

   This happens when you try to open an existing project, but you didn’t open project file “.qpf” to start Quartus.

2. **Can’t synthesis current design – top partition does not contain any logic**

   Reason: Project name is different as top design name. For example, you named your project as “lab2”, but the top level BDF file is called “lab2SOP.bdf”.

   Solution: You can rename “lab2SOP.bdf” to “lab2.bdf”.

3. **Can’t place PIN assignment on node HEX0[0], or other nodes**

   Reason: Your device is wrong.

   Solution: Go to “Assignment -> Device” and select the correct device.

4. **Compilation error: design doesn't fit in the device/successful compilation but no results on board even the schematic is correct.**

   Reason: Your device is wrong.

   Solution: Go to “Assignment -> Device” and select the correct device.

5. **Block or Symbol “NOT” of instance “inst” is already defined as a signal name or another logic function**

   Reason: Instance name conflict

   Solution: Right click on the symbol has error, select “Properties”, change the instance name to unique name.

6. **Modelsim Launching Error from Quartus Editor**

   Reason: Modelsim is not setup properly

   Solution: Go to *Tools> License Setup> General> EDA Tools Options> Modelsim-Altera and set the path as "C:\intelFPGA\17.0\modelsim_ase\win32aloem"*. Accordingly, set the *win32aloem* path on your personal laptop.

7. **“Load cancelled” on Modelsim**

Make sure that all the required libraries, *altera_ver* and *fiftyfivenm_ver* are added in the *Start Simulation dialog box*.

8. **"Error loading design" on Modelsim**

   Verify that correct Verilog netlist file is selected under work tab in the “Start Simulation” dialog box.

9. **“Native Link error” window pop up when trying to open Modelsim**

   Reason: design hasn’t been compiled yet

   Solution: compile your design before opening Modelsim

10. **Can't select Import assignments, devices etc. under "Assignment" tab on Quartus**

    Make sure that you have opened up the qpf file for the project, then try pin assignment and compilation. You should also verify that quartus license file is correct by doing this, *Tools > License Setup> License file: 28333@license.engr.ucdavis.edu*

11. **All Pins are assigned in the “Assignment Editior”, even those not used in your project**

    Reason: Your project doesn’t include your design file (.bdf)

    Solution: Add all design files into project.

12. **Can’t import assignment, because it is current file**

    Reason: The qsf file under same directory of your project

    Solution: Generate a new qsf file from System Builder or move the existing qsf file to a subdirectory inside your project

13. **Can’t launch the ModelSim-Altera software – the path to the location of the executables for the ModelSim-Altera software were not specified or the executables were not found at the specified path.**

    Reason: unknown. The message persisted even after linking modelsim to the correct folder.

    Solution: Uninstall and reinstall the software.

2021/01/21 Added “Can’t launch the ModelSim...” error and solution.