## **SPARE GATES**

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- Large VLSI designs made by cautious designers will often include spare gates
- As the name states, these are extra gates that are functionally unused. To minimize leakage power, they should be disabled
  - Ex: logic gate inputs tied to *Vdd* or *Gnd*
- They are however ready to be used if needed
  - Connected to *Vdd* and *Gnd*. FFs connected to *clock*
- They are extremely useful in two scenarios if a failure is found in the chip:
  - 1) Extra gates are needed for FIB fixes
  - 2) A small number of gates can be added or changed without changing the expensive transistor-related layers but instead by changing only a few metal layers