PHOTOMASKS

magic Layers vs. Mask Layers

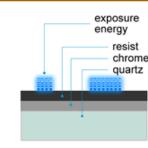
- magic allows designers to work with logical layers
- Chip fabrication requires more detailed layers
- magic captures all necessary information and generates the rest
- Example magic layout with m1-m2 via

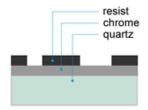
Example m1-m2 via pattern in actual mask

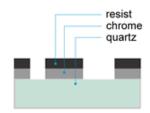
Mask Costs

- Approximate cost for a set of masks for the indicated CMOS fabrication technology
 - 28 nm \$2 million
 - 14/16 nm \$4 million
 - 7 nm \$8-10 million
 [Mark Papermaster, CTO AMD, CTO Forum, Nov 2016]
- Two of the reasons for the dramatic increases in cost are the finer features sizes, and the need for many more masks for multiple patterning lithography

- 1. Generate Pattern
 - Convert circuit design data to image in resist through e-beam/laser exposure.
- 2. Develop Resist
 - Develop temporary pattern in resist to serve as a match for etching.
- 3. Etch Chrome
 - Define permanent pattern in chrome.





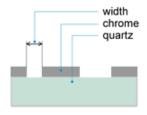


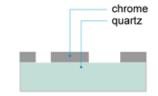
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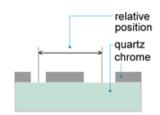
4. Remove Resist

EEC 116, B. Baas

- Remove temporary masking layer.
- 5. Measure Critical Dimensions
 - Ensure features are the proper size.
- 6. Measure Feature Placement
 - Ensure features are in the proper position.

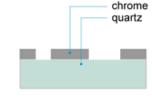


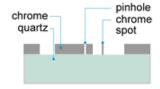


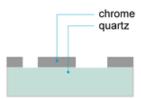


- 7. Initial Clean
 - Clean for defect inspection.

- 8. Inspect for Defects
 - Ensure no unetched chrome or pinholes are present.
- 9. Repair
 - Repair any defects found.







10. Pre-Pellicle Clean

- Remove any particulates before pellicle application.
- *Pellicle* is a protective cover that shields the photomask from damage and dirt.
- 11. Apply Pellicle
 - Provide a particle barrier to ensure the integrity of the pattern from particles.

12. Audit

– Final check.

