Aaron Stillmaker

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Research Interests

High speed low power many core processor architecture, VLSI design, digital circuit design, hardware optimization, Verilog hardware design, parallel algorithms, paralyzed database sorting algorithms, enterprise applications, and digital signal processing applications.

Education

2008-Present **University of California, Davis** Davis,CA
Degree Objective: Ph.D., Electrical and Computer Engineering
Major: Digital Design and Computer Systems
Minor: Signals and Systems
Expected Graduation: 2014
Lab: VLSI Computation Lab, Advisor: Bevan M. Baas Ph.D.

2004–2008 **California State University, Fresno** Fresno, CA
Magna Cum Laude, Smittcamp Honors College: President's Scholar
B.S. Major: Computer Engineering, Minor: Business

Publications and Presentations

Aaron Stillmaker
"Energy-Efficient Sorting on a Many-Core Processor Array."
Invited Talk. Oracle (Sun Microsystems). Santa Clara, CA, March 2013.

Aaron Stillmaker, Lucas Stillmaker, and Bevan Baas,
"Fine-Grained Energy-Efficient Sorting on a Many-Core Processor Array,"
IEEE International Conference on Parallel and Distributed Systems (ICPADS 2012), Singapore, December 2012.

Aaron Stillmaker, and Bevan Baas,
"Modular Sorting on a Fine-Grained Many-Core Processor Array,"
UC Davis ECE Department Industrial Affiliates Conference, June 2012.

Aaron Stillmaker, Zhibin Xiao, and Bevan Baas,
"Toward More Accurate Scaling Estimates of CMOS Circuits from 180 nm to 22 nm,"
Technical Report ECE-VCL-2011-4, VLSI Computation Laboratory, ECE Department, University of California, Davis, December 2011.

Aaron Stillmaker, Zhibin Xiao, Bin Liu, and Bevan Baas,
"Computing Enterprise Workloads With Many-Core Arrays as Special-Purpose Processors,"
C2S2 Annual Review, October 2011.

Aaron Stillmaker, Zhibin Xiao, and Bevan Baas,
"Computing Enterprise Workloads With Many-Core Arrays and Special-Purpose Processors,"
C2S2 Annual Review, October 2010

Work Experience

2008-Present **VCL, ECE Department, University of California, Davis** Davis, CA
Graduate Student Research Assistant
Working on research projects for Dr. Baas in the VLSI Computation Laboratory (VCL). Currently working on designing the 3rd generation of our group's AsAP processor. Previously implemented a low powered external database sort on the fine-grained AsAP2 many-core processor array coding in C++, CUDA and Assembly Language. Wrote a dual clock FIFO in Verilog for communicating between two clock frequencies. Researching the use of a fine-grained many-core processor array for enterprise workloads.

2011-Present **ECE Department, University of California, Davis** Davis, CA
Teaching Assistant
Managed and taught lab sections and graded student work. Worked with instructors for ECE 116 (VLSI Design), ECE 70 (Computer Structure and Assembly Language), and ENG 6 (Engineering Problem Solving). Worked closely with students to help them learn material, and created quizzes, home works, and projects for the courses.

2007-2008 **Pelco** Clovis, CA
2006 Summer Software Test Specialist (Intern)
Tested Software for new digital video recording devices, created back-end scripts to run tests on programs, wrote automated testing scripts, and worked with developers to fix problems.

2007-2008 **ECE Department, California State University, Fresno** Fresno, CA
Lab Instructor, ECE 1 Lab
Instructed a Lab class for introduction to electrical and computer engineering lab as well grading for multiple lab sections.

2002–2008 **A.L.A. Custom Computing** Fresno, CA
Co-Founder/ General Partner
Build custom computers from parts, set up networks for small businesses, and create large scale multimedia presentations.

Tools / Skills

Verilog, NCVerilog, Design Compiler, SimVision, Magic, IRSim, HSpice, C/C++, CUDA, Java, Assembly Language (MIPS & x86), Matlab, Perl, Bash, Unix

Relevant Coursework

Graduate: Low Powered Digital IC, DSP VSLI Design, Design and Optimization of Embedded Systems, Graphics Architecture, Digital Signal Processing, Digital Image Processing, Code Generation, High Performance Computer Architecture, Advanced Computer Architecture

Undergraduate: VLSI Design, Advanced Computer Architecture, Digital Logic and System Design, Programming in C and C+, Analog Circuit Analysis, Signals and Systems, Computer System Architecture Organization, Digital Signals Processing, Random Signals Analysis, Verilog HDL, Computer Processor Architecture, Computer Networks and Distributed Processing, Operating Systems, Software Engineering

Extra Curricular

- GAANN Fellow (2008)
- Reviewer for IEEE Journal of Solid-State Circuits (JSSC), IEEE Design and Test of Computers, IEEE/ACM International Symposium on Microarchitecture (MICRO), and IEEE International Conference on Computer Design (ICCD)
- Chapter Advisor, Tau Beta Pi, UC Davis (2008-Present)
- Chief Justice, Student Court (2008); Senator At-Large (2006-2007), Associated Students Inc., CSU Fresno
- Graduate Student Member, IEEE
- Member (2005-Present); President, Tau Beta Pi, CSUF (2007)
- Member (2005-Present); President, Eta Kappa Nu, CSUF (2006)
- Member, Phi Kappa Phi

References

Available upon request