Ultra Low Loss Millimeter Wave Multichip Module Interconnects

Anh-Vu H. Pham, Joy Laskar, Vikram B. Krishnamurthy, *Member, IEEE,* H. S. Cole, and T. Sitnik-Nieters

***Abstract*—We present the design and electrical characterization of a multilayer organic based multichip module (MCM) for use at W-band (75–110 GHz). The ultra-low loss microstrip transmission line on Kapton E® (a trademark of DuPont) thin films and benzocyclobutene (BCB) adhesives is reported at W-band. An electrical model for a vertically stacked via interconnect to an integrated circuit (IC) is experimentally developed. This interconnect exhibits very low parasitics and preserves excellent matched conditions for devices and circuits in a module. The electrical performance of the vertically stacked via offers superior performance relative to ribbon and wire bond results reported in the literature at millimeter wave frequencies. We conclude that this technology is capable of realizing compact modules at millimeter wave frequencies.**

***Index Terms*— Interconnects, MCM, organic materials, W-band.**

I. Introduction

THE driving forces behind the development of new packaging approaches are the reduction of size, weight, and improvement of functionality. Key to success is to reduce parasitics associated with interconnects and to utilize the vertical dimensions to accommodate different types of circuitry. Conventionally, ribbon bonds are used as interconnects for components and integrated circuits (IC's) on a single layer ceramic substrate that is housed in a module. Ribbon and wire bonds are a primary source of parasitics at millimeter wave frequencies. The use of ribbon bonds is not effective and feasible to realize compact modules because its parasitics can significantly degrade the performance of IC's and the entire module. There has been on-going research to develop various packaging approaches to eliminate ribbon bonds and to increase the packaging efficiency [1]. The effort has been focusing on the development of three-dimensional (3-D) multichip modules which increase the packaging density. The approach we are pursuing is an overlay of dielectric films with IC's embedded in recessed cavities [2]–[6] in a variety of substrates. This 3-D packaging approach offers very low parasitic interconnects and compact modules.

In this paper, we present the design and rigorous characterization of a multilayer organic based MCM at W-band (75–110 GHz). These results are the first to date on a multilayer MCM at W-band. Interconnects in this module are mainly microstrip and stripline structures in various dielectric thin films with vertically stacked vias for connections to IC's and other interconnect structures. We characterize and compare the performance of the interconnects on organic materials and ceramic. We experimentally develop an electrical model for the stacked vias and extract their parasitic elements. These vertical interconnects provide the transitions from microstrip and stripline structures to IC's embedded in recessed cavities in a substrate. In addition, we design and fabricate test structures which include two microstrip lines interconnected with vertically stacked vias and microstrip lines traversing an air filled cavity to evaluate the parasitics of the connection from the microstrip to the IC. We characterize these structures and compare their performance with ribbon bonds.

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II. Multi-Layer Packaging Concept

The multilayer organic based MCM is a chip first approach, developed by GE/Lockheed Martin, where IC's are placed in cavities formed in a ceramic or plastic substrate [2]–[6]. The architecture grants the module its excellent performance because the ability to interconnect layers are formed above the IC's where stacked vias are used to make contact with the pads of the IC's housed in ceramic cavities. Ti/Cu/Ti is the metallization for the multi-layer interconnects. The dielectric layer is usually composed of three layers, with each layer consisting of an adhesive and a polymer dielectric. In our two test coupons, the initial layer is composed of Ultem® (a trademark of General Electric) adhesive, a thermoplastic polyetherimide, and a Kapton E® dielectric film. The second and third layers are composed of either a siloxane polyimide/epoxy (SPIE) blend adhesive or a thermoset polymer [benzocyclobutene (BCB)] with a Kapton E® dielectric film. In this paper, we abbreviate the two combinations of dielectric layers with adhesives as KE/BCB and KE/SPIE. Fig. 1 shows how an IC in a cavity can be connected to components in a module.

III. Investigation of Interconnect Loss

Several 50-Ω microstrip transmission lines with different lengths have been designed and fabricated on KE/BCB, KE/SPIE, and alumina. The total thickness of the organic dielectric layers including adhesives is 110 μm. The total metallization thickness including Ti/Cu/Ti is 4 μm. Since these microstrip lines are effectively on six dielectric layers, a

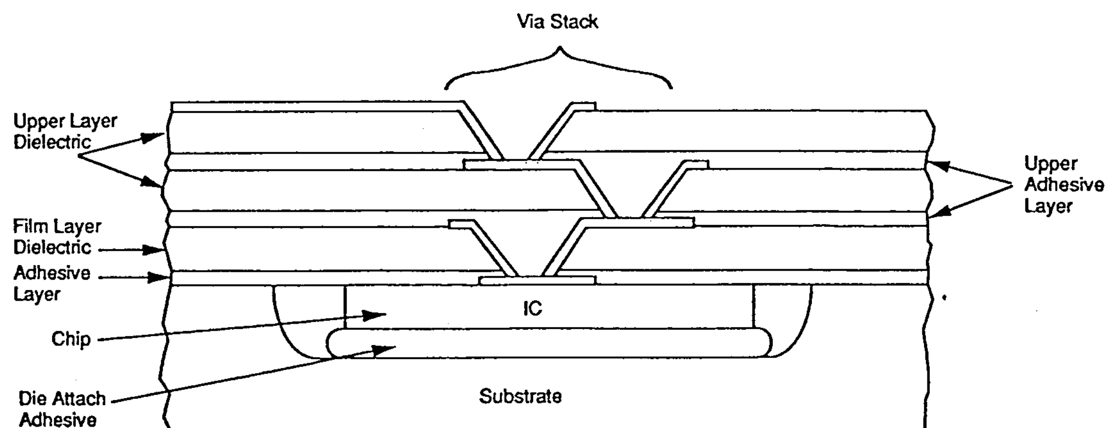
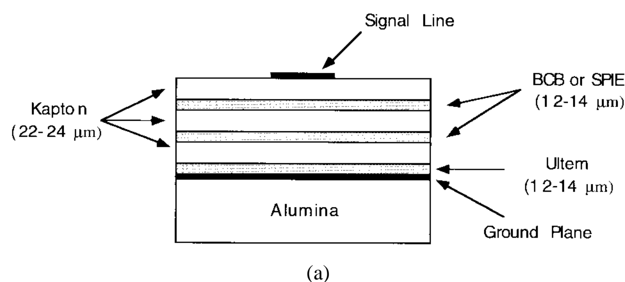
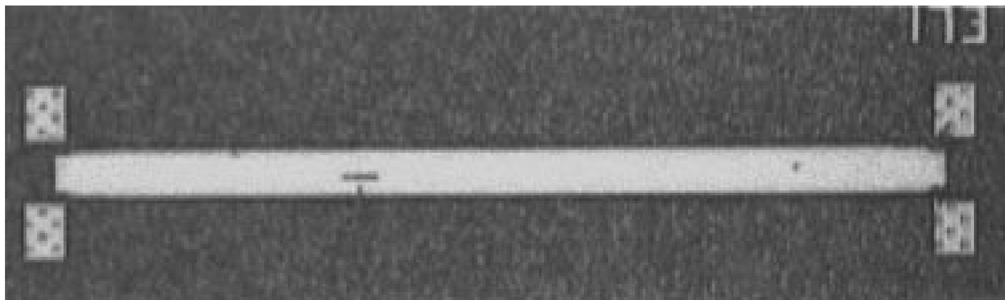


Fig. 1. A cross section of the multilayer organic based MCM, demonstrating interconnects using stacked vias. The IC pads are connected to the microstrip/stripline interconnects by stacked vias.



(a)



(b)

Fig. 2. (a) Cross section and (b) top view of microstrip line test structures on multilayer dielectric films with adhesives. The microstrip line has CPW launches, which are formed with stacked vias connecting to the common ground. Each stack consists of three staggered 50 μm by 50 μm vias.

commercial electromagnetic (EM) simulator using the Method of Moments [7] is used to optimize the strip width to achieve a 50-Ω characteristic impedance. This simulator takes into account the conductor thickness and its loss. The strip width of 50-Ω microstrip transmission lines is nominally 240 μm for the relative dielectric constants of polymers and adhesives in the range of 2.9–3.2 [5]. Likewise, the strip width of a microstrip transmission line on an 120 μm thick alumina substrate is nominally 120 μm because of its higher dielectric constant. The microstrip transmission lines have a ground–signal–ground input configuration for on-wafer probing. Fig. 2(a) and (b) depict a cross-section and a layout of microstrip lines for characterization.

An HP85109C automatic network analyzer (ANA), whose W-band test-set has WR-10 waveguide output, is used to measure S-parameters of microstrip transmission lines. Air coplanar waveguide microprobes (ACP®, a trademark of Cascade Microtech, Inc.), which have WR-10 waveguide input, are employed for electrical contacts to the ground-signal-ground pads of the microstrip lines. The microprobes are connected directly to the W-band test-set using WR-10 waveguide. On-wafer thru-reflect-line (TRL) calibration is performed using a W-band impedance standard substrate (ISS) from Cascade Microtech prior to measurements [8], [9]. This W-band ISS provides a set of TRL standards, including coplanar waveguide transmission lines of different lengths and short standards (reflects) for calibration. After the calibration, the measurement reference planes are defined at the probe tips. Since the dielectric properties of adhesives and polymers are affected by humidity, the devices are baked in a N_2 ambient at 100 °C over night and stored in a desiccator. The measurements are performed in positive-flow N_2 environment to minimize water absorption.

Microstrip transmission lines on KE/BCB, KE/SPIE, and

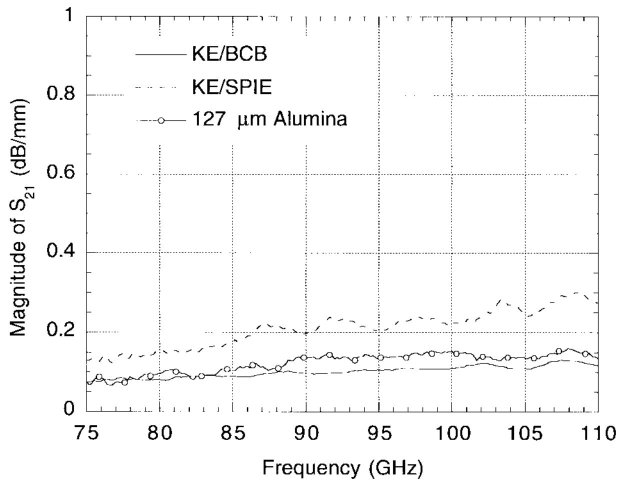
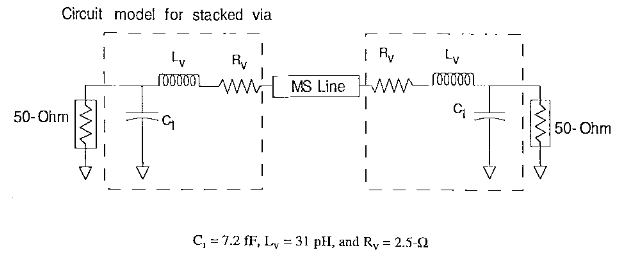


Fig. 3. Magnitude of S_{21} (dB/mm) versus frequency data for the following three types of microstrip lines: multilayer 50-Ω microstrip with Kapton E dielectric and BCB adhesive (KE/BCB), multilayer 50-Ω microstrip with Kapton E dielectric and SPIE (KE/SPIE), and 50-Ω microstrip on 127 μm thick alumina.

alumina are measured, respectively. The insertion loss (S_{21}) of the microstrip lines is comprised of dielectric and conductor loss [10]. Radiation loss can be neglected for the dimensions of the microstrip lines in this experiment. The dielectric loss of the microstrip lines on KE/BCB and KE/SPIE is contributed by both the Kapton and adhesive materials. Fig. 3 shows the measured insertion loss per unit length of 50 Ω microstrip transmission lines on KE/BCB, KE/SPIE, and alumina. These results are comprised of the total loss, which includes both the conductor and dielectric losses. We find that the total loss of the microstrip line on KE/BCB is less than that of the microstrip line on KE/SPIE, where the only difference is the two adhesive layers BCB and SPIE. Therefore, the reduction in loss of the microstrip line on KE/BCB results from the use of the lower loss BCB adhesive as compared to the SPIE adhesive. In addition, the microstrip transmission lines on KE/BCB and alumina have comparable overall loss at W-band. One advantage of the low dielectric material is the wide width of the 50 Ω microstrip transmission line, which reduces the conductor loss and thereby the total loss of the microstrip transmission line [10]–[12]. These results demonstrate that an ultra low loss microstrip transmission line can be realized at W-band with the use of BCB.

IV. Vertical Interconnect Modeling

Since vertically stacked vias are used to connect microstrip and stripline structures in this multilayer module, it is crucial to develop an electrical model to determine their parasitic effects. In this paper, an empirical technique developed at Georgia Tech (based on frequency domain measurements) is used to model the stacked vias [13], [14]. The test structures used in this experiment are 4.5 and 8.0 mm long microstrip transmission lines with CPW launch configurations as shown in Fig. 2(b). The ground pads of the CPW launches are connected to the common ground plane by an array of stacked vias, where each stack consists of three staggered 50 μm by 50 μm vias. This technology has passed the MIL-STD-



C_l = 7.2 fF, L_v = 31 pH, and R_v = 2.5-Ω

Fig. 4. The equivalent circuit model of the microstrip line with CPW launches. This structure is used to determine a model for the stacked vias. The lumped elements in the dashed rectangular box are the equivalent circuit model of the stacked vias.

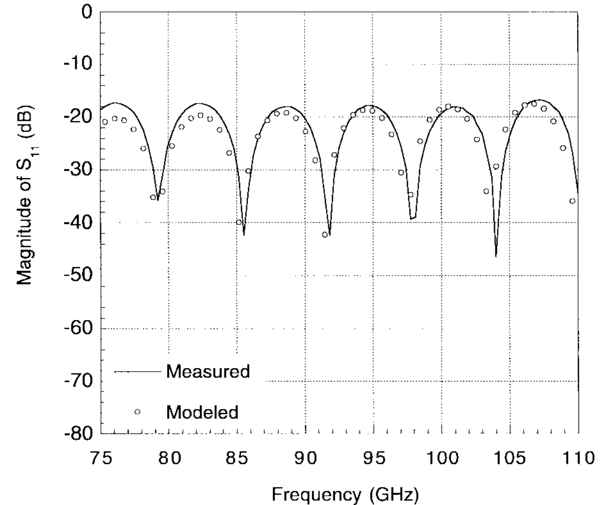
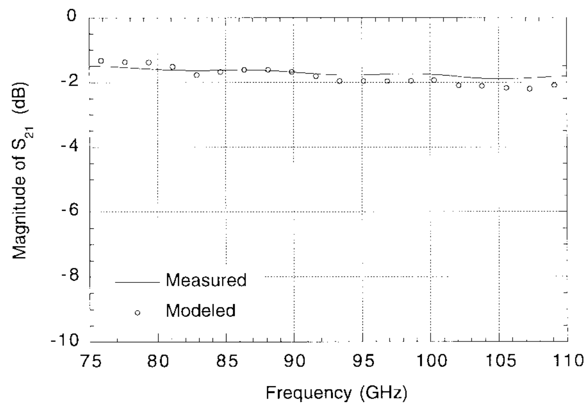


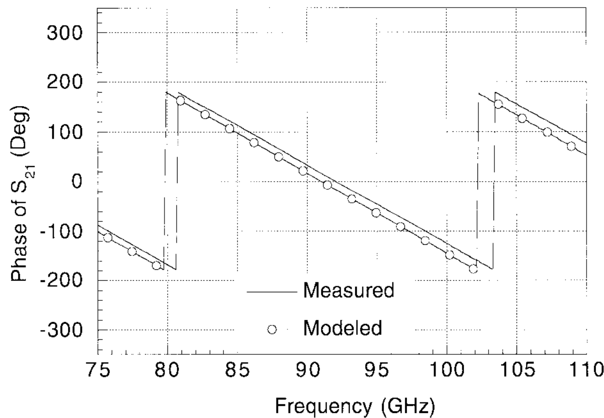
Fig. 5. Measured and modeled S_{11} of the 8-mm long 50-Ω microstrip line (Fig. 2) with the vertical stacked via interconnect. The results include the responses of the CPW launches.

883 reliability specifications. For modeling purposes, the test structure is considered to have three parts: two stacked vias from the ground plane to the CPW pads at two ends and a microstrip transmission line in the middle.

The test structures have been measured with measurement reference planes at the probe tips, defined by TRL calibration using the W-band ISS. The measured S-parameters of these test structures include the response of the microstrip transmission line and the stacked vias. A circuit topology for the test structure is suggested as shown in Fig. 4 and, the lumped elements in the dashed rectangular boxes model the parasitics of the stacked vias. The lumped element parameters are determined by optimization. The MS Line as shown in Fig. 4 represents the microstrip transmission line in the middle of the test structure. The S-parameters of this microstrip line are known quantities and obtained from a commercial EM simulator using the Method of Moments [7]. The EEsof microwave design system (MDS) is used to optimize the parasitic elements of the stacked vias to correlate the measured and modeled S-parameters of the entire circuit which establishes a well-defined model of the parasitic components for the stacked vias. Figs. 5, 6(a), and 6(b) show the measured and modeled return and insertion losses of the test structure, which includes the stacked vias and the 8.0 mm long microstrip transmission line. The circuit model of the via is tested in the 4.5 mm long



(a)



(b)

Fig. 6. Measured and modeled magnitude and phase of S_{21} of the 8-mm long 50-Ω microstrip line (Fig. 2) with the vertical stacked via interconnect. The results include the responses of the CPW launches.

TABLE I
A COMPARISON OF THE RETURN LOSS OF STACKED VIAS AND A RIBBON BOND

Frequency (GHz)	Return loss (dB) of 110-μm stacked vias	Return loss (dB) of a 110-μm ribbon bond	Return loss (dB) of a 250-μm ribbon bond
75	25	5.5	1.8
95	23	4.2	1.3
110	21	3.5	1.0

microstrip line structure to verify the results. The measured and modeled S-parameters of this test structure agree within ±5%, which demonstrates the accuracy of the via model.

We compare the performance of the stacked vias with ribbon bonds. The S-parameters of the ribbon bonds are obtained from the EM simulator using the Method of Moments [7]. Typical ribbon bond dimensions are 120 μm wide and 25 μm thick. The S-parameters of the via are obtained from the developed equivalent circuit model. Table I compares the return loss of 110 and 250 μm long ribbon bonds with 110 μm high stacked vias. The return loss of the stacked vias is less than 20 dB demonstrating that the stacked vias provide an excellent matched condition. The insertion loss of the stacked vias shown in Table II is 0.24 dB better than that of the 110 μm ribbon bond. The actual ribbon bond lengths are expected to be longer and, as shown in Tables I and II, the characteristics

TABLE II
A COMPARISON OF THE INSERTION LOSS OF STACKED VIAS AND A RIBBON BOND

Frequency (GHz)	Insertion loss (dB) of 110-μm stacked vias	Insertion loss (dB) of a 110-μm ribbon bond	Insertion loss (dB) of a 250-μm ribbon bond
75	0.12	0.36	1.56
95	0.16	0.60	2.38
110	0.20	0.87	3.10

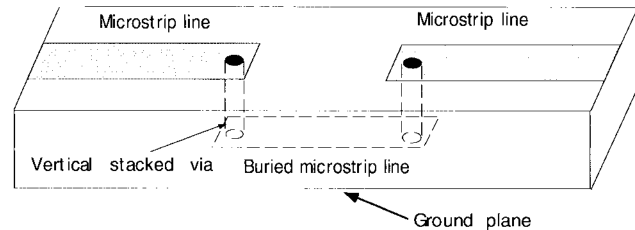


Fig. 7. Schematic representation of 50-Ω microstrip lines to a 50-Ω buried microstrip line transition using a vertically stacked via. The first microstrip line has a dielectric thickness of 110 μm. The bottom and top layer thicknesses of the buried microstrip are 72 and 36 μm, respectively. Therefore, the vias have a height of 36 μm. The width and length of the buried microstrip line is 144 and 3950 μm, respectively.

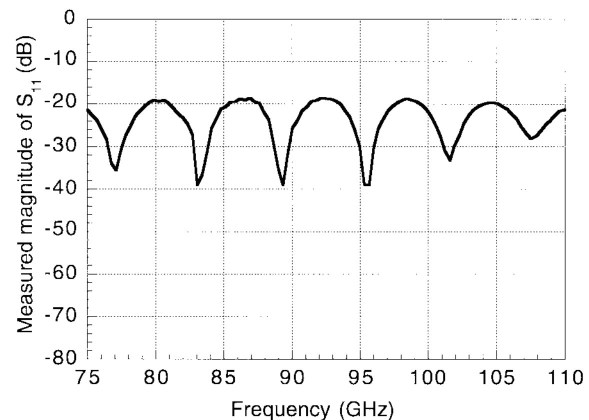
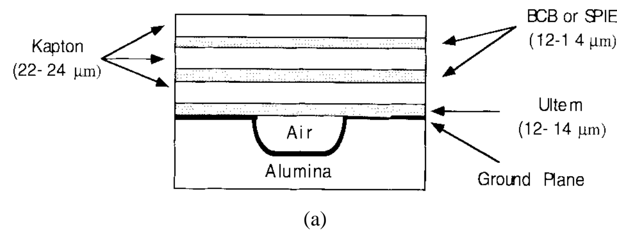


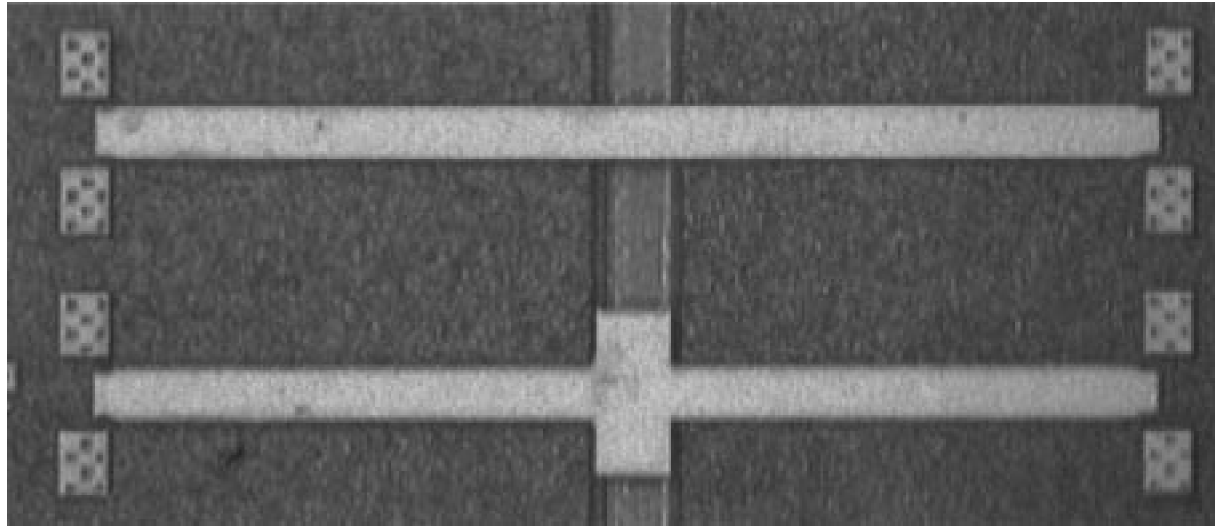
Fig. 8. Measured magnitude of S_{11} of a 50-Ω microstrip line to 50-Ω buried microstrip line transition using a vertically stacked via, as shown in Fig. 6. The CPW launches for probing have been de-embedded.

of a 250 μm long ribbon bond deteriorate significantly. This comparison demonstrates that the stacked vias are an excellent interconnect at millimeter wave frequencies for 3-D modules. These results are, to the best of our knowledge, superior to results reported at W-band for ribbon bonds and flip-chip [15]. In addition, the stacked vias provide match conditions eliminating matching networks while maintaining a 50 Ω impedance system, which reduces the overall loss in the interconnect.

As can be seen in Fig. 4, the lumped model for the stacked vias introduces negligible parasitics. Further, we have analyzed the performance of two 50 Ω microstrip lines connected with a vertical via stack, as shown in Fig. 7. After de-embedding the CPW to microstrip transitions for probing [14], we can accurately determine the performance of the structure, including the vertical via stack, as shown in Fig. 8. The return loss is approximately 20 dB at W-band. This result



(a)



(b)

Fig. 9. (a) Cross section and (b) top view of microstrip line test structures on multilayer dielectric films with adhesives and air gap discontinuity.

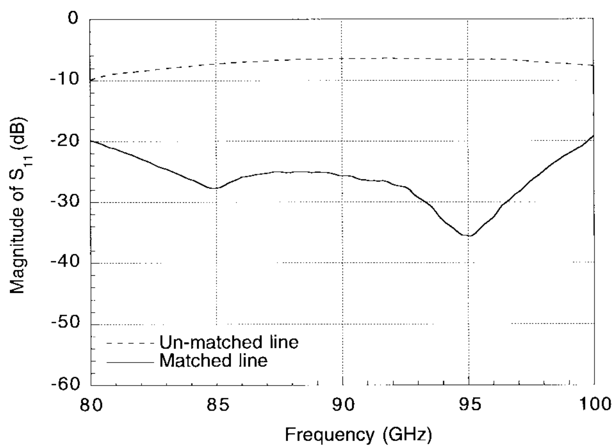


Fig. 10. Measured magnitude of S_{11} of microstrip transmission lines (Fig. 8) over an air cavity.

demonstrates that stacked vias do not require an additional matching network to maintain a 50 Ω impedance system and represents a competitive vertical interconnect at millimeter wave frequencies.

V. Microstrip-to-IC Interconnect Parasitics

The study of a connection from a microstrip line to an IC in a recessed cavity is performed. In this packaging architecture, the IC is placed in a recessed cavity larger than the dimensions of the IC. A 380-μm wide gap, filled with air, typically exists between the IC and any edge of the cavity. To establish electrical connections to the IC pads (Fig. 1), a microstrip line traverses one edge of the cavity, crosses the air gap to the IC, where the vertical via stack then connects the microstrip line to the pads of the IC. A microstrip line can be designed with a very well-controlled characteristic impedance on the multilayer dielectric films. When it is traversing the recessed cavity, the air gap causes a discontinuity in its characteristics, resulting in a poor return loss at millimeter wave frequencies. Across this air gap region, the effective dielectric constant decreases, resulting in an increased characteristic impedance. To compensate this effect, the strip width is increased locally across this air gap region to establish a matched 50-Ω connection to the IC. Several structures have been designed to investigate this air gap discontinuity. The cross-section and the layout of the structures are shown in Fig. 9(a) and (b). These structures consist of metalized recessed cavities in an alumina substrate with microstrip lines traversing above a multi-layer interconnect and are measured using the procedure as outlined above. However, the CPW launches are not de-embedded to account for the parasitic effects of stacked vias. In Fig. 10, we show the return loss of the structure with a matched and unmatched section at W-band. Without the compensation of the matched section, the return loss is degraded by the air discontinuity. The simple matched section improves the return loss to be less than 20 dB at W-band and demonstrates that the air gap phenomena exists in this packaging approach. However, as seen from Fig. 10, this discontinuity can be corrected easily with a matching

section. For different dimensions of air gaps and interconnects, optimized match sections are required to obtain optimum return loss.

VI. Conclusion

We have presented the design and electrical characterization of the multi-layer organic based MCM. We have demonstrated that microstrip transmission lines on KE/BCB and alumina have comparable loss at W-band. The developed electrical model for the vertical stacked vias demonstrate that they have ultra low parasitics and are superior to what can be achieved with ribbon bonds at W-band. These results are, to the best of our knowledge, superior to results reported for ribbon bonds and flip-chip at W-band and demonstrate that the multi-layer MCM approach presented here is suitable for packaging at W-band.

Acknowledgment

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References

[1] E. Cohen, "High density microwave packaging program," in *IEEE MTT-S Dig.,* 1995, vol. 1, pp. 169–172.
[2] R. O. Carlson, C. W. Eichelberger, R. J. Wojnarowski, L. M. Levinson, and J. E. Kohl, "A high density copper/polyimide overlay interconnection," in *Proc. 8th IEPS Int. Electron. Packag. Conf.,* 1988, pp. 793–804.
[3] P. D. Cooper, M. M. Fithian, R. J. Street, and W. P. Kornrumpf, "A C-band GaAs MMIC T/R module using microwave high-density-interconnect technology," in *Proc. 18th Govt. Microcircuit Appl. Conf.,* 1992, pp. 613–616.
[4] V. B. Krishnamurthy, H. S. Cole, and T. Sitnik-Nieters, "Use of BCB in high frequency MCM interconnects," in *IEEE Trans. Comp., Packag., Manufact. Technol.,* vol. 19, pp. 42–47, Feb. 1996.
[5] P. Cooper, P. Piacente, and R. Street, "Multichip-on-flex plastic encapsulated MHDI-low cost substrateless manufacturing for microwave and millimeter wave modules," in *IEEE MTT-S Dig.,* June 1996, pp. 219–222.
[6] A. Pham, J. Laskar, V. Krishnamurthy, H. S Cole, and T. Sitnik-Nieters, "Ultra low loss millimeter wave MCM interconnects," in *Proc. IEEE 6th EPEP Dig.,* Oct. 1997, pp. 213–216.
[7] Sonnet Software, Inc., 1020 Seventh North Street, Suite 210, Liverpool, NY 13088.
[8] A. Pham, J. Laskar, S. Basu, and J. Pence, "Comparison of air coplanar microprobes for on-wafer measurements at W-band," in *IEEE MTT-S Dig.,* June 1997, pp. 1659–1662.
[9] Cascade Microtech, Inc., 14255 S.W. Brigadoon Court, Beaverton, OR 97005.
[10] E. J. Denlinger, "Losses of microstrip lines," *IEEE Trans. Microwave Theory Tech.,* vol. MTT-28, pp. 513–522, June 1980.
[11] H. A. Wheeler, "Formulas for the skin effect," in *Proc. IRE,* 1942, vol. 30, pp. 412–424.
[12] M. Nakatsugawa *et al.*, "Line-loss and size reduction techniques for millimeter-wave RF front-end boards by using a polyimide/alumina-ceramic multilayer configuration," *IEEE Trans. Microwave Theory Tech.,* vol. 45, pp. 2308–2315, 1997.
[13] T. Wang, J. R. Mautz, and R. F. Harrington, "The excess capacitance of a microstrip via in a dielectric substrate," *IEEE Trans. Computer-Aided Design,* vol. 9, pp. 48–56, Jan. 1990.
[14] A. Pham, J. Laskar, and J. Schappacher, "Development of on-wafer microstrip characterization techniques," in *Proc. IEEE 47th ARFTG Dig.,* June 1996, pp. 85–94.
[15] T. Krems, W. H. Haydl, H. Massler, and J. Ruediger, "Advantages of flip chip technology in millimeter-wave packaging," in *IEEE MTT-S Dig.,* June 1997, vol. 1, pp. 987–990.

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