

# On the Feasibility of CMOS Multiband Phase Shifters for Multiple-Antenna Transmitters

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**Abstract**—We present the design of an integrated multiband phase shifter in RF CMOS technology for phased array transmitters. The phase shifter has an embedded classical distributed amplifier for loss compensation. The phase shifter achieves a more than  $180^\circ$  phase tuning range in a 2.4-GHz band and a measured more than  $360^\circ$  phase tuning range in both 3.5-GHz and 5.8-GHz bands. The return loss is less than  $-10$  dB at all conditions. The feasibility for transmitter applications is verified through measurements. The output power at a 1-dB compression point ( $P_{1\text{ dB}}$ ) is as high as 0.4 dBm at 2.4 GHz. The relative phase deviation around  $P_{1\text{ dB}}$  is less than  $3^\circ$ . The design is implemented in  $0.18\text{-}\mu\text{m}$  RF CMOS technology, and the chip size is  $1200\ \mu\text{m} \times 2300\ \mu\text{m}$  including pads.

**Index Terms**—Adaptive arrays, CMOS analog integrated circuits, distributed amplifiers (DAs), phase shifters, radio transmitters.

## I. INTRODUCTION

MULTIPLE-ANTENNA schemes have recently gained attention for the development of high speed wireless applications. By controlling the time/phase delay and gain of the signal in each antenna path independently, multiple-antenna systems can improve the signal-to-noise ratio, and the requirements on power amplifiers (PA) can be also relaxed through spatial power combining. Therefore, multiantenna systems are quite attractive for fully integrated transmitter scheme (Fig. 1) in CMOS technology [1], where the breakdown voltage of transistors degrades with the technology scaling-down. As key elements of phased array antennas, RF phase shifters have been recently implemented in silicon integrated circuits [2]–[5], while low  $Q$ -factor passive devices and a small tuning ratio of varactor capacitance (typically  $2\sim 4$ ) in CMOS represent challenges in the implementation of multiband continuous phase shifters with low loss and large phase tuning ranges [4]. Furthermore, a phase shifter has to meet the specified linearity requirement for transmitter applications preceding the power amplifier, which typically requires 0 dBm linear input power.

The first CMOS multiband phase shifter with effective continuous phase tuning over 2.4 to 6 GHz was previously reported by the authors in [5], where an embedded cascaded single-stage

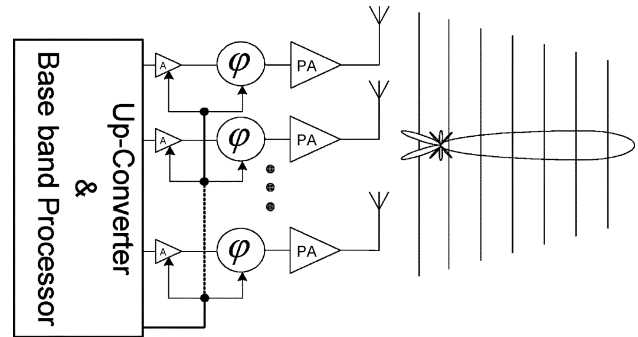


Fig. 1. Phased array transmitter.

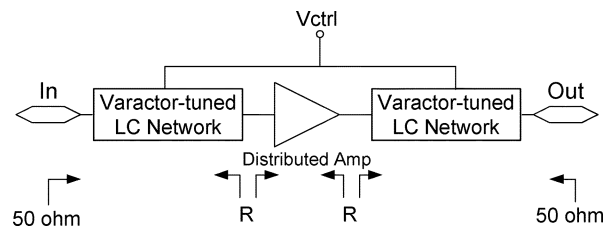


Fig. 2. Multiband phase shifter topology [5].

distributed amplifier (CSSDA) is employed for loss compensation. In this letter, we present a new design, which employs a classical distributed amplifier (DA) [6], aimed for transmitter applications. The phase shifter achieves a measured continuous  $180^\circ$  and  $360^\circ$  phase tuning range at 2.4-GHz and 3.5/5.8-GHz bands, respectively. The gain is as high as 4.35 dB and the return loss is less than  $-10$  dB from 2.4 to 6 GHz. The phase shifter achieves minimum 0.44-dBm output  $P_{1\text{ dB}}$  at 2.4 GHz. The relative phase deviation at  $P_{1\text{ dB}}$  is less than  $3^\circ$ , and this indicates the phase shifter can achieve accurate phase control under large signal operations.

## II. PHASE SHIFTER CIRCUIT

The phase shifter topology is shown in Fig. 2, where two varactor-tuned  $LC$  networks have been designed to provide both phase shifting and broadband impedance matching. The impedance matching networks allow the distributed amplifier to have high input and output impedance for the increase of transmission gain, and the loss compensation can be enhanced without the penalty of more power consumption. The new design in this work employs a classical distributed amplifier (DA), instead of CSSDA in [5], which are shown in Fig. 3.

### A. DA Versus CSSDA

The schematic diagrams of CSSDA and DA are shown in Fig. 3. In both topologies, the gate and drain capacitances are syn-

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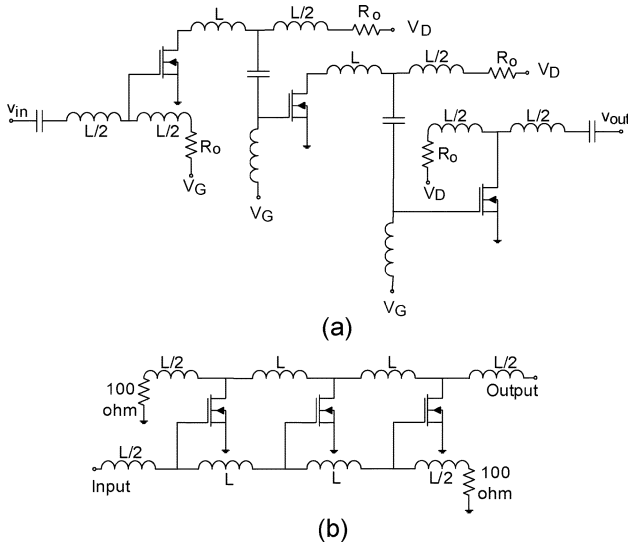


Fig. 3. Schematic diagrams of (a) CSSDA and (b) DA.

thesized in parallel to form artificial transmission lines, namely gate and drain lines, and therefore the amplifier can have a wide bandwidth.

For frequencies far below the cutoff frequency, the gain of CSSDA and DA can be simplified as (1) and (2)

$$G_{\text{CSSDA}} = \frac{1}{2} g_m^N (Z_g Z_d)^{\frac{N}{2}}, \quad (1)$$

$$G_{\text{DA}} = \frac{1}{2} N g_m (Z_g Z_d)^{\frac{1}{2}} \quad (2)$$

where  $Z_g$  and  $Z_d$  stand for the characteristic impedance of gate line and drain line, respectively, and  $g_m$  is the transconductance of transistors in each stage.

The gain of DA is proportional to the stage number  $N$ , while that of CSSDA is exponential to  $N$ . The inferiority of DA in terms of transmission gain mainly comes from the additive nature of the classical distributed amplifier, where the output currents from each individual stage are combined in an additive manner at the output terminal. However, it is the additive current nature that enables DA to yield higher linearity than a CSSDA with the equivalent power consumption. Therefore, a classical distributed amplifier (DA), instead of CSSDA, is employed in this work for transmitter applications where linearity is more concerned.

### B. Loss Compensation

As seen from (2), the concept of [5] still holds, and the characteristic impedance ( $Z_g$  and  $Z_d$ ) of gate and drain lines can be increased for achieving higher gain without the penalty of consuming more power. If we define the impedance transformation ratio  $r = Z/50$ , the power consumption of distributed amplifiers can be theoretically reduced by  $r$  times for the same gain compared with  $r = 1$  for  $Z = 50 \Omega$  design. We design  $R = 100 \Omega$  (Fig. 2), and two varactor-tuned  $LC$  networks provides both phase tuning and broad impedance transforming between  $50 \Omega$  and  $100 \Omega$ .

The simulated gain of the three-stage distributed amplifier is 11 dB for frequencies up to 8 GHz. The distributed amplifier draws 32-mA current from 1.8-V power supply.

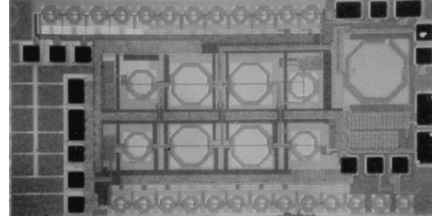


Fig. 4. Die photograph of the multiband phase shifter.

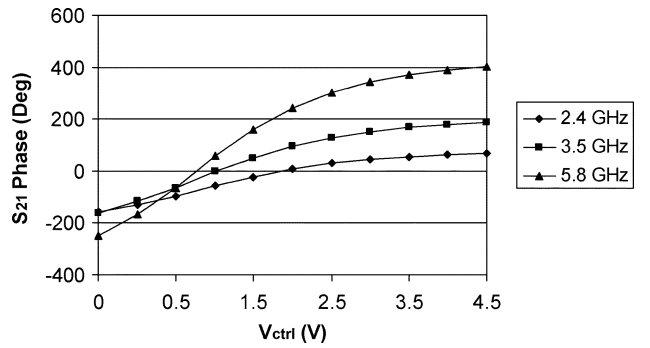


Fig. 5. Measured transmission phase versus control voltage.

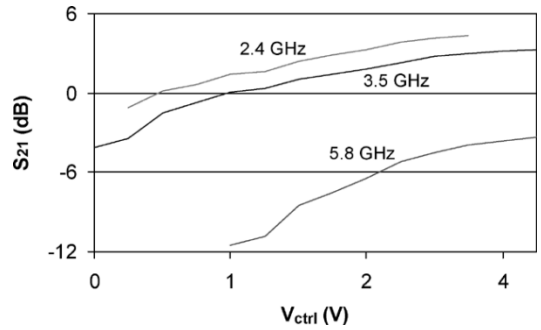


Fig. 6. Measured insertion loss versus control voltage at 2.4 GHz, 3.5 GHz, and 5.8 GHz.

## III. MEASUREMENT RESULTS OF PHASE SHIFTERS

The phase shifter was implemented with IBM 180 nm RF CMOS technology. The chip size is  $2.3 \text{ mm} \times 1.2 \text{ mm}$  including pads, and the die photograph is shown in Fig. 4.

### A. S-Parameter Measurements

$S$ -parameter measurements were conducted at room temperature using a Cascade Microtech probe station and an Agilent E8364B Performance Network Analyzer.

The  $S_{21}$  measurements were focused on three frequency bands: 2.4 GHz, 3.5 GHz, and 5.8 GHz, and the measured relative phase tuning ranges with  $V_{\text{ctrl}}$  from 0 to 4.5 V are  $220^\circ$ ,  $360^\circ$ , and  $650^\circ$ , respectively (Fig. 5). For the same control voltage range, the return loss is less than  $-10$  dB from 2.4 to 6 GHz.

As shown in Fig. 6, the insertion loss in a 2.4-GHz band varies from  $-1.05$  dB to 4.35 dB gain for  $180^\circ$  phase tuning. The insertion loss varies from  $-4.10$  dB to 3.27 dB gain in a 3.5-GHz band, and  $-11.5$  dB to  $-3.35$  dB in a 5.8-GHz band for  $360^\circ$  phase tuning, respectively. The corresponding control voltage ranges are also shown in Fig. 6 for each frequency band. The insertion

TABLE I  
OUTPUT POWER AT 1-dB COMPRESSION POINT AND OIP3 (dBm)

| Freq.   | $P_{1dB}$ | OIP3 |
|---------|-----------|------|
| 2.4 GHz | 0.44      | 9.8  |
| 3.5 GHz | -3.24     | 7.26 |
| 5.8 GHz | -4.74     | 5.68 |

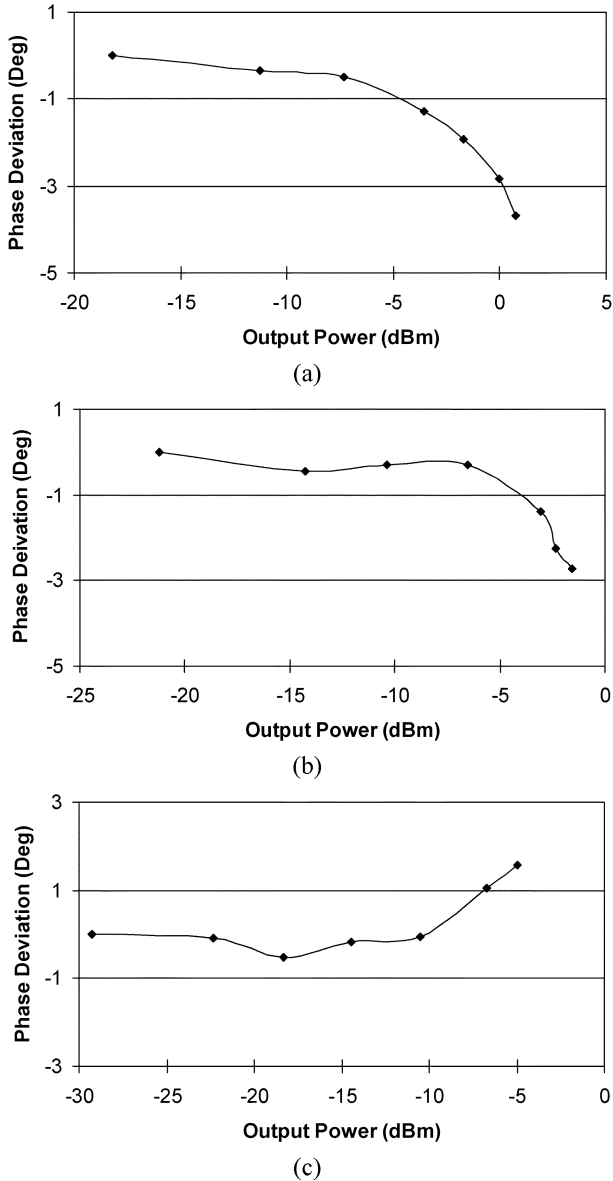


Fig. 7. Relative phase deviation versus output power at (a) 2.4 GHz, (b) 3.5 GHz, and (c) 5.8 GHz.

loss resulting from the lossy passive components has been significantly compensated by the embedded amplifier. The insertion loss variation within a 20-MHz bandwidth is less than  $\pm 0.1$  dB.

### B. Linearity

For transmitter application, the linearity of the phase shifter is also an important specification. Both  $P_{1dB}$  and IP3 have been measured, and the measurement results under worst conditions

through the whole phase tuning range are listed in Table I. The phase shifter can deliver 0.44-dBm output power at 2.4 GHz, and the output IP3 is up to 9.8 dBm. The linearity slightly degrades as frequency.

The phase error determines the directivity accuracy of a multi-antenna system. AM-PM measurement was conducted to provide a rough roadmap for phase deviation under large signal operation. Fig. 7 shows the relative phase deviation versus output power at 2.4 GHz, 3.5 GHz, and 5.8 GHz. The phase deviation is less than  $3^\circ$  until the output power reaches the 1-dB compression point. This indicates that the phase shifter can still achieve accurate phase control under large signal operations, and is therefore suitable for transmitter applications.

### C. Discussion

The insertion loss variation during phase tuning can be compensated through a preceding attenuator, and the attenuator is controlled by a look-up table [3], [5], which stores the phase/loss information of the phase shifter and the corresponding control voltage for the attenuator.

The chip was also mounted on an evaluation board and measured with SMA connectors. The insertion loss degradation is less than 0.3 dB, and the phase tuning range decreases about  $10^\circ$ . Furthermore, the simulation including the parasitics of bondwires and QFN package [7] shows less than 0.1-dB degradation of insertion loss. This indicates that the circuit is insensitive with package.

## IV. CONCLUSION

This letter presents a multiband phase shifter in 180-nm CMOS technology aiming for integrated multiple-antenna systems. The measurement results show this design can achieve more than  $180^\circ$  tuning range and usable over 2.4 to 6 GHz bands. The phase shifter is capable of delivering minimum 0.44-dBm linear output power at 2.4 GHz, and the phase deviation is less than  $3^\circ$  at a 1-dB compression point.

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