

## Info about Cadence Tools & Documentation:

### 1. IC50:

The different tools available in the **IC50** DFII environment for Digital, Analog and Mixed signal design are as follows:

Virtuoso(R) Schematic Composer VHDL Interface [5.0]  
Virtuoso(R) Schematic Composer Verilog(R) Interface [5.0]  
Virtuoso(R) Schematic Composer HSPICE Interface [5.0]  
Virtuoso(R)-XL Layout Editor [5.0]  
Virtuoso(R) Compactor [5.0]  
Cadence(R) Analog Oasis Run-Time Option [5.0]  
Cadence(R) Electronic Design for Manufacturability Option [5.0]  
Cadence(R) SPICE [5.0]  
Spectre(R) Circuit Simulator [5.0]  
Spectre(R)-RF Simulation Option [5.0]  
Cadence(R) Analog HSPICE Interface Option [5.0]  
Virtuoso(R) Schematic Composer [5.0]  
Cadence(R) Analog Design Environment [5.0]  
Dracula(R) Graphical User Interface [5.0]  
Virtuoso(R) Schematic Composer to design compiler integration [5.0]  
Cadence(R) RC Network Reducer Option [3.0]  
Cadence(R) AMS Designer Environment [5.0]  
Dracula(R) Physical Verification and Extraction Suite [4.9]  
Diva(R) Physical Verification and Extraction Suite [5.0]  
Cadence(R) SKILL Development Environment [CAT 97B]  
Virtuoso(R) EDIF 200 Reader [5.0]  
Virtuoso(R) EDIF 300 Connectivity Reader/Writer [5.0]  
Virtuoso(R) EDIF 300 Schematic Reader/Writer [5.0]

These can be summarized as:

	<b>Executable</b>	<b>Tasks</b>
Front End		
	icde	Basic digital and analog design entry
	icds	Front-end design (icde plus digital design environment
	icms	Front-end analog, mixed signal, and microwave design (icds plus analog, mixed signal, and microwave environment and Diva LVS)
	icca	Front-end design with floor planning (icds)
Layout		
	layout	Basic layout design with interactive DRC
	layoutPlus	Basic layout design with automated design tools and interactive verification (layout plus, Virtuoso® Compactor, Diva, InQuery, VXL)
Place and Route Systems		
	icca	Cell-based chip assembly
	msfb	Mixed-signal IC design. Excludes Place and Route software
	icfb	Front-to-back design (includes most Cadence tools) Chip Finishing
	vce	Chip finishing for custom and digital designs using SoC Encounter and the Virtuoso Chip Editor on Open Access.

As mentioned above, all the front-end and backend tools can be invoked into a single environment by using the command "icfb".  
All the above binaries are stored at "common/pkg/cadence/IC50/tools.hppa/dfll/bin"

## **2. DSM SE5.3: (For Place and Route)**

Silicon Ensemble-Gate Ensemble(R)-Ultra Place-and-Route

Binaries/Executable: /usr/pkg/cadence/DSME53/tools/dsm/bin/se24

## **3. SPR: (Synthesis, Place and Route)**

Buildgates Extreme Synthesis

Binaries/Executable: /usr/pkg/cadence/SPR50/BuildGates/v05.00-p008/bin/pks\_shell

## **4. LDV:**

Cadence(R) Simulation Analysis Environment [4.1]  
Cadence(R) NC-Sim Mixed-Language Simulator [4.1]  
Cadence(R) NC-Verilog(R) Simulator [4.1]  
Cadence(R) NC-VHDL Simulator [4.1]  
Cadence(R) Verification Cockpit [4.1]  
Cadence(R) AMS Designer Simulator [4.1]

Binaries/Executable: /usr/pkg/cadence/LDV41/tools/dsm/bin/ncvlog

## **5. SOC:**

Cadence(R) First Encounter Ultra [2002.3]  
Silicon Ensemble(TM)-PKS Optimization [1.1]

Binaries/Executable: /usr/pkg/cadence/SOC23/tools/dsm/bin/ncvlog

## **6. CADMOS:**

CM00100: PaciflC Static Noise Analyzer for Custom Digital ICs [4.0]  
CM00200: SeismlC Substrate Noise Analyzer for Mixed Signal ICs [4.0]  
CM00300: CeltlC Crosstalk Analyzer for Cell-based Designs [4.0]

Binaries/Executable: /usr/pkg/cadence/CADMOS41/

## **7. ICC:**

Virtuoso(R) Custom Placer [11.0]  
Virtuoso(R) Custom Router [11.0]  
Cadence(R) Chip Assembly Router [11.0]

Binaries/Executable: /usr/pkg/cadence/ICC110/

## **8. NEOCELL:**

NeoCell Analog Physical Synthesis

Binaries/Executable: /usr/pkg/cadence/NEOCELL31/

## **9. SPW:**

SPW Wideband CDMA Library [4.8]  
SPW Communication Library [4.8]  
SPW GSM Verification Environment [4.8] SPWLTI [4.8]

SPW IS136 Verification Environment [4.8] SPW Multimedia Design Kit [4.8]  
Cadence(R) SPW Model Manager [4.8]  
Cadence(R) Signal Processing Worksystem link to NC Simulators [4.8]  
SPW PCS CDMA Verification Environment [4.8]  
SPW WLAN Library [4.8]

Binaries/Executable: /usr/pkg/cadence/SPW481/

#### **10. PSD:**

For PCB

Binaries/Executable: /usr/pkg/cadence/PSD142

#### **Documentation:**

Use the command "cdsdoc" in unix shell to invoke the documentation.

Here are some related docs.

1. Composer - NC Verilog Integration for Composer User Guide  
- Verilog-XL Integration for Composer User Guide
2. DFII
3. Virtuoso Layout Editor
4. Cadence to Synopsys Interface User Guide

#### **Verilog Simulator**

There are two ways to use Verilog, either through DFII environment OR using the LDV binaries.

DFII:

- After opening the DFII env by using "icfb" command, create a new library. In this library, create a cellview for *Verilog Editor* and a cellview for *Schematic*. You can write your code in verilog Editor.
- From the schematic window, use *Tools - Simulation - VerilogXL* to open the VerilogXL simulation window. OR you can open NCVerilog simulation window. Cadence has two Verilog simulators. NCVerilog is the new version and is faster.

LDV: Compile the Verilog code using the executable  
/usr/pkg/cadence/LDV41/tools/dsm/bin/ncvlog

#### **Synthesis:**

BuildGates is the Synthesizer of Cadence.

Executable: /usr/pkg/cadence/SPR50/BuildGates/v05.00-p008/bin/pks\_shell  
Run the synthesis script in this shell.