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Porous Silicon Coated With Ultra-Thin Diamond-Like Carbon Film Cathodes

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ABSTRACT

The main requirements to electron field emission cathodes are their efficiency, stability and uniformity. In this work we combined the properties of porous silicon layers and diamond-like carbon (DLC) film to obtain emission cathodes with improved parameters. The layered structures of porous silicon and DLC film were formed both on flat n-Si surface and silicon tips created by chemical etching. The conditions of the anodic and stain etching of silicon in HF containing solution under the illumination have been widely changed. The influence of thin (≤10nm) DLC film coating of the porous silicon layer on electron emission has been investigated. The parameters of emission efficiency such as field enhancement coefficient, effective emission areas and threshold voltages have been estimated from current-voltage dependencies to compare and characterize different layered structures. The improvement of the emission efficiency of silicon tip arrays with porous layers coated with thin DLC film has been observed. These silicon-based structures are promising for flat panel display applications.

INTRODUCTION

There are many investigations directed toward the improvement of the emission properties of cathodes. For low voltage applications the tip radii should be made very small in order to achieve a high field enhancement coefficient. The processes required to manufacture very sharp and uniform emitters are relatively complicated. The porous silicon (PS) layers are perspective for the improvement of electron field emission. The stability of the emission current as well as its density can be increased and the applied voltage can be decreased for silicon cathodes by depositing or forming a PS layer on their surface [1–6]. The lowering of the emission voltage is caused by the electric field enhancement due to the presence of the sharp asperities (also referred as fibrils or protrusions) of porous silicon. Due to the variation of the formation conditions the density of asperities, which act as separate emission centers, can be in the range of 10^8–10^{11} asperities per mm^2 [1].

On the other hand, due to the distribution of radii of the tips in the array most of the emission current flows through the tips having small radii. If the tip is very small its thermal resistance is very high and the equilibrium temperature necessary to dissipate the power may be greater than the melting point [7]. As a result some tips can be overheated and blunted. In the case of porous layer on the silicon tip surface the blunting and destruction of some asperities does not influence the emission significantly since other asperities can begin to contribute to the emission process.

One of the restrictions for broad application of porous silicon for field emission is connected with the instability of properties of this material. In the process of formation of the porous layer on the silicon surface the latter is contaminated with atoms of H, O, Si–H_2, Si–O–H groups etc. During the emitter operation under non-high-vacuum conditions or even

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during a long-term shelf storage different atoms and molecules penetrate into porous layer and change PS properties.

In this work the investigation of electron field emission from silicon tips with porous silicon layer on their surface has been performed. To improve the emission properties the tips with the porous layer were covered with the thin diamond-like carbon (DLC) film. DLC film is very suitable material for the field emission application due to its low work function, high chemical and mechanical stability as well as high thermal conductivity [8–9]. The ultrathin DLC film was used to minimize the influence of the atmosphere on the porous silicon properties.

EXPERIMENT

The electron field emission was investigated both from silicon tips with porous layer (with and without DLC coating) and from porous silicon formed on the flat wafer surface. The arrays of initial silicon emitter tips were fabricated using the method for formation of the silicon points by the wet chemical etching. The cathodes were formed on (100) Si n-type wafers (N_d=10^{15} cm^{-3}) by patterning with Si_3N_4 as a masking material. The tips sharpening was performed by oxidation of the as–etched tips at 900^{O}C in wet oxygen. After the oxidation the oxide was removed in HF:H_2O solution. This sharpening technique allowed the production of tips with the curvature radius of 10–20 nm. The height of the silicon tips was about 4 μm. The tips density was 2.5×10^5 tips/cm^2. The radii were estimated by scanning electron microscopy (SEM).

Polysilicon was formed by two different methods, namely, by electrochemical anodisation and pure chemical etching in buffering solutions.

By the electrochemical method porous silicon was formed on silicon tips as well as on the flat wafer surfaces. The electrolyte composition was 1:1 of 48% HF and ethanol. The anodisation process was conducted under illumination with the intensity of 30 mW/cm^2 for holes generation in n-type silicon. The anodisation current density and the etching time varied from 5 to 50 mA/cm^2 and from 15 to 60 s respectively. The thickness of obtained porous layers increased with the time of anodic etching while the pores size and, hence, the porosity of the layers increased with the anodisation current density [10].

During chemical (stain) etching the polysilicon layer was formed in the HF:HNO_3:H_2O solution. In this case the content of nitric acid determined the degree of porosity. The effect of etching time was also studied. The chemical etching is simpler than the electrochemical and, therefore, could be more suitable for practical applications [11].

The ultrathin DLC film of ~100Å thick was deposited on the porous silicon by the method of plasma enhanced chemical vapor deposition (PE CVD) from CH_4:H_2 mixture. The gas pressure in the chamber was 0.4 Torr and applied bias was 1800 V. The substrate temperature during film deposition was 60^{O}C.

The measurements of the emission current from samples were performed in a vacuum system that could be pumped out to the stable pressure of 10^{-6} Torr. The emission current was measured at the ungated cathode-anode diode structure. The emitter-anode spacing L was kept equal to 20 μm for all the experiments. We fabricated a test diode structures by the sandwiching anode and cathode plates. A silicon wafer was used as a cathode and a molybdenum wire was used as an anode. The emission current–voltage characteristics were obtained with the current sensitivity of 5 nA over the voltage range up to 1500 V. A 0.56 MΩ resistor was placed in series with the cathode to provide short-circuit protection.

The thickness and refractive index of the DLC films on flat silicon surface of the wafers were measured with the laser ellipsometer (λ=632.8 nm).

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RESULTS AND DISCUSSION

The typical SEM micrographs of silicon tip without and with PS layer are shown in Fig. 1. The view of PS layer at high magnification is also shown. As can be seen after anodization the top of tip is blunted, but the tip surface has more developed micro-morphology. Many asperities are observed.

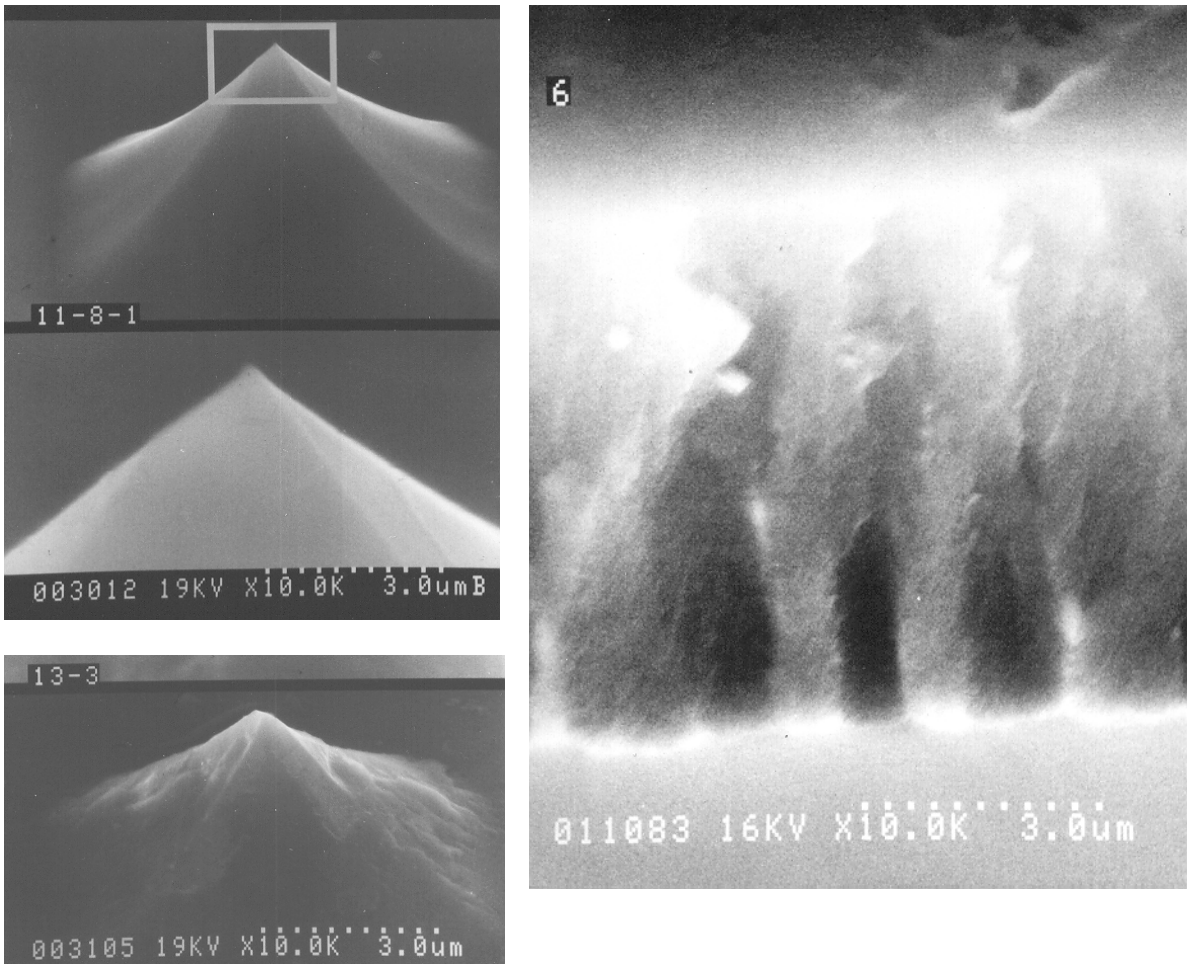

Figure 1. SEM micrographs of silicon tips without (a) and with PS layer (b). (c) – enlarged image of the PS layer.

The current-voltage characteristics and corresponding Fowler-Nordheim plots of electron field emission from silicon tip array with PS layer coated with thin DLC film and arrays without coating are shown in Fig. 2. As can be observed the coating with ultra-thin DLC film helps to decrease the threshold voltages significantly. The threshold voltage of silicon tips without PS layer was 530 V. Depending on porous silicon preparation conditions two types of curves, namely, a smooth curve and a curve with peaks, are obtained. The possible mechanism for the peaks appearance can be connected with high-field reconstruction of the porous silicon layer.

For the explanation of experimental results and their comparison for different samples we have determined the emitting areas α of 7.5×10^3 tip array from Fowler-Nordheim plots

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according to procedure described in [12, 13]. By forming the porous silicon layer we create asperities on silicon surface and, therefore, increase the emitting area in comparison to one for untreated silicon tip. Increase of emission area by factor of 1.5-2.5 versus anodization time (at fixed etching current density j=25 mA×cm^{-2}) is observed for etching times up to 30 s.

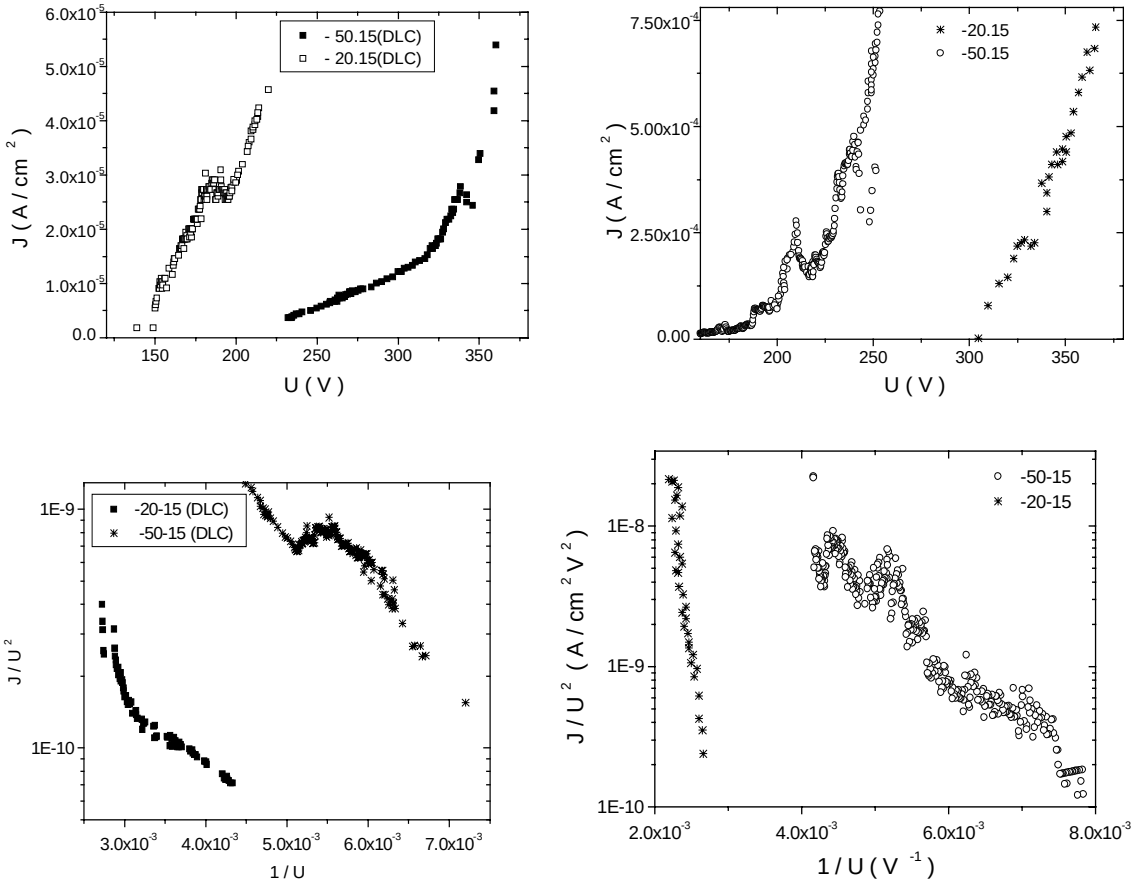

Figure 2.
Current-voltage (upper graphs) and Fowler-Nordheim (lower graphs) characteristics of electron field emission from Si tips arrays with PS layer covered with DLC (left) and without DLC coating (right). The two regimes of PS formation are: 20 and 50 mA/cm^2, both for 15 s.

Experimental dependences of electron field emission threshold voltage (V_{th}) were measured for different anodization currents and etching times used to form the porous silicon layer. The influence of current density on V_{th} and the effect of thin DLC film coating is shown in Fig. 3. Short-term stability of electron field emission current for tip array with the porous silicon layer is shown in Fig. 4. The coating of the tips with thin DLC film resulted in significant improvement of the emission stability for measured current levels up to 50 μA. We believe that the coating of PS layer with thin DLC film allows to protect pores of PS layer from penetration of atoms and molecules of residual gases and their interaction with porous silicon layer. As a result the emission properties of porous silicon layer are stabilized. In addition, the DLC films deposited under conditions described above have lower work function in comparison with untreated porous silicon. A shift of the threshold voltages into a lower voltage region, corresponding to increased porosity of the silicon layer with increased etching time, is observed.

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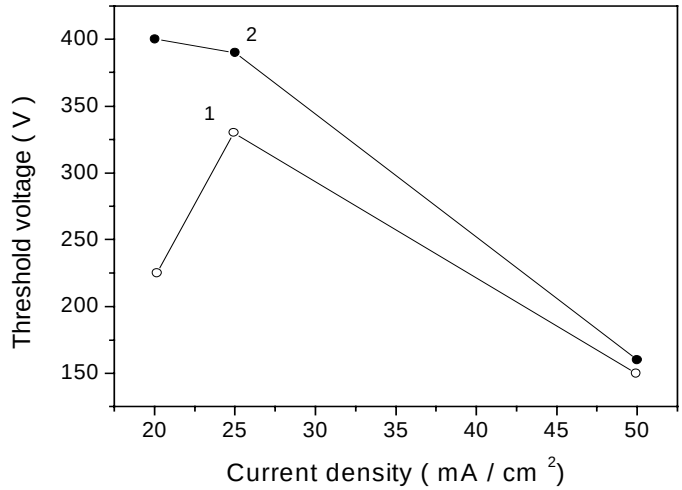

Figure 3.
Dependence of the threshold voltage (V_{th}) for Si tip array on the etching current density: (1) tips coated with porous silicon layer; (2) same tips coated with additional DLC layer.

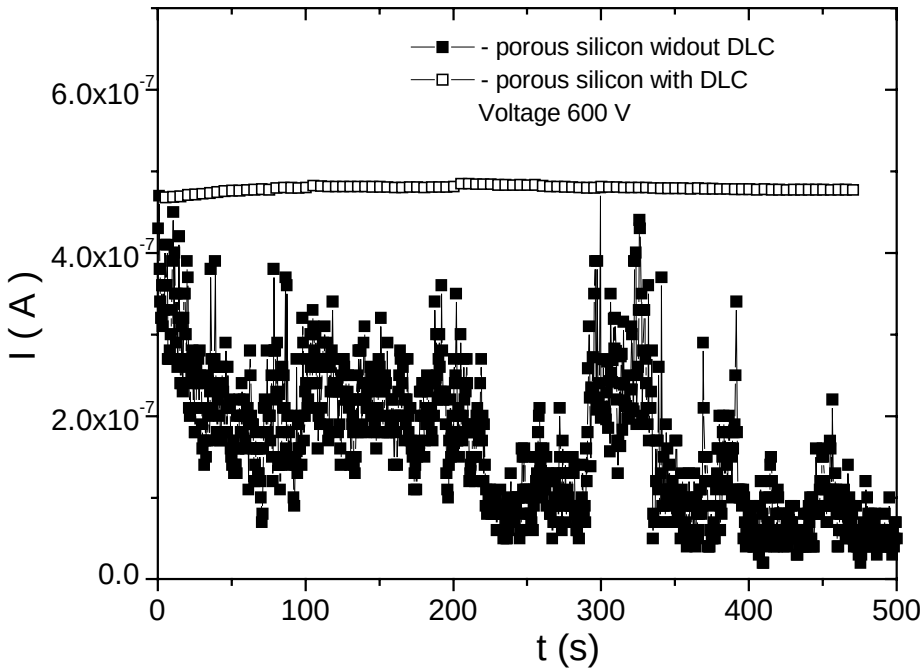

Figure 4. Time stability of electron field emission from Si tips with porous silicon layer.

CONCLUSION

The electron field emission from silicon tip array with porous silicon layer on the surface and influence of DLC coating have been investigated. The PS layers were prepared in various conditions using electrochemical etching and chemical etching. It was shown that conditions of PS growth influence on emission parameters significantly. The coating of PS layer with thin DLC film allowed to improve efficiency and stability of electron field emission.

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