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Fabrication and Characterization of Singly-Addressable Arrays of Polysilicon Field-Emission Cathodes.

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ABSTRACT

Polysilicon is a promising candidate material for field-emission microelectronics devices. It can be competitive for large-size, cost-sensitive applications such as flat-panel displays and micro electro-mechanical systems. Singly-addressable arrays of field-emission cells were fabricated in a matrix configuration using a subtractive process on Polysilicon-On-Insulator substrates. Matrix rows were fabricated as insulated polycrystalline silicon strips with sharp emission tips; and matrix columns were deposited as gold thin film electrodes with round gate openings. Ion implantation has been used to provide the required conductivity of the poly-Si layer. To reduce radius of curvature of the polysilicon tips, a sharpening oxidation process was used. The final device had polysilicon emission tips with end radii smaller than 15 nm, surrounded by gate apertures of 0.4 μm in diameter. Field emission properties of the cathodes were measured at a pressure of about 10^{-8} Torr, to emulate vacuum conditions available in sealed vacuum microelectronics devices. It was found that an emission current of 1 nA appears at a gate voltage of 25 V and can be increased up to 1μA at 70 V. Over this range of current, no "semiconductor" deviation from the Fowler-Nordheim equation was observed. I-V characteristics measured in cells of a 10x10 matrix, with a cell spacing of 50 μm demonstrated good uniformity and reproducibility.

INTRODUCTION

Low-voltage field-emission cathodes are a promising type of electron source for vacuum microelectronics devices. During the last ten years, a broad collection of new emissive materials such as diamond and diamond-like carbon, compound semiconductors, noble metals, etc., have been used for field-emission cathode fabrication. Single crystal silicon, because of its advantages in VLSI technology still remains one of the most frequently used materials for many applications including flat-panel display, multi-beam lithography, microscopy, and data-storage devices [1,2]. However as the size of the single-crystal Si substrates increases, the factors related to manufacturing cost and technological complexity impose further limitation on fabrication of the cathodes for flat-panel displays and micro electro-mechanical systems. Polycrystalline silicon may be considered as a good alternative to single crystalline silicon because it can be cost-effectively deposited over larger size dielectric substrates and still be compatible with traditional semiconductor manufacturing methods.
Recently, it was found by E. Boswell and colleagues in diode emission tests, that the polycrystalline silicon field emitters fabricated using wet etching method, exhibit an emission behavior similar to single crystal silicon emitters [3]. It was observed that the oxidation sharpening had little effect on the field-emission characteristics due to the presence of sharp emitting silicon tips in a polycrystalline material. In a structure fabricated by H. Uh and others, both single and polysilicon gated field-emission arrays were fabricated on oxidized silicon

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substrates using RIE etching and sharpening oxidation. Stable emission currents of 0.1 μA/tip were measured at 82 V for polycrystalline tips with a gate aperture of 1.2 μm and at 80 V for single-crystal tips with gate aperture 1.6 μm [4]. This result is similar to the data obtained previously from excellent, uniform, very-low turn-on voltage single crystal silicon field emission arrays described by M.Ding et al [5].
In this paper we present a new version of a low-cost and dependable method of fabrication of singly-addressable arrays for multi-beam vacuum microelectronics device applications.

EXPERIMENTAL DETAILS

The singly-addressable field-emission cathodes matrix consist of polysilicon "stripes" in which the emission tips are formed, over coated with oxide and having metal stripes, perpendicular to the polysilicon lines, which is used to form the gates.
The fabrication process requires a silicon-oxide-silicon structure consisting of a silicon substrate with at least 1 μm of oxide and 3 μm of polycrystalline silicon. Initial poly-silicon deposition techniques, performed at standard 620 C°, resulted in a surface with significant roughness and large silicon grain size. This influenced the minimum feature size obtainable (we use Karl Suss MA-6 vacuum contact lithography) and had a negative effect on the shape and geometry of the silicon tips. To reduce the grain size and to provide a more smooth coating, we lowered the deposition temperature to the lower value of 590 C°.
The initial resistivity of the polycrystalline silicon layer exceeded 100 kΩ-cm, which was excessively high for our application. To reduce the resistivity, the layer of polysilicon was doped by phosphor ion implantation using a dose of 3×10^{14} cm^{-2} at of 80 keV. No subsequent annealing was performed. The polysilicon was oxidized with total time 2 hours at 1100°C to obtain a 0.15 μm thick SiO_2 layer. The oxidation time was sufficient for annealing and impurity activation. After oxidation, the measured bulk resistivity of the polysilicon layer was close to 3 Ω-cm and the sheet resistance was 10 kΩ/ . This resistivity inherent to the polysilicon enabled us to obtain series resistors of 1 MΩ for each emission tip. The resistors proved to stabilize the field emission current from the individual tips, as expected.
Following the ion implantation step, the oxide layer was coated with 0.1 μm chromium to provide an etch mask. The process flow of the singly addressable array fabrication includes two chrome-oxide-polysilicon structure-etching steps. The first step produces a simple system of insulated polysilicon cathode stripes, which do not require high-resolution lithography. A variety of wet etching processes of chromium, silicon dioxide and polysilicon layers were tested for obtaining these stripes. Good results were obtained, including tilted sidewalls of the polysilicon stripes in which the cathodes are later etched. The cross-section shape provided effective step-coverage of the cathode stripes afterward with the gate metal layer. Although dry etching of polysilicon was also investigated, the sidewalls were excessively vertical and it was found that wet etching resulted in better uniformity across a 4-inch wafer.
The second masking and etching step forms the tip portion of the cathode electrodes, leaving a 1 μm diameter chrome/oxide tip cap where the tip is to be formed. Because of the grain structure of polysilicon it is extremely important doing tip etching to use isotropic reactant. Plasma etching in a SF_6/O_2 gas mixture as well as pure SF_6 was attempted. It is found that pure SF_6 provides more smooth and uniform etching in comparison with mixtures using 10% and 50% O_2.

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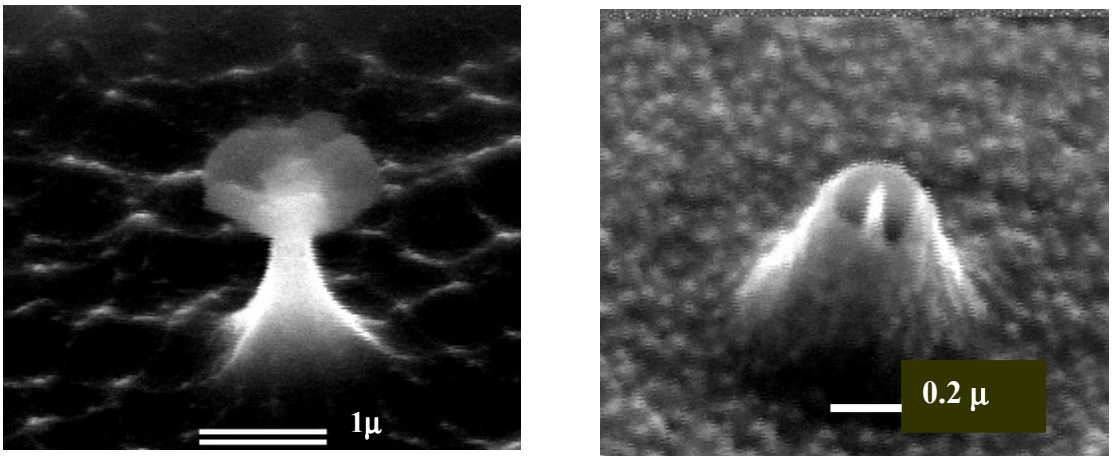

a) b)

Figure 1. a) Polycrystalline silicon tip before oxidation sharpening. Oxide cap is on top of the tip. b) A completed volcano-type field-emission cell, having 0.3 μ gate opening and approximately 15 nm tip curvature radii.

The tip etch is continue until the diameter of the narrowest part of the tip decreases down to 0.2 μm as it is shown on Fig.1. At this point oxidation sharpening is carried out. A combination of wet and dry oxygen is used because tip sharpening is more effective in dry oxygen at low temperature; however the oxidation time would be excessively long if only dry oxidation is used. This oxidation also increased the thickness of oxide on the surface of cathode stripes and reduced the gate-cathode current leakage.

The gold film used as a gate electrode was deposited by electron-beam evaporation using the method we have previously described elsewhere [6]. As a result, the gate metal is coated on the sidewall of the tip and is barely masked by the oxide cap. This method allows us to form the gate aperture, having a diameter of 0.3-0.4 μm using conventional optical lithography technology with resolution normally producing larger feature sizes. Tip caps were subsequently removed by wet etching of the silicon dioxide. The final "volcano-type" emission cell is shown in Fig.1b. The typical tip curvature radius is estimated using microscopy, to be on the order of 15 nm.

DISCUSSION.

We tested the electrical and emission properties of the cathodes in a matrix configuration. No electrical cross-leakage between the cathode stripes and the gate electrodes in air was observed (up to 10 V DC and 1 nA sensitivity). Field emission properties of the cathodes were measured in a vacuum chamber under a residual gas pressure of 10^{-8} Torr. Characterization was performed without bake out of the vacuum system. No tip conditioning or field forming steps was performed. The Hewlett-Packard 4142B modular DC source/monitor was used to acquire the emission data. The gate electrode was grounded, positive potential (up to 100 V) applied to stainless steal foil anode, and the cathode had a negative bias. Anode-cathode spacing was approximately 1 mm.

Figure 2a shows current-voltage characteristic, obtained from a single-cell cathode with a gate opening of 0.4 μm. It was found that emission current of 1 nA is first registered at a gate voltage 25 V, increasing to 10 nA at 30 V. The Fowler-Nordheim (FN) plot for this region is a straight line, as it shown on Fig. 2b. To achieve 1 μA we needed to increase the voltage between the tip

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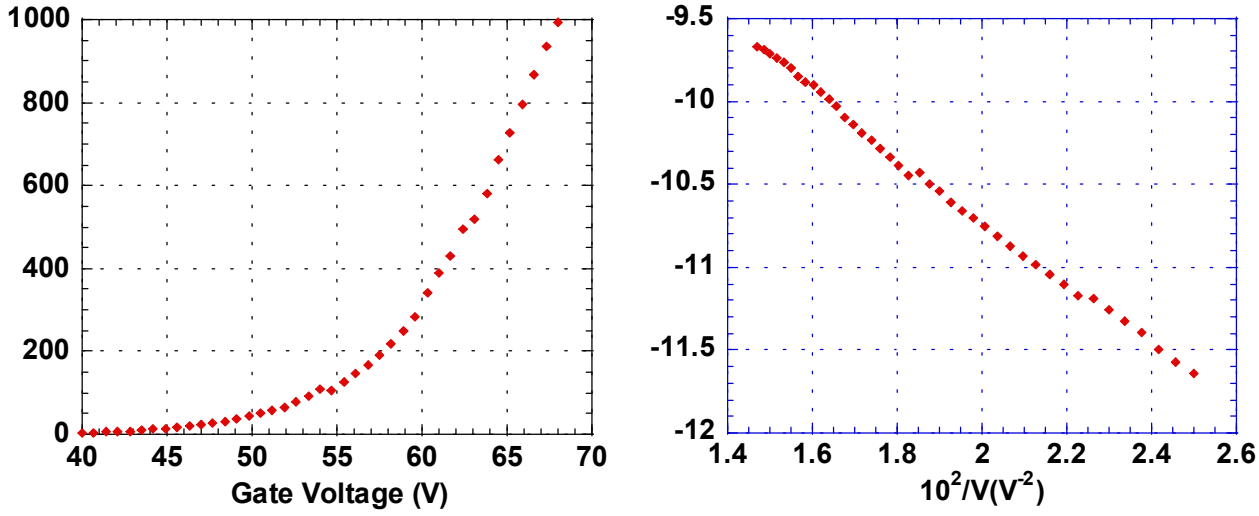

a) b)

Figure 2. a) Anode current vs. gate voltage plot and b) the Fowler-Nordheim plot for the anode current up to 1000 nA.

and the gate to 68 V. For the tested range of current no "semiconductor" deviation from Fowler-Nordheim equation was observed. We consider that combination of sufficient doping level within silicon grains and high sheet resistivity on the grain borders are responsible for this behavior. The minor shifts in the plot on Fig. 2b could be explained by fluctuations of emission current, which are usually significant for single tip field emitters. The dependence of the anode current varying with gate and anode voltage as a parameter (e.g. "triode characteristics") is shown in Fig. 3 Lifetime of an individual cathode cell was up to 200 hours. Several cathodes were damaged under attempts to extract and maintain maximum possible levels of emission current. It was observed that tip damage by emission current occurred under loading of 1.5 µA per tip. These attempts often resulted in the tip destructing, as shown in Fig. 4.

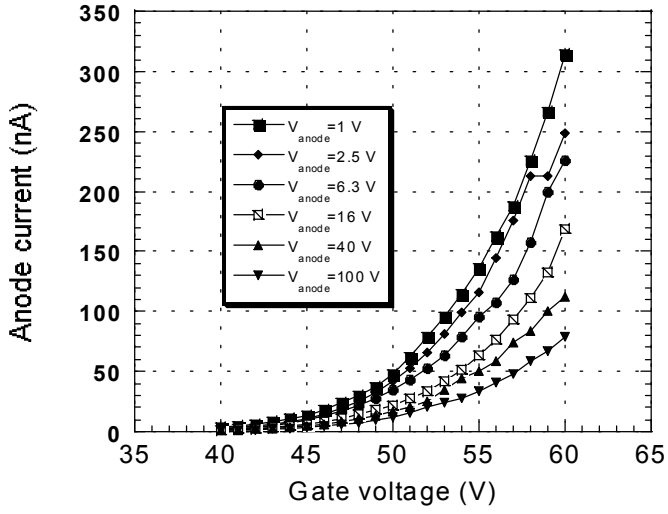

Figure 3. Anode current vs. gate voltage at different anode potentials relative to gate potential (e.g. "triode characteristics").

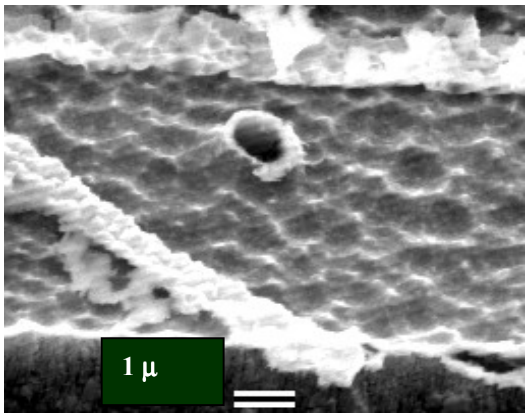

Figure 4. SEM picture showing an exploded cell, caused by excessive steady-state cathode current

High electrical and heat conductivity of the gold gate film and MΩ resistivity of cathode strip minimized damage of the structure, which is important for high-density matrix applications. I-V characteristics of separated cells in the 10x10 matrix, with the distance between adjacent emitters of 50 micron were tested demonstrating good uniformity and reproducibility. The emission current does not appear to be significantly affected by the random crystalline orientation of the emitting tip crystallite of each cathode.

CONCLUSION

Polycrystalline silicon on an insulated substrate is suitable for field-emission cathode fabrication instead of SOI wafers as it allows us to avoid the cost and size limitation.
We developed subtractive technology of singly-addressable cathode matrix fabrication, which provides a gate opening as small as 0.3 micron using contact lithography with a resolution of 1 micron. Loading resistors of any required resistance could be integrated with the cathode because of high intrinsic resistivity of polycrystalline silicon layer. An anisotropy of resistance of polycrystalline layer in lateral and orthogonal directions improve linearity of Fowler-Nordheim characteristics of the field-emission cathode.
The emission current up to 1 μA was extracted from a single tip at a gate voltage not exceeding 70 V.

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