Structure and Electrical Characteristics of Silicon Field-Emission Microelectronic Devices

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Abstract—**Field emission current is measured from arrays of wet chemically etched silicon cold-cathode diodes. Two types of cathode tips are measured both as-etched and after sharpening by low-temperature oxidation. The measurements are compared with results from simulations. The field enhancement increase resulting from tip sharpening is less than expected from simulation. The currents measured follow a Fowler–Nordheim characteristic and have been found temperature-insensitive from 130 to 360 K. Turn-on voltage is near 4 V, a value much less than measured from most other field emission sources. With a 920 nm anode–cathode spacing, a minimum 0.2-μA current per cathode is found. Telegraph noise of about 1% at 20 V is observed. These sharpened silicon tips are a viable cold cathode for vacuum microelectronics and other electron device applications.**

I. Introduction

COLD CATHODES which emit electrons via field emission, rather than thermionic emission, are considered useful for applications in vacuum microelectronics, electron-beam instrumentation, display technology, and microwave device technology. It is also believed that there is potential for application to circuitry requiring radiation and/or temperature insensitivity. A recent resurgence of interest in this topic [1], [2] has demonstrated a wide number of possibilities for fabrication of cold cathodes. The most established technique for making these cathodes is by deposition of metal, through a specially prepared shadow mask, to form precise microscopic whiskers; this structure is generally referred to as a "Spindt cathode," after the inventor [3]. Spindt cathodes have clearly been demonstrated to operate via the field emission process with a current density following a Fowler–Nordheim tunneling process equation

$$J = K_1 \frac{E^2}{\phi} \exp\left[-\frac{K_2 \phi^{3/2}}{E}\right] \tag{1}$$

where K_1 and K_2 are constants, ϕ is the work function of the emitting surface, and E is defined by

$$E = \frac{\beta V}{d} \tag{2}$$

where V is the anode–cathode voltage, and β is the "field enhancement factor," which is greater than one (e.g., the parallel-plate condition) in the case of a pointed cathode near a planar anode or grid, and d is the spacing between the cathode tip and the anode. The factor β is a function of cathode radius of curvature at the point of emission. To the first order, (1) is independent of temperature. These field emission cathodes can be used individually or in arrays. Typical Spindt cathodes need greater than 50-V applied bias to obtain currents $> \approx 1$ μA per tip.

We have recently explored the use of silicon field emission tips as an alternative to the Spindt cathode [4]. Silicon is well understood as a starting material for micromachining techniques. The work function of n-type silicon (4.2 eV) is comparable to the values used in some Spindt cathodes. It has also been demonstrated that silicon tips can be sharpened by a low-temperature oxidation process to near atomic dimensions, thereby dramatically reducing the emission surface radius of curvatuve and correspondingly increasing the field enhancement factor β [5]. Because silicon is the central material in the established IC process technology, it is believed that Si field emission tips can be integrated into circuits which contain standard MOS or bipolar support circuitry. Fabrication of a microtriode using exclusively standard Si IC processes was recently demonstrated [6].

This paper describes silicon cathodes fabricated by either anisotropic or isotropic wet chemical etching and operated in a diode configuration to experimentally verify field emission according to (1). Cathode characteristics are compared both as-etched and after low-temperature sharpening. Operation is verified over a range of temperatures. The expected field enhancement in both unsharpened and sharpened cathode tips is found by simulation and is compared with the measurements.

It is found that these cathodes do emit according to a Fowler–Nordheim tunneling characteristic and that the field enhancement does increase with sharpening of the tips, although not as great as the simulations project. The operation initiates at significantly lower voltages than

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other cathodes with comparable current densities. The emission is temperature-insensitive and operates with a reasonable noise level. Reproducible characteristics have been found between successive fabrication lots of cathodes.

II. Experiment

A. Cathode Formation

An extensive investigation of methods for forming silicon points by wet chemical etching was performed and has been reported elsewhere [7]. Two etching techniques from that study which give uniform results are used as the cathodes for this experimental work. Both are formed by patterning Si_3N_4 as a masking material on (001) Si n-type wafers ($N_D = 10^{16}$ cm^{-3}). The nitride masks are 10-μm squares; in an array form, these squares are spaced on 20-μm centers. In the first etching technique, the unmasked Si is etched in 10 molar KOH solution at 55°C with secondary butanol mixed in the solution to saturation. The etching process undercuts the Si_3N_4, selecting the {331} facets, leaving six-sided tip with a 54° side angle and an approximately 100-nm radius of curvature at the tip, as-etched. An array of these anisotropically etched tips, with some of the masks still in place, is shown in the SEM photograph of Fig. 1(a). The etch was at the point where the undercut was just complete and some of the masks had already been dislodged during the ensuing handling. Any further etching results in tip rounding which remains even after the tip sharpening procedure.

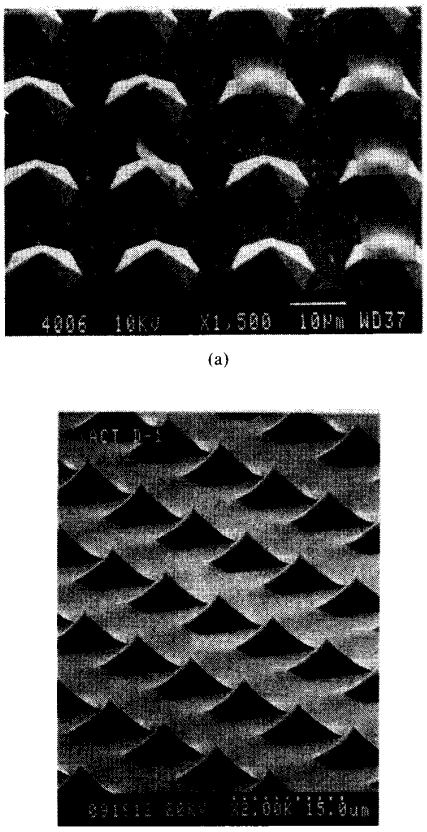
The second tip formation technique in this study uses the identical masking followed by etching in a common isotropic Si polish, $HNO_3:CH_3COOH:HF$ mixed 25:10:3 (by volume, standard MOS-grade aqueous reagents) at 25°C. The result is a very steep four-sided pyramid structure, again with approximately 100-nm radius of curvature at the tip, as-etched. An array of these cathode tips is shown in Fig. 1(b). For simplicity, in the ensuing text and figures, these two types of Si tips are referred to as "KOH" or "HF-HNO_3" tips, respectively.

The tip sharpening was performed by oxidation of the as-etched tips at 950°C in dry O_2 for 5 h. After the oxidation, the oxide is removed in HF, leaving the tips with only a native oxide and approximately 500 Å shorter than their original height. This sharpening technique has been shown to produce tips with a radius of curvature of the order of 10 Å [5].

B. Diode Structure for Measurement

Arrays of diodes were prepared for the measurements. In each case, 50 × 50 arrays of Si field emission tips were fabricated on a 1-mm square die. Nine dies were arranged (widely spaced) within a 1-in square on a single n-type wafer; after the tips were completely formed, the 1-in squares were cut from the wafer. The anode was made by thermally oxidizing a p-type Si wafer, wet etching windows through the oxide, coating the backside with Al, cutting to 1-in squares, and precision aligning the windows over the cathodes. The final structure was clamped together; the clamping is on the substrate support away from the diode assembly to assure there is no distortion of the anode-cathode spacing. Fig. 2 shows a schematic cross section of the final diode structure (not to scale, with the tips shown qualitatively only) which demonstrates the alignment and dielectric isolation. Care is necessary in arranging such devices to avoid particulates either separating or misaligning the cathode–anode assembly. The dielectric isolation between anode and cathode consists of a $SiO_2/Si_3N_4/SiO_2$ composite; this system of films was developed to eliminate any possible Frenkel–Poole conduction in the insulator. The average anode–cathode spacing in the measurements is 920 nm. Although we have no way of measuring the spacing variation in the final assembled structure, the total variation in the sharpened tip height is about 100 Å, due to the oxidation procedure. The goal in using this particular diode structure is to fix the array size and anode–cathode spacing and vary only the type of tips, e.g., KOH or HF-HNO_3, sharpened or unsharpened.

All measurements, regardless of temperature, were made in a diffusion- pumped vacuum cryostat with a room-



(a)

(b)

Fig. 1. Scanning electron micrographs of as-etched silicon field emission cathodes used in the measurements. (a) Section of anisotropically etched tip array, with Si_3N_4 masking still visible. (b) Isotropically etched tip array. (a) and (b) are referred to as "KOH tips" and "HF-HNO_3 tips," respectively, in the text and figures.

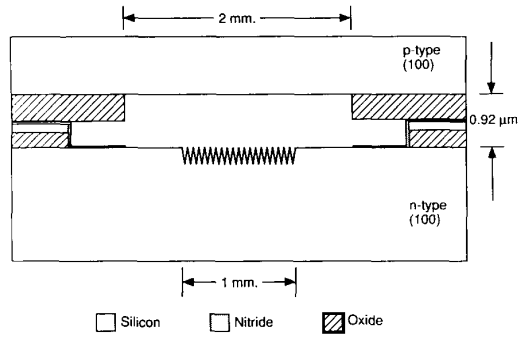


Fig. 2. Cross-section schematic diagram of the diode measurement structure. Drawing is conceptual only and not to scale. Arrays contained 50 × 50 tips, spaced on 20-μm centers.

temperature base pressure of 10^{-6} torr. The measurement structures, as described, were bonded to a sample holder within the cryostat. All measurement structures have nine parallel arrays of 2500 field emission points (e.g., 22500 tips in each individual diode structure). Although the arrays are quite precise, it is likely that some points do not emit. No separate experiment was undertaken to verify the exact number of tips emitting during a given measurement.

C. Field Enhancement Estimation

The expected enhancement (β) in the electric field, due to sharpening of the chemically etched cathodes, was calculated by dividing the maximum field on a tip by the parallel-plate field (that is the voltage divided by the tip-to-anode distance). The maximum field on the tip is calculated using a two-dimensional, finite-element static field code (STAT2D) described elsewhere [8]. Some of the results of this modeling are shown in Fig. 3(a) and (b). These examples directly correspond to the unsharpened KOH tip and sharpened HF–HNO_3 tip (the two extremes in tip radius) used in the measurements presented in this work. In these two cases, the anode–cathode tip spacing was 1.5 μm and there was 10 V applied. Only the tip regions are shown in Fig. 3 with the corresponding distribution of lines of uniform electric field. It should be noted that the scale factors in Fig. 3(a) and (b) differ by a factor of 20. In Fig. 3(a), the maximum electric field on the unsharpened KOH tip is 300 V · μm^{-1}. As expected, the sharpened HF–HNO_3 tips in Fig. 3(b) have a much higher maximum electric field of 2.0 kV · μm^{-1}, which is near the field ionization value for a pure Si tip.

The β value of the unsharpened tips is 47, whereas for the sharpened tips it is 300, giving an increase in β of a factor of 6.4. According to (1), this should result in a forty-fold increase in current density. A caveat in this estimation is that the model assumes the emission tip in each case is a smooth metallic surface. Sharpened tips with near atomic dimensions actually have an irregular surface morphology. It is unknown how this alters the field emission process, but this is being investigated in our on-going effort.

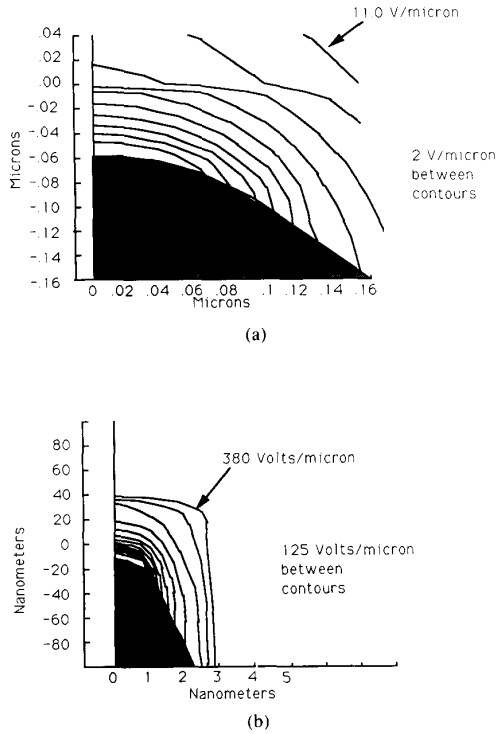


Fig. 3. Simulations of electric field in (a) as-etched KOH and (b) sharpened HF–HNO_3 tips. Note differing scales.

III. Results

Diode characteristics were reproducibly measured from our test structures. Fig. 4 shows room-temperature *I–V* measurements of as-etched and sharpened KOH and HF–HNO_3 cathode arrays. The two types of as-etched tips do not vary appreciably in conduction, despite the steeper sides of the HF–HNO_3 tips (see Fig. 1(a) and (b)). After sharpening, there is a nonlinear increase in current, although less than expected. The HF–HNO_3 tips did, in this case, conduct more than the KOH tips. The close anode–cathode spacing and the tip sharpness combined to produce the low operating voltage range of these devices. Most diode arrays failed (shorts) at applied voltages above 50 V. Fig. 4 also show Fowler–Nordheim (F–N) plots of the diode characteristics for both the as-etched and sharpened cases. The F–N plot is used in our case to verify conduction via field emission as opposed to some other rectifying mechanism.

Diode characteristics were also measured at various temperatures. A true field emission condition should be essentially temperature-insensitive. Fig. 5 shows *I–V* and F–N plots for an unsharpened KOH tip array at both room temperature and elevated to 360 K. The conduction is clearly field emission. Fig. 6(a) and (b) shows F–N plots for sharpened KOH (Fig. 6(a)) and sharpened HF–HNO_3 cathodes (Fig. 6(b)). In the case of Fig. 6(b), we see the expected temperature insensitivity over a wide range of temperatures. However, as seen in Fig. 6(a), the sharpened KOH cathode arrays did not conduct as expected. This is the only case in which we observed such a tem-

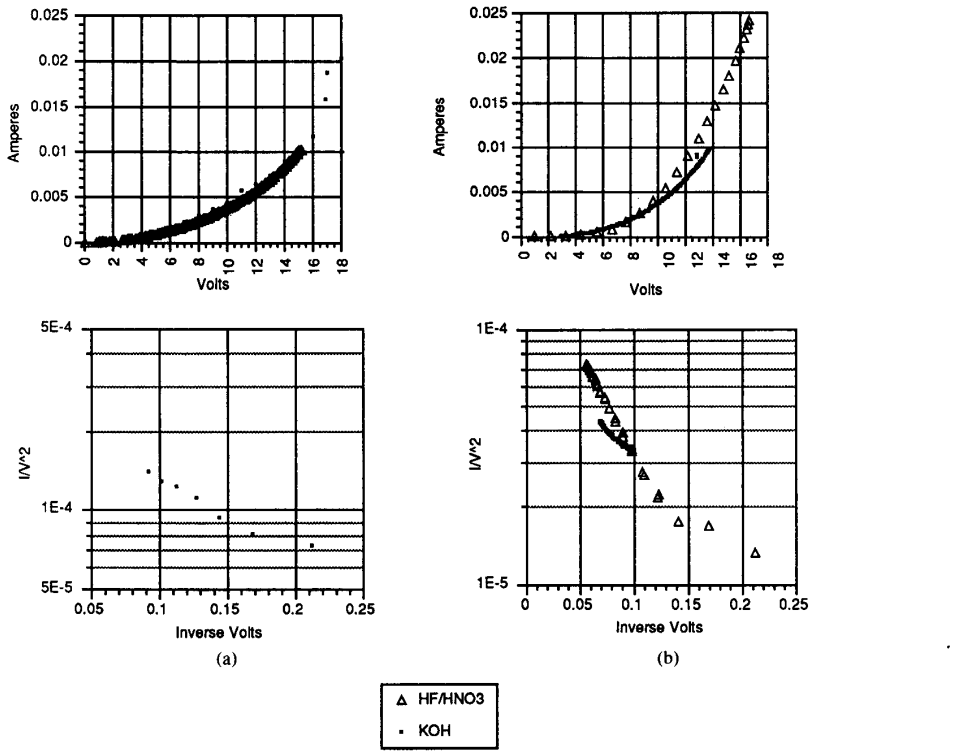


Fig. 4. *I–V* and Fowler–Nordheim (F–N) plots of room-temperture measurements made in (a) as-etched and (b) sharpened-tip diodes.

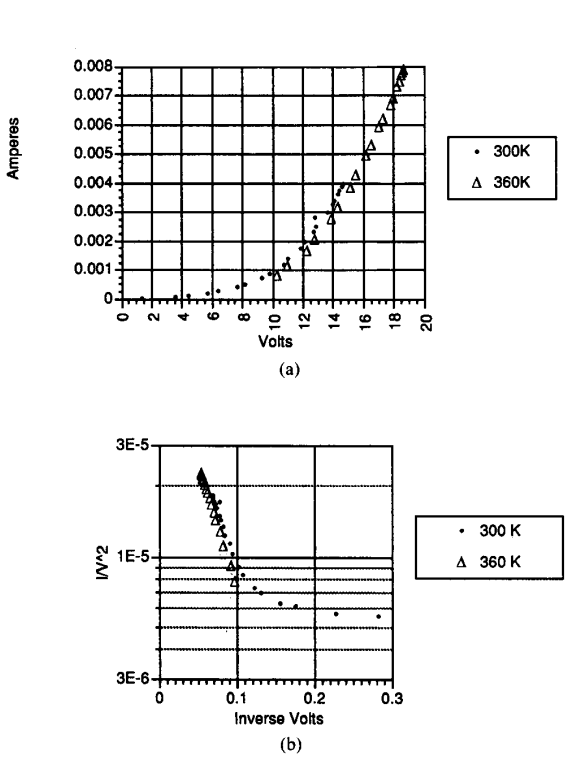


Fig. 5. (a) *I–V* and (b) F–N plots measured from an unsharpened KOH array at room temperature and elevated temperature.

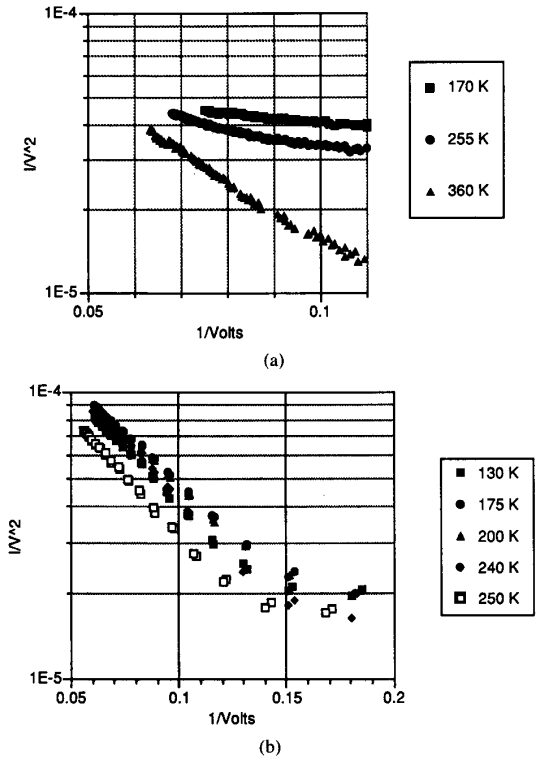


Fig. 6. F–N plots of emission from sharpened tips at various temperatures. (a) KOH tips and (b) $HF–HNO_3$ cathodes.

perature-dependant variation; we have no certain explanation of this anomaly to present here.

Noise was measured in these devices. The dominant noise observed at room temperature is telegraph noise of approximately 20 nA per tip at 20-V applied bias. Burst durations are typically 50–100 μs. This noise cannot be passivated. At elevated temperatures the noise level increases with increasingly variable magnitude. The noise also increases substantially if the pressure is increased. It is observed that the diodes operate for significant time (up to hours before failure) even at atmospheric pressure. In such cases, however, the noise value is very large; for example, at 25-V bias and 760 torr, the peak-peak noise is $\approx 20\%$ of the dc current.

IV. Discussion

The voltage at which there is significant conduction in these arrays (for example, 1 mA at 4-V applied bias) is lower than what has been reported with Spindt cathodes. This could be very important if these types of cathodes are to be used in applications integrated with standard microelectronic components, where supply voltages are typically 15 V or less. The 5-mA current at 10 V seen in Fig. 4 corresponds to 0.2 μA per tip if it is assumed that all tips are equally conducting. Since there must be some statistical variation in tip height, and correspondingly a variation in anode–cathode spacing between tips, it is reasonable to assume that some tips are not conducting and, as a result, single-tip structures may have greater current under similar conditions to those here.

If we assume that field emission occurs from discrete sites of constant area on these cathode tips, then the tip sharpening should cause the total current to increase proportionally with any increase in current density due to enhanced β (calculated to increase by a factor of 6.4 in this case). The increase in measured total current does not appear significant in sharpened cathodes except at higher (e.g., above 10 V) anode–cathode bias. There are several possible explanations for this. First, our inability to actually measure the anode–cathode spacing once the diode structure is assembled prevents us from proving that we have the exact same spacing for both the as-etched and sharpened cathodes. Furthermore, the oxidation process used in the sharpening does reduce the tip height somewhat and the exact value of this reduction is not easily measureable. It is possible that our anode–cathode spacing is greater in the sharpened tip case; such a condition would reduce the increase of β. A second possibility is that the sharpened tips are field-ionized (note the high fields in Fig. 3(b)) during initial operation and become unsharpened immediately upon conduction. A third possibility is that either the emission site area changes with tip sharpening so that increases in current density are not reflected by major increase in total current, or the emission from atomically sharp tips is seriously affected by the surface morphology.

The low-voltage operation characteristic seen in the F–N plot of Fig. 5 and Fig. 6(b), which appears to follow a significantly shallower slope than above 10 V, has been observed by others as well. A possible explanation, proposed elsewhere [9], may lie in statistical variations in the initial cathode turn-on voltage. This may also explain the temperature sensitivity in the sharpened KOH cathodes in Fig. 6(a): it is possible, because of the shallower angle of the KOH tips, that the statistical variations in height is greater after sharpening than in the $HF–HNO_3$ tip case. This could cause these tips to have differing break points between the two F–N curve slopes.

Although the average spacing in these measurements is 920 nm, the use of IC processing techniques with these types of cathodes makes virtually any spacing possible. It is likely that for reliable low-voltage operation, smaller spacings can be easily used, with correspondingly higher currents at a given bias and, possibly, lower turn-on voltage values.

V. Conclusions

We have measured low-voltage field emission from arrays of silicon cathode tips fabricated by wet chemical etching. A field-enhancement factor was simulated for cathodes which have been sharpened by low-temperature oxidation. Such sharpening produces a measurable increase in conduction, although with lower values than expected from the simulations. Minimum turn-on voltage is about 4 V. Tip current is at least 0.2 μA per tip at 10 V for sharpened tips. Temperature-insensitive field emission current is measured from 130 to 250 K using sharpened isotropically etched Si cathode tips.

It is believed that this cold cathode technology is viable for use in vacuum microelectronic devices, such as microtriodes, electron-beam instrumentation and applications, display applications, and microwave devices. The low-voltage operation is highly desirable in applications to vacuum integrated circuits or hybrids with existing IC technologies. These cathodes are adaptable to a self-aligned grid configuration, making a larger range of applications possible.

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